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P1 98.2



# N-CHANNEL MOS FIELD EFFECT POWER TRANSISTORS

## 2SK1059, 2SK1059-Z

**DESCRIPTION** The 2SK1059, 2SK1059-Z are N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

- FEATURES**
- 4 V Gate Drive — Logic level —
  - Low  $R_{DS(on)}$
  - No Second Breakdown
  - Designed for Hybrid Integrated Circuits

**ABSOLUTE MAXIMUM RATINGS**

Maximum Temperatures	
Storage Temperature . . . . .	-55 to +150 °C
Junction Temperature . . . . .	150 °C Maximum
Maximum Power Dissipations	
Total Power Dissipation* . . . . .	2.0 W
Total Power Dissipation ( $T_c = 25\text{ °C}$ )** . . . . .	20 W
Maximum Voltages and Currents ( $T_a = 25\text{ °C}$ )	
$V_{DSS}$ Drain to Source Voltage . . . . .	60 V
$V_{GSS}$ Gate to Source Voltage . . . . .	±20 V
$I_{D(DC)}$ Drain Current (DC) . . . . .	±5 A
$I_{D(pulse)}$ Drain Current (pulse)*** . . . . .	±20 A

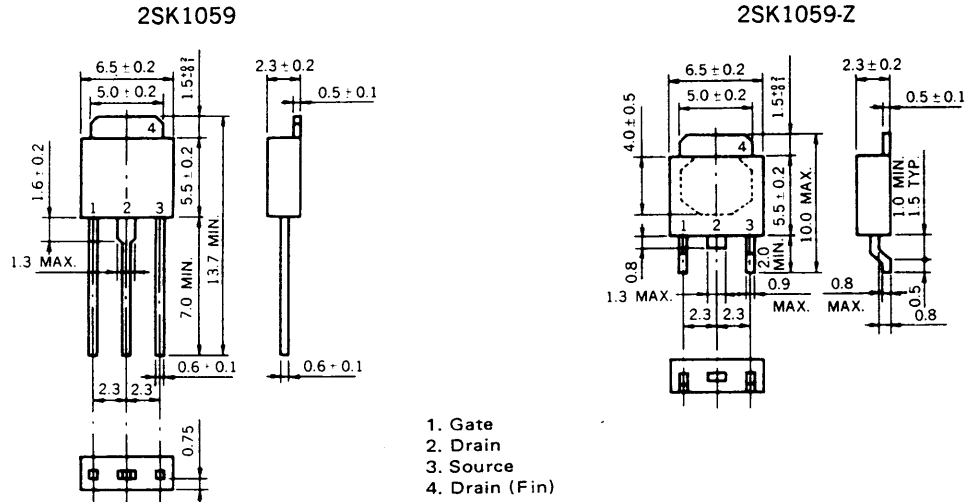
\* Mounted on ceramic substrate of 7.5 cm<sup>2</sup> x 0.7 mm  
 \*\*  $T_c = 25\text{ °C}$   
 \*\*\*  $PW \leq 10\ \mu s$ , Duty Cycle  $\leq 1\%$

**ELECTRICAL CHARACTERISTICS ( $T_a = 25\text{ °C}$ )**

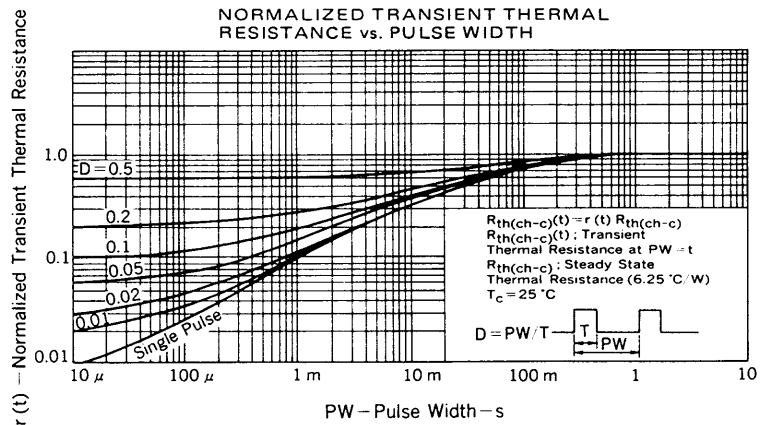
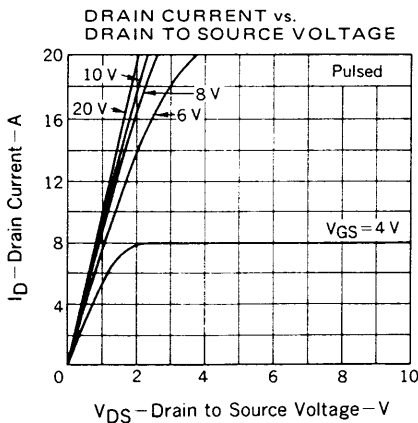
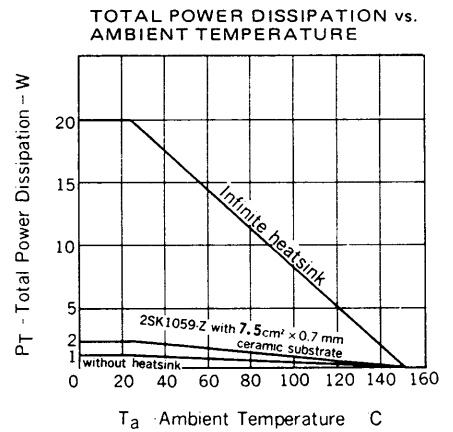
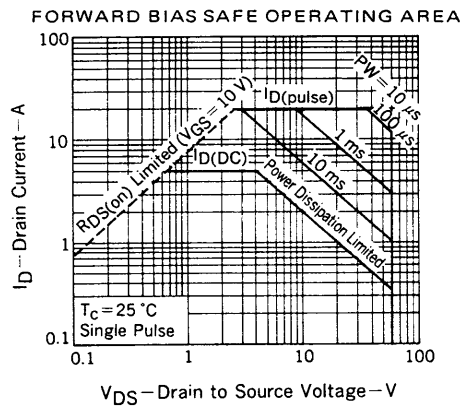
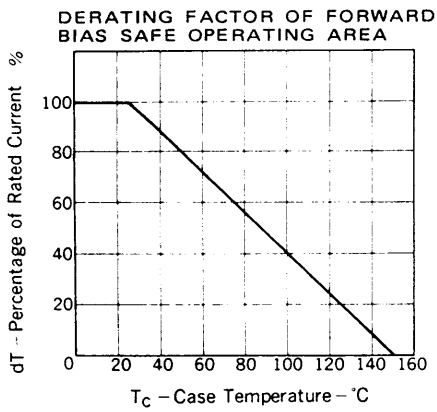
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.1	0.135	$\Omega$	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$
$R_{DS(on)}$	Drain to Source On-State Resistance		0.15	0.22	$\Omega$	$V_{GS} = 4\text{ V}, I_D = 3\text{ A}$
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$
$ y_{fs} $	Forward Transfer Admittance	4.0			S	$V_{DS} = 10\text{ V}, I_D = 3\text{ A}$
$I_{DSS}$	Drain Leakage Current			10	$\mu A$	$V_{DS} = 60\text{ V}, V_{GS} = 0$
$I_{GSS}$	Gate to Source Leakage Current			±100	nA	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0$
$C_{iss}$	Input Capacitance		900		pF	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
$C_{oss}$	Output Capacitance		350		pF	
$C_{rss}$	Reverse Transfer Capacitance		100		pF	
$t_{d(on)}$	Turn-On Delay Time		10		ns	$I_D = 3\text{ A}, V_{DD} = 10\text{ V}$ $R_L = 17\ \Omega$ $R_{in} = 10\ \Omega$
$t_r$	Rise Time		40		ns	
$t_{d(off)}$	Turn-Off Delay Time		110		ns	
$t_f$	Fall Time		30		ns	

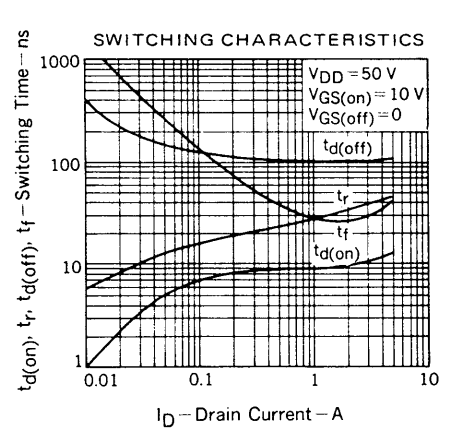
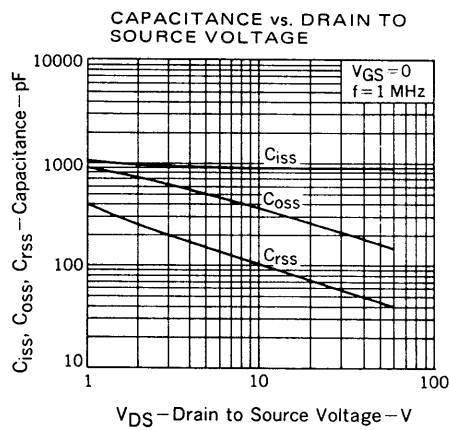
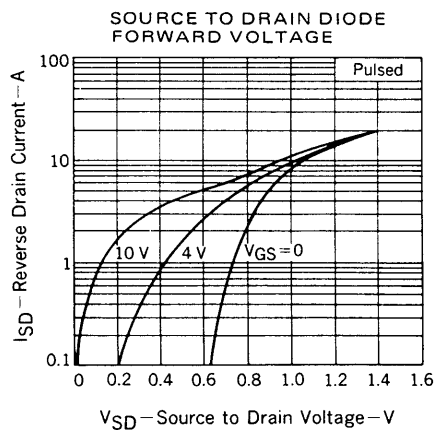
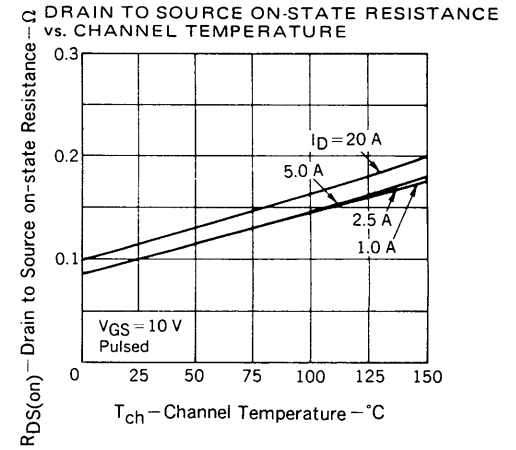
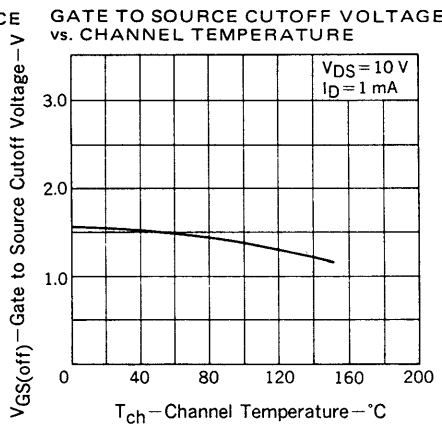
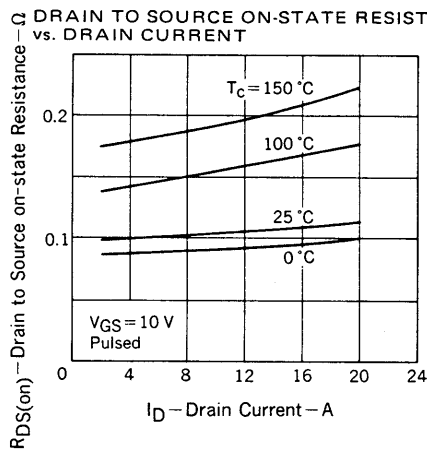
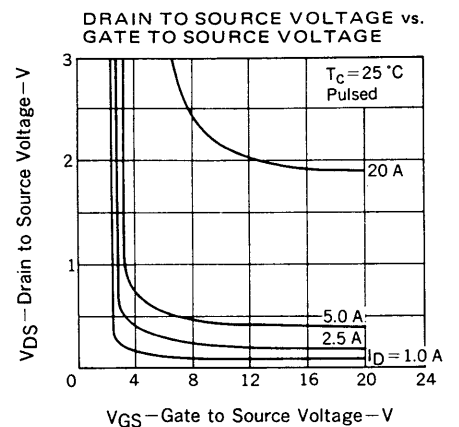
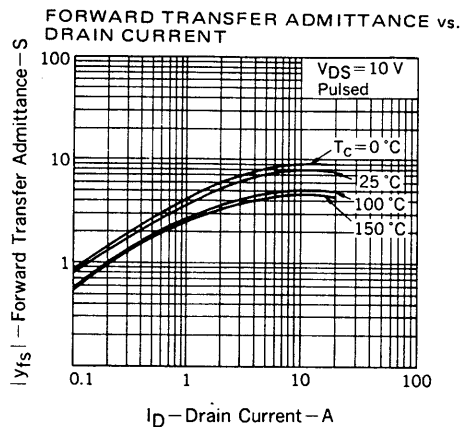
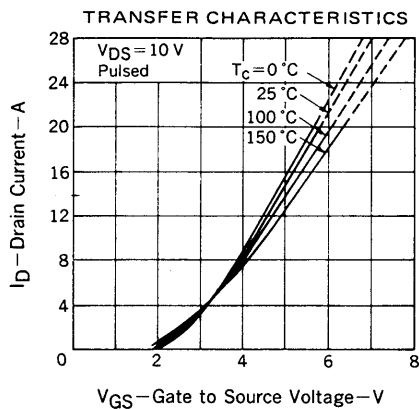
NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

**PACKAGE DIMENSIONS (Unit: mm)**

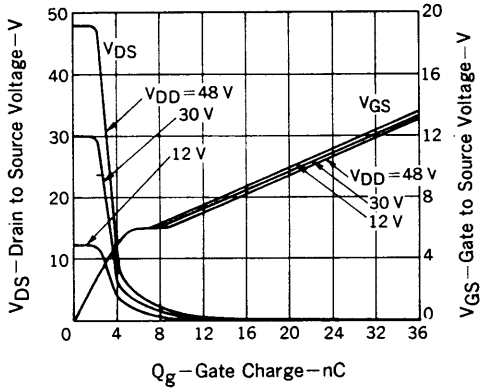


**TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

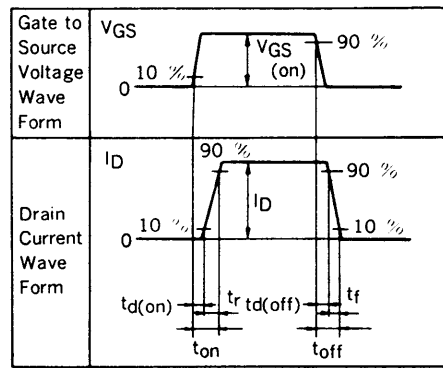
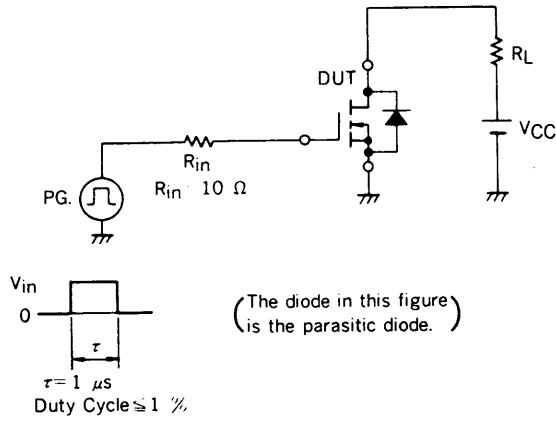




DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SWITCHING TIME TEST CIRCUIT



GATE CHARGE TEST CIRCUIT

