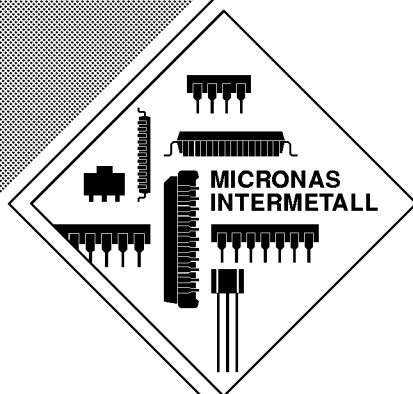


PRELIMINARY DATA SHEET

MSP 34x0G
Multistandard
Sound Processor Family



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Multistandard Sound Processor Family

The hardware and software description in this document is valid for the MSP 34x0G version A2 and following versions. One existing incompatibility to the version A1 is listed in the appendix section 7.

1. Introduction

The MSP 34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 1–1 shows a simplified functional block diagram of the MSP 34x0G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x0G has optimum stereo performance without any adjustments.

All MSP 34x0G versions are pin and software downward-compatible to the MSP 34x0D. The MSP 34x0G further simplifies controlling software. Standard selection requires a single I²C transmission only.

The MSP 34x0G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I²C interaction is necessary (Automatic Sound Selection).

The MSP 34x0G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China.

The ICs are produced in submicron CMOS technology. The MSP 34x0G is available in PLCC68, PSDIP64, PSDIP52, and in PQFP80 packages.

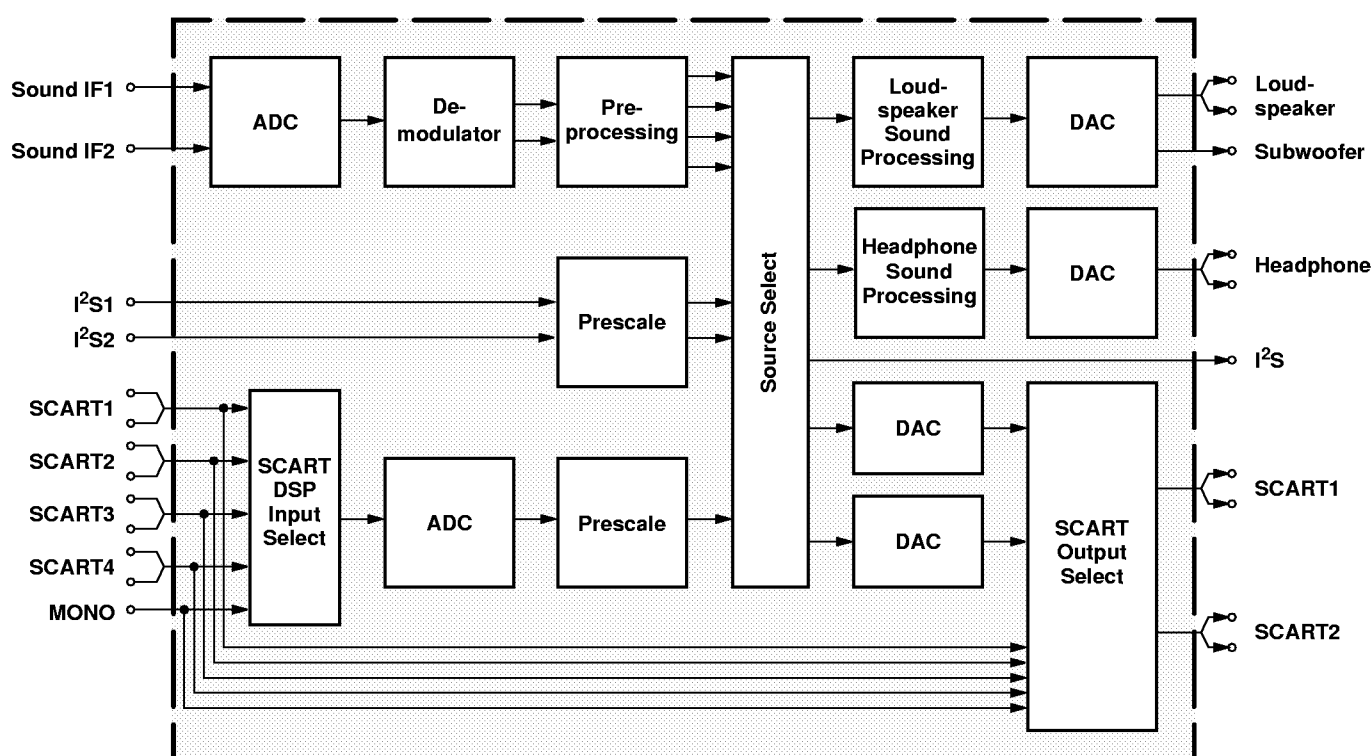


Fig. 1–1: Simplified functional block diagram of the MSP 34x0G

1.1. MSP 34x0G Version List

Version	Description
MSP 3410G (planned)	NICAM Version (can handle all A2 systems and all NICAM systems)
MSP 3430G (A1 available A3 available Q4/98)	BTSC Version
MSP 3440G (A3 available Q4/98)	NTSC Version (can handle A2 Korea system, the BTSC, and the Japanese EIA-J system)
MSP 3450G (planned)	Global Version (can handle all systems)

1.2. Features of the MSP 34x0G Family

1.2.1. Common Features of MSP 34x0G

- Standard Selection with single I²C transmission
- Automatic Sound Selection (mono, stereo, or bilingual)
- Automatic Carrier Mute function
- Interrupt output indicating status change
- Loudspeaker and headphone channel with balance, bass, treble, loudness, volume
- AVC: Automatic Volume Correction
- Subwoofer output with on-chip programmable low pass and complementary high-pass filters
- 5-band graphic equalizer for loudspeaker channel
- Spatial effect for loudspeaker channel
- Processing of all deemphasis filtering
- 2 selectable sound IF (SIF) inputs
- 4 Stereo SCART (line) inputs, 1 mono input
- 2 Stereo SCART (line) outputs
- Complete SCART in/out switching matrix
- 2 I²S inputs, 1 I²S output
- Dolby Pro Logic with DPL 351xA coprocessor

1.2.2. Specific Features of MSP 3410G

- Automatic Standard Detection of terrestrial TV standards
- All NICAM standards
- All analog FM-Stereo A2 standards
- Simultaneous demodulation of high-deviation FM-Mono and NICAM (China)
- Very high deviation FM-Mono mode (China, Eutelsat, etc.)
- FM demodulation of all analog satellite standards
- Adaptive deemphasis for satellite (according to ASTRA specification)
- ASTRA Digital Radio (ADR) together with DRP 3510A

1.2.3. Specific Features of MSP 3430G

- Demodulation of the BTSC multiplex signal
- Demodulation of the SAP channel
- Alignment free digital DBX noise reduction
- BTSC stereo separation significantly better than specification
- SAP and stereo detection for BTSC system
- Demodulation of the FM-Radio multiplex signal

1.2.4. Specific Features of MSP 3440G

- Automatic Standard Detection of terrestrial TV standards
- Demodulation of the BTSC multiplex signal
- Demodulation of the SAP channel
- Alignment free digital DBX noise reduction
- SAP and stereo detection for BTSC system
- Korean FM-Stereo A2 standard
- Alignment free Japanese standard EIA-J
- BTSC and EIA-J stereo separation significantly better than specification
- Demodulation of the FM-Radio multiplex signal

1.2.5. Specific Features of MSP 3450G

The MSP 3450G as a global multistandard IC contains **all features** listed above.

1.3. MSP 34x0G Versions and their Application Fields

Table 1–1 provides an overview of TV sound standards that can be processed by the MSP 34x0G family. In addition, the MSP 34x0G is able to handle the terrestrial FM-Radio standard. With the MSP 34x0G, a

complete multimedia receiver covering all TV sound standards together with terrestrial and satellite radio sound can be built; even ASTRA Digital Radio can be processed (with a DRP 3510A coprocessor).

Table 1–1: TV Sound Standards covered by the MSP 34x0G IC Family (details see Appendix A)

MSP Version				TV-System	Position of Sound Carrier /MHz	Sound Modulation	Color System	Broadcast e.g. in:
3430	3440	3410	3450	B/G	5.5/5.7421875	FM-Stereo (A2)	PAL	Germany
					5.5/5.85	FM-Mono/NICAM	PAL	Scandinavia, Spain
				L	6.5/5.85	AM-Mono/NICAM	SECAM-L	France
				I	6.0/6.552	FM-Mono/NICAM	PAL	UK, Hong Kong
				D/K	6.5/6.2578125	FM-Stereo (A2, D/K1)	SECAM-East	Slovak. Rep.
					6.5/6.7421875	FM-Stereo (A2, D/K2)	PAL	currently no broadcast
					6.5/5.85	FM-Mono/NICAM	PAL	China, Hungary
				Satellite	6.5 7.02/7.2 7.38/7.56 etc.	FM-Mono FM-Stereo ASTRA Digital Radio (ADR) with DRP 3510A	PAL	Europe Sat. ASTRA
				M	4.5/4.724212	FM-Stereo (A2)	NTSC	Korea
					4.5	FM-FM (EIA-J)	NTSC	Japan
					4.5	BTSC-Stereo + SAP	NTSC	USA
				FM-Radio	10.7	FM-Stereo Radio		USA, Europe

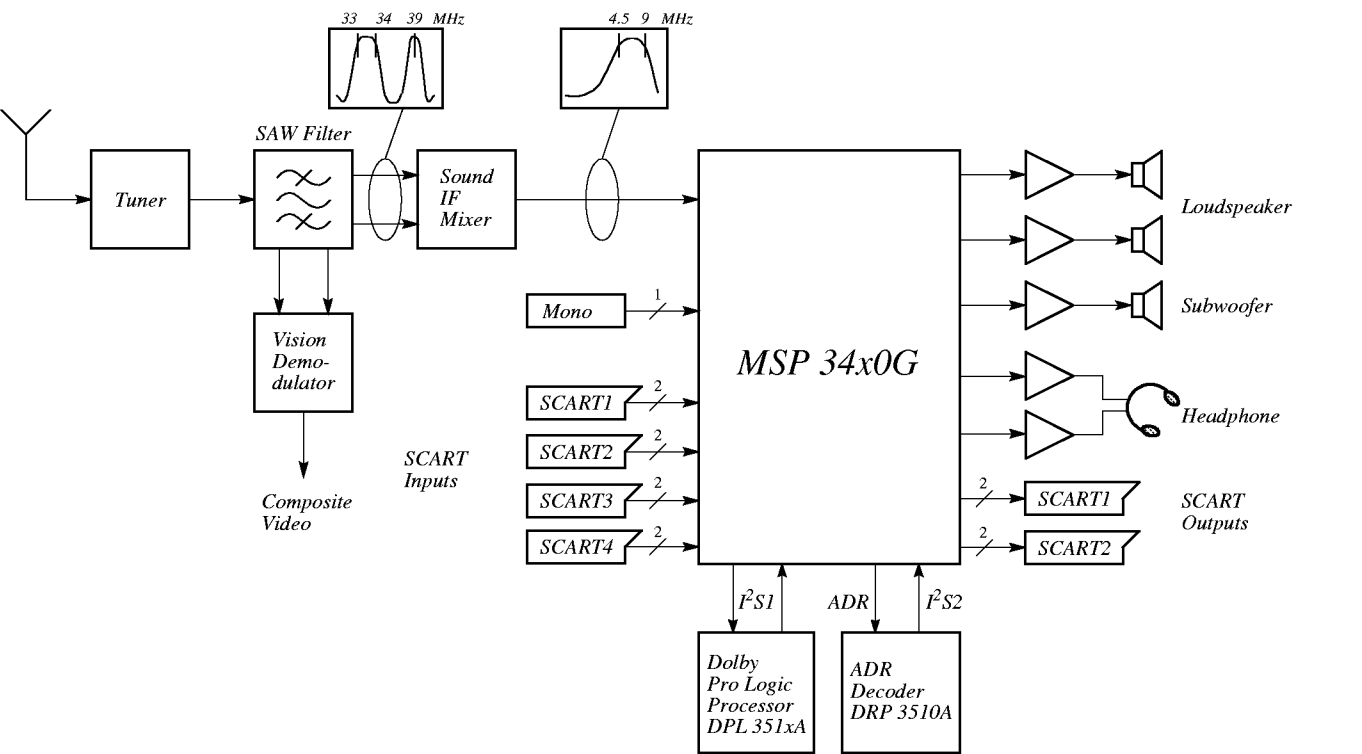


Fig. 1–2: Typical MSP 34x0G application

2. Functional Description

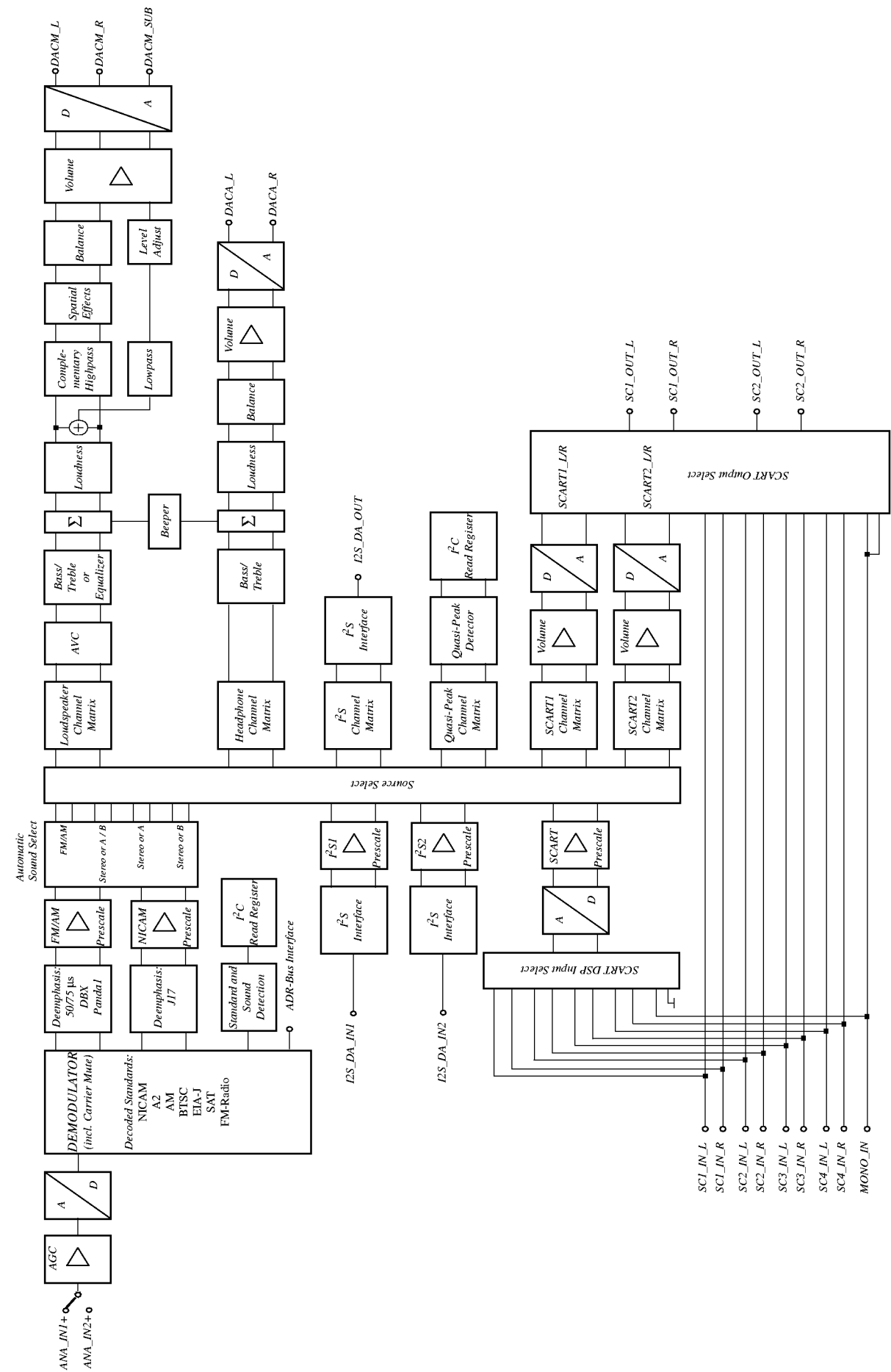


Fig. 2-1: Signal flow block diagram of the MSP 34x0G (input and output names correspond to pin names)

2.1. Architecture of the MSP 34x0G Family

Fig. 2–1 on page 8 shows a simplified block diagram of the IC. The block diagram contains all features of the MSP 3450G. Other members of the MSP 34x0G family do not have the complete set of features: The demodulator handles only a subset of the standards presented in the demodulator block; NICAM processing is only possible in the MSP 3410G and MSP 3450G.

2.2. Sound IF Processing

2.2.1. Analog Sound IF Input

The input pins ANA_IN1+, ANA_IN2+, and ANA_IN– offer the possibility to connect two different sound IF (SIF) sources to the MSP 34x0G. The analog-to-digital conversion of the preselected sound IF signal is done by an A/D-converter. An analog automatic gain circuit (AGC) allows a wide range of input levels. The high-pass filters formed by the coupling capacitors at pins ANA_IN1+ and ANA_IN2+ see Section 9. “Appendix E: Application Circuit” on page 91 are sufficient in most cases to suppress video components. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, further filtering is recommended.

2.2.2. Demodulator: Standards and Features

The MSP 34x0G is able to demodulate all TV-sound standards worldwide including the digital NICAM system. Depending on the MSP 34x0G version, the following demodulation modes can be performed:

A2 Systems: Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

NICAM Systems: Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog (FM or AM) carrier. For D/K-NICAM, the FM carrier may have a maximum deviation of 384 kHz.

Very high deviation FM-Mono: Detection and demodulation of one FM carrier with a maximum deviation of 540 kHz.

BTSC-Stereo: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L–R)-carrier and detection of the SAP sub-carrier. Processing of the DBX noise reduction.

BTSC-Mono + SAP: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP subcarrier. Processing of the DBX noise reduction.

Japan Stereo: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L–R)-carrier.

FM-Satellite Sound: Demodulation of one or two FM carriers. Processing of high-deviation mono or narrow bandwidth mono, stereo, or bilingual satellite sound according to the ASTRA specification.

FM-Stereo-Radio: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L–R)-carrier.

The demodulator blocks of all MSP 34x0G versions have identical user interfaces. Even completely different systems like the BTSC and NICAM systems are controlled the same way. Standards are selected by means of MSP Standard Codes. Automatic processes handle standard detection and identification without controller interaction. The key features of the MSP 34x0G demodulator blocks are

Standard Selection: The controlling of the demodulator is minimized: All parameters, such as tuning frequencies or filter bandwidth, are adjusted automatically by transmitting one single value to the STANDARD SELECT register. For all standards, specific MSP standard codes are defined.

Automatic Standard Detection: If the TV sound standard is unknown, the MSP 34x0G can automatically detect the actual standard, switch to that standard, and respond the actual MSP standard code.

Automatic Carrier Mute: To prevent noise effects or FM identification problems in the absence of an FM carrier, the MSP 34x0G offers a carrier mute feature, which is activated automatically if the TV sound standard is selected by means of the STANDARD SELECT register. If no FM carrier is available at one of the two MSP demodulator channels, the corresponding demodulator output is muted.

2.2.3. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The correct deemphasis filters are already selected by setting the standard in the STANDARD SELECT register. The level adjustment has to be done by means of the FM/AM and NICAM prescale registers. The necessary dematrix function depends on the selected sound standard and the actual broadcasted sound mode (mono, stereo, or bilingual). It can be manually set by the FM Matrix Mode register or automatically set by the Automatic Sound Selection.

2.2.4. Automatic Sound Select

In the Automatic Sound Select mode, the dematrix function is automatically selected based on the identification information in the STATUS register. No I²C interaction is necessary when the broadcasted sound mode changes (e.g. from mono to stereo).

The demodulator supports the identification check by switching between mono compatible standards (standards that have the same FM mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, and D/K-NICAM. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

In case of high bit-error rates, the MSP 34x0G automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2–1 summarizes all actions that take place when Automatic Sound Select is switched on.

To provide more flexibility, the Automatic Sound Select block prepares four different source channels of demodulated sound (Fig 2–3). By choosing one of the four demodulator channels, the preferred sound mode can be selected for each of the output channels (loudspeaker, headphone, etc.). This is done by means of the Source Select registers.

The following source channels of demodulated sound are defined:

- **“FM/AM” channel:** Analog mono sound, stereo if available. In case of NICAM, analog mono only (FM or AM mono).
- **“Stereo or A/B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).

- **“Stereo or A” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).
- **“Stereo or B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Fig 2–2 shows the source channel assignment of the demodulated signals in case of manual mode. If manual mode is required, more information can be found in the section “Demodulator Source Channels in Manual Mode” on page 84. Fig 2–3 and Table 2–2 show the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

Note: The analog primary input channel contains the signal of the mono FM/AM carrier or the L+R signal of the MPX carrier. The secondary input channel contains the signal of the 2nd FM carrier, the L–R signal of the MPX carrier, or the SAP signal.

2.3. Preprocessing for SCART and I²S Input Signals

The SCART and I²S inputs need only be adjusted in level by means of the SCART and I²S prescale registers.

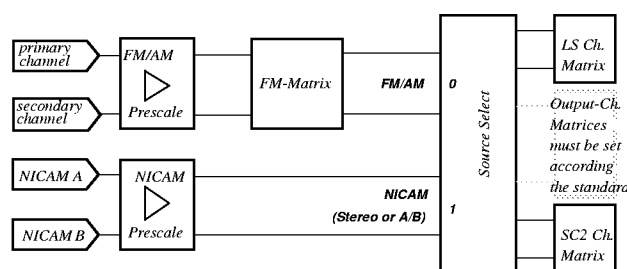


Fig. 2–2: Source channel assignment of demodulated signals in Manual Mode

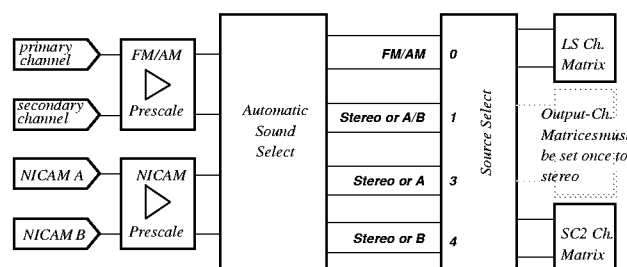


Fig. 2–3: Source channel assignment of demodulated signals in Automatic Sound Select Mode

Table 2–1: Performed actions of the Automatic Sound Selection

Selected TV Sound Standard	Performed Actions
B/G-FM, D/K-FM, M-Korea, and M-Japan	Evaluation of the identification signal and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. Identification is acquired after 500 ms.
B/G-NICAM, L-NICAM, I-NICAM, and D/K-NICAM	Evaluation of NICAM-C-bits and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. NICAM detection is acquired within 150 ms.
	In case of bad or no NICAM reception, the MSP switches automatically to FM/AM mono and switches back to NICAM if possible. A hysteresis prevents periodical switching.
B/G-FM, B/G-NICAM or D/K1-FM, D/K2-FM, D/K-NICAM	Automatic searching for stereo/bilingual-identification in case of mono transmission. Automatic and non-audible changes between Dual-FM and FM-NICAM standards while listening to the basic FM-Mono sound carrier. Example: If starting with B/G-FM-Stereo, there will be a periodical alternation to B/G-NICAM in the absence of FM-Stereo/Bilingual or NICAM-identification. Once an identification is detected, the MSP keeps the corresponding standard.
M-BTSC-STEREO, FM Radio	Evaluation of the pilot signal and automatic switching to mono or stereo. Preparing four demodulator source channels according to Table 2–2. Detection of the SAP carrier. Pilot detection is acquired after 200 ms.
M-BTSC-SAP	In the absence of SAP, the MSP switches to BTSC-Stereo if available. If SAP is detected, the MSP switches automatically to SAP (see Table 2–2).

Table 2–2: Sound modes for the demodulator source channels with Automatic Sound Select

			Source Channels in Automatic Sound Select Mode			
Broadcasted Sound Standard	Selected MSP Standard Code ³⁾	Broadcasted Sound Mode	FM/AM (source select: 0)	Stereo or A/B (source select: 1)	Stereo or A (source select: 3)	Stereo or B (source select: 4)
M-Korea B/G-FM D/K-FM M-Japan	02 03, 08 ¹⁾ 04, 05, 0B ¹⁾ 30	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo
		BILINGUAL: Languages A and B	Left = A Right = B	Left = A Right = B	A	B
B/G-NICAM L-NICAM I-NICAM D/K-NICAM D/K-NICAM (with high deviation FM)	08, 03 ²⁾ 09 0A 0B, 04 ²⁾ , 05 ²⁾ 0C	NICAM not available or error rate too high	analog Mono	analog Mono	analog Mono	analog Mono
		MONO	analog Mono	NICAM Mono	NICAM Mono	NICAM Mono
		STEREO	analog Mono	NICAM Stereo	NICAM Stereo	NICAM Stereo
		BILINGUAL: Languages A and B	analog Mono	Left = NICAM A Right = NICAM B	NICAM A	NICAM B
M-BTSC	20, 21	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo
	20	MONO+SAP	Mono	Mono	Mono	Mono
		STEREO+SAP	Stereo	Stereo	Stereo	Stereo
	21	MONO+SAP	Left = Mono Right = SAP	Left = Mono Right = SAP	Mono	SAP
		STEREO+SAP	Left = Mono Right = SAP	Left = Mono Right = SAP	Mono	SAP
FM Radio	40	MONO	Mono	Mono	Mono	Mono
		STEREO	Stereo	Stereo	Stereo	Stereo

¹⁾ The Automatic Sound Select process will automatically switch to the mono compatible analog standard.

²⁾ The Automatic Sound Select process will automatically switch to the mono compatible digital standard.

³⁾ The MSP Standard Codes are defined in Table 3–6 on page 20.

2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels, SCART, or I²S input) to the desired output channels (loudspeaker, headphone, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

2.5. Audio Baseband Processing

2.5.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The Automatic Volume Correction (AVC) solves this problem by equalizing the volume level.

Within a certain range, the AVC keeps the average output signal at a constant level. This is done by measuring the average amplitude of the incoming signal and calculating an appropriate correction gain. To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions (time constant: 16 ms). To suppress oscillation effects, the gain increases rather slowly for low level inputs. The time constant (normal range: 2–8 seconds) is programmable by means of the AVC register (see page 28).

In the following, the implemented levels are defined: If the input signal varies in a range of –24 dBr to 0 dBr, the AVC maintains a fixed output level of –18 dBr. A level of 0 dBr corresponds to full scale input or output (in case of SCART input or output, this is $2 V_{\text{RMS}}$, for loudspeaker output this is $1.4 V_{\text{RMS}}$. Condition: prescale and volume registers are in the 0 dB position). If the input signal is lower than –24 dBr, the AVC amplifies the input with a fixed gain of 6 dB.

Example: A static input signal of 1 kHz on SCART has an output level as shown in Table 2–3.

Table 2–3: Input/Output Characteristic of AVC

SCART Input 0 dBr = $2 V_{\text{RMS}}$	Volume Correction	Main Output 0 dBr = $1.4 V_{\text{RMS}}$
0 dBr	–18 dB	–18 dBr
–6 dBr	–12 dB	–18 dBr
–12 dBr	–6 dB	–18 dBr
–18 dBr	–0 dB	–18 dBr
–24 dBr	+6 dB	–18 dBr
–30 dBr	+6 dB	–24 dBr
(Conditions: Loudspeaker Volume = 73_{hex} = 0 dB, SCART Prescale = 20_{hex} = 0 dB)		

2.5.2. Loudspeaker and Headphone Outputs

The following baseband features are implemented in the loudspeaker and headphone output channels: bass/treble, loudness, balance, and volume. A square wave beeper can be added to the loudspeaker and headphone channel. The loudspeaker channel additionally performs: equalizer (not simultaneously with bass/treble), spatial effects, and a subwoofer cross-over filter.

2.5.3. Subwoofer Output

The subwoofer signal is created by combining the left and right channels directly behind the loudness block. It is filtered by a third-order low-pass with programmable corner frequency followed by a level adjustment. At the loudspeaker channels, a complementary high-pass filter can be switched on. Subwoofer and loudspeaker output use the same volume (Loudspeaker Volume Register).

2.5.4. Quasi-Peak Detector

The quasi-peak readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

attack time: 1.3 ms
decay time: 37 ms

2.6. SCART Signal Routing

2.6.1. SCART DSP In and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include full matrix switching facilities. To design a TV set with four pairs of SCART-inputs and two pairs of SCART-outputs, no external switching hardware is required. The switches are controlled by the ACB user register (see page 34).

2.6.2. Stand-by Mode

If the MSP 34x0G is switched off by first pulling STANDBYQ low and then (after $>1\ \mu\text{s}$ delay) switching off the 5-V, but keeping the 8-V power supply ('**Stand-by'-mode**), the SCART switches maintain their position and function. This allows the copying from selected SCART-inputs to SCART-outputs in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the 5-V supply, RESETQ going high 2 ms later), all internal registers except the ACB register (page 34) are reset to the default configuration (see Table 3–4 on page 18). The reset position of the ACB register becomes active after the first I²C transmission into the Baseband Processing part (subaddress 12_{hex}). By transmitting the ACB register first, the reset state can be redefined.

2.7. I²S Bus Interface

It is possible to route in an external coprocessor for special effects, like surround processing and sound field processing. Routing can be done with each input source and output channel via the I²S inputs and outputs.

Two possible interface formats are supported:

1. The SONY format: I2S_WS changes at the word boundaries.
2. The PHILIPS format: I2S_WS changes one I2S_CL period before the word boundaries.

The I²S bus interface consists of five pins:

1. I2S_DA_IN1, I2S_DA_IN2:
For input, four channels (two channels per line, 2*16 bits) per sampling cycle (32 kHz) are transmitted.
2. I2S_DA_OUT:
For output, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.
3. I2S_CL:
Gives the timing for the transmission of I²S serial data (1.024 MHz).
4. I2S_WS:
The I2S_WS word strobe line defines the left and right sample.

The MSP 34x0G normally serves as the master on the I²S interface. In this case, the clock and word strobe lines are driven by the MSP 34x0G. In slave mode, these lines are input to the MSP 34x0G and the master clock is synchronized to 576 times the I2S_WS rate (32 kHz). NICAM operation is not possible in this mode.

All I²S options can be set by means of the MODUS register (see page 22).

A precise I²S timing diagram is shown in Fig. 4–24 on page 61.

2.8. ADR Bus Interface

For the ASTRA Digital Radio System (ADR), the MSP 3410G and MSP 3450G performs preprocessing such as carrier selection and filtering. Via the 3-line ADR-bus, the resulting signals are transferred to the DRP 3510A coprocessor, where the source decoding is performed. To be prepared for an upgrade to ADR with an additional DRP board, the following lines of MSP 34x0G should be provided on a feature connector:

- AUD_CL_OUT
- I2S_DA_IN1 or I2S_DA_IN2
- I2S_DA_OUT
- I2S_WS
- I2S_CL
- ADR_CL, ADR_WS, ADR_DA

For more details, please refer to the DRP 3510A data sheet.

2.9. Digital Control I/O Pins and Status Change Indication

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the I²C-bus by means of the ACB register (see page 34). This enables the controlling of external hardware switches or other devices via I²C-bus.

The digital input/output pins can be set to high impedance by means of the MODUS register (see page 22). In this mode, the pins can be used as input. The current state can be read out of the STATUS register (see page 23).

Optionally, the pin D_CTR_I/O_1 can be used as an interrupt request signal to the controller, indicating any changes in the read register STATUS. This makes polling unnecessary, I²C bus interactions are reduced to a minimum (see STATUS register on page 23 and MODUS register on page 22).

2.10. Clock PLL Oscillator and Crystal Specifications

The MSP 34x0G derives all internal system clocks from the 18.432-MHz oscillator. In NICAM or in I²S-Slave mode, the clock is phase-locked to the corresponding source. Therefore, it is not possible to use NICAM and I²S-Slave mode at the same time.

For proper performance, the MSP clock oscillator requires a 18.432-MHz crystal. Note that for the phase-locked modes (NICAM, I²S-Slave), crystals with tighter tolerance are required.

Remark on using the crystal:

External capacitors at each crystal pin to ground are required. They are necessary for tuning the open-loop frequency of the internal PLL and for stabilizing the frequency in closed-loop operation. The higher the capacitors, the lower the resulting clock frequency. The nominal free running frequency should match 18.432 MHz as closely as possible.

Clock measurements should be done at pin AUD_CL_OUT. This pin must be activated for this purpose (see Table 3–8 on page 22).

3. Control Interface

3.1. I²C Bus Interface

3.1.1. Device and Subaddresses

The MSP 34x0G is controlled via the I²C bus slave interface.

The IC is selected by transmitting one of the MSP 34x0G device addresses. In order to allow up to three MSP ICs to be connected to a single bus, an address select pin (ADR_SEL) has been implemented. With ADR_SEL pulled to high, low, or left open, the MSP 34x0G responds to different device addresses. A device address pair is defined as a write address (80, 84, or 88 hex) and a read address (81, 85, or 89 hex) (see Table 3–1).

Writing is done by sending the device write address, followed by the subaddress byte, two address bytes, and two data bytes. Reading is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address (81, 85, or 89 hex) and reading two bytes of data. Refer to section 3.1.2. for the I²C bus protocol and to section “Programming Tips” on page 36 for proposals of MSP 34x0G I²C telegrams. See Table 3–2 for a list of available subaddresses.

By means of the RESET bit in the CONTROL register, the MSP can be reset by the controller.

Due to the internal architecture of the MSP 34x0G, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the MSP cannot accept another complete byte of data until it has performed some other function (for example, servicing an internal interrupt), it will hold the clock line I2C_CL LOW to force the transmitter into a wait state. The positions within a transmission where this may happen are indicated by 'Wait' in section 3.1.2. The maximum wait period of the MSP during normal operation mode is less than 1 ms.

Hardware problem handling:

In case of any hardware problems (e.g. interruption of the power supply of the MSP), the MSP's wait period is extended to 1.8 ms. After this time, the MSP does NOT send the acknowledge bit after the device address. The data line will be left HIGH by the MSP and the clock line will be released. The master can then generate a STOP condition to abort the transfer.

The master is able to recognize the error state by the missing acknowledge bit from the MSP. The MSP can be reset via I²C-bus by means of the CONTROL register. While transmitting the reset protocol to 'CONTROL', the master must ignore the missing acknowledge bits (NAK) from the MSP.

A general timing diagram of the I²C Bus is shown in Fig. 4–23 on page 59.

Table 3–1: I²C Bus Device Addresses

ADR_SEL	Low		High		Left Open	
Mode	Write	Read	Write	Read	Write	Read
MSP device address	80 hex	81 hex	84 hex	85 hex	88 hex	89 hex

Table 3–2: I²C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL	0000 0000	00	Write	software reset of MSP (see Table 3–3)
TEST	0000 0001	01	Write	only for internal use
WR_DEM	0001 0000	10	Write	write address demodulator
RD_DEM	0001 0001	11	Write	read address demodulator
WR_DSP	0001 0010	12	Write	write address DSP
RD_DSP	0001 0011	13	Write	read address DSP

Table 3–3: Control Register (Subaddress: 00_{hex})

Name	Subaddress	15 (MSB)	14	13..1	0 (LSB)
CONTROL	00 hex	1 : RESET 0 : normal	0	0	0

3.1.2. Protocol Description

Write to DSP or Demodulator

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte high	ACK	data-byte low	ACK	P
---	----------------------	------	-----	----------	-----	----------------	-----	---------------	-----	----------------	-----	---------------	-----	---

Read from DSP or Demodulator

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	read device address	Wait	ACK	data-byte high	ACK	data-byte low	NAK	P
---	----------------------	------	-----	----------	-----	----------------	-----	---------------	-----	---	---------------------	------	-----	----------------	-----	---------------	-----	---

Write to Control or Test Registers

S	write device address	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P
---	----------------------	------	-----	----------	-----	----------------	-----	---------------	-----	---

Note: S = I²C-Bus Start Condition from master
P = I²C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= MSP, light gray) or master (= controller dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate ‘End of Read’ or from MSP indicating internal error state
Wait = I²C-Clock line is held low, while the MSP is processing the I²C command. This waiting time is max. 1 ms

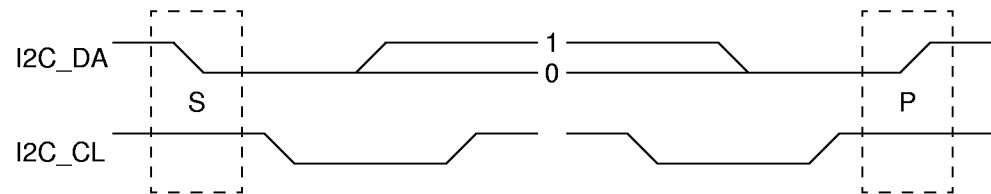


Fig. 3–1: I²C bus protocol (MSB first; data must be stable while clock is high)

3.1.3. Proposals for General MSP 34x0G I²C Telegrams

3.1.3.1. Symbols

daw	write device address (80 _{hex} , 84 _{hex} or 88 _{hex})
dar	read device address (81 _{hex} , 85 _{hex} or 89 _{hex})
<	Start Condition
>	Stop Condition
aa	Address Byte
dd	Data Byte

3.1.3.2. Write Telegrams

<daw 00 d0 00>	write to CONTROL register
<daw 10 aa aa dd dd>	write data into demodulator
<daw 12 aa aa dd dd>	write data into DSP

3.1.3.3. Read Telegrams

<daw 11 aa aa <dar dd dd>	read data from demodulator
<daw 13 aa aa <dar dd dd>	read data from DSP

3.1.3.4. Examples

<80 00 80 00>	RESET MSP statically
<80 00 00 00>	Clear RESET
<80 10 00 20 00 03>	Set demodulator to Standard 03 _{hex}
<80 11 02 00 <81 dd dd>	Read STATUS
<80 12 00 08 01 20>	Set loudspeaker channel source to NICAM and Matrix to STEREO

More examples of typical application protocols are listed in section "Programming Tips" on page 36.

3.2. Start-Up Sequence: Power-Up and I²C Controlling

After POWER ON or RESET (see Fig. 4–22), the IC is in an inactive state. All registers are in the reset position (see tables 3–4 and 3–5), the analog outputs are muted. The controller has to initialize all registers for which a non-default setting is necessary.

3.3. MSP 34x0G Programming Interface

3.3.1. User Registers Overview

The MSP 34x0G is controlled by means of user registers. The complete list of all user registers is given in the following tables. The registers are partitioned into the Demodulator section (Subaddress 10_{hex} for writing, 11_{hex} for reading) and the Baseband Processing sections (Subaddress 12_{hex} for writing, 13_{hex} for reading).

Write and read registers are 16-bit wide, whereby the MSB is denoted bit [15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, with the most significant byte transferred first). All write registers, except the demodulator write registers, are readable.

Unused parts of the 16-bit write registers must be zero.
Addresses not given in this table must not be written.

For reasons of software compatibility to the MSP 34x0D, an Expert/Compatibility Mode is available. More read and write registers together with a detailed description of the expert mode can be found in the "Appendix B: Expert/Compatibility Mode" on page 73.

An overview of all MSP 34x0G Write Registers is shown in Table 3–4; all Read Registers are given in Table 3–5.

Table 3–4: List of MSP 34x0G Write Registers

Write Register	Address (hex)	Bits	Description and Adjustable Range	Reset	See Page
I²C Subaddress = 10_{hex} ; Registers are <i>not</i> readable					
STANDARD SELECT	00 20	[15..0]	Initial Programming of complete Demodulator	00 00	21
MODUS	00 30	[15..0]	Demodulator, Automatic and I ² S options	00 00	22
I²C Subaddress = 12_{hex} ; Registers are <i>all</i> readable by using I²C Subaddress = 13_{hex}					
Volume loudspeaker channel	00 00	[15..8]	[+12 dB ... –114 dB, MUTE]	MUTE	27
Volume / Mode loudspeaker channel		[7..0]	1/8 dB Steps, Reduce Volume / Tone Control / Compromise	00 _{hex}	
Balance loudspeaker channel [L/R]	00 01	[15..8]	[0...100 / 100% and 100 / 0...100%] [–127...0 / 0 and 0 / –127...0 dB]	100%/100%	28
Balance mode loudspeaker		[7..0]	[Linear mode / logarithmic mode]	linear mode	
Bass loudspeaker channel	00 02	[15..8]	[+20 dB ... –12 dB]	0 dB	29
Treble loudspeaker channel	00 03	[15..8]	[+15 dB ... –12 dB]	0 dB	30
Loudness loudspeaker channel	00 04	[15..8]	[0 dB ... +17 dB]	0 dB	31
Loudness filter characteristic		[7..0]	[NORMAL, SUPER_BASS]	NORMAL	
Spatial effect strength loudspeaker ch.	00 05	[15..8]	[–100%...OFF...+100%]	OFF	32
Spatial effect mode/customize		[7..0]	[SBE, SBE+PSE]	SBE+PSE	
Volume headphone channel	00 06	[15..8]	[+12 dB ... –114 dB, MUTE]	MUTE	27
Volume / Mode headphone channel		[7..0]	1/8 dB Steps, Reduce Volume / Tone Control	00 _{hex}	
Volume SCART1 output channel	00 07	[15..8]	[+12 dB ... –114 dB, MUTE]	MUTE	33
Loudspeaker source select	00 08	[15..8]	[FM/AM, NICAM, SCART, I ² S1, I ² S2]	FM/AM	26
Loudspeaker channel matrix		[7..0]	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	26
Headphone source select	00 09	[15..8]	[FM/AM, NICAM, SCART, I ² S1, I ² S2]	FM/AM	26
Headphone channel matrix		[7..0]	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	26
SCART1 source select	00 0a	[15..8]	[FM/AM, NICAM, SCART, I ² S1, I ² S2]	FM/AM	26
SCART1 channel matrix		[7..0]	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	26
I ² S source select	00 0b	[15..8]	[FM/AM, NICAM, SCART, I ² S1, I ² S2]	FM/AM	26
I ² S channel matrix		[7..0]	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	26
Quasi-peak detector source select	00 0c	[15..8]	[FM/AM, NICAM, SCART, I ² S1, I ² S2]	FM/AM	26
Quasi-peak detector matrix		[7..0]	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	26
Prescale SCART input	00 0d	[15..8]	[00 _{hex} ... 7F _{hex}]	00 _{hex}	25
Prescale FM/AM	00 0e	[15..8]	[00 _{hex} ... 7F _{hex}]	00 _{hex}	24
FM matrix		[7..0]	[NO_MAT, GSTERERO, KSTEREO]	NO_MAT	25
Prescale NICAM	00 10	[15..8]	[00 _{hex} ... 7F _{hex}] (MSP 3410G, MSP 3450G only)	00 _{hex}	25
Prescale I ² S2	00 12	[15..8]	[00 _{hex} ... 7F _{hex}]	10 _{hex}	25
ACB : SCART Switches a. D_CTR_I/O	00 13	[15..0]	Bits [15..0]	00 _{hex}	34
Beeper	00 14	[15..0]	[00 _{hex} ... 7F _{hex}]/[00 _{hex} ... 7F _{hex}]	0/0	34
Prescale I ² S1	00 16	[15..8]	[00 _{hex} ... 7F _{hex}]	10 _{hex}	25
Mode tone control	00 20	[15..8]	[BASS/TREBLE, EQUALIZER]	BASS/TREB	29

Table 3–4: List of MSP 34x0G Write Registers, continued

Write Register	Address (hex)	Bits	Description and Adjustable Range	Reset	See Page
Equalizer loudspeaker ch. band 1	00 21	[15..8]	[+12 dB ... –12 dB]	0 dB	30
Equalizer loudspeaker ch. band 2	00 22	[15..8]	[+12 dB ... –12 dB]	0 dB	30
Equalizer loudspeaker ch. band 3	00 23	[15..8]	[+12 dB ... –12 dB]	0 dB	30
Equalizer loudspeaker ch. band 4	00 24	[15..8]	[+12 dB ... –12 dB]	0 dB	30
Equalizer loudspeaker ch. band 5	00 25	[15..8]	[+12 dB ... –12 dB]	0 dB	30
Automatic Volume Correction	00 29	[15..8]	[off, on, decay time]	off	28
Subwoofer level adjust	00 2C	[15..8]	[0 dB ... –30 dB, mute]	0 dB	33
Subwoofer corner frequency	00 2D	[15..8]	[50 Hz ... 400 Hz]	00 _{hex}	33
Subwoofer complementary high-pass		[7..0]	[off, on]	off	33
Balance headphone channel [L/R]	00 30	[15..8]	[0...100 / 100% and 100 / 0...100%] [–127...0 / 0 and 0 / –127...0 dB]	100 %/100 %	28
Balance mode headphone		[7..0]	[Linear mode / logarithmic mode]	linear mode	
Bass headphone channel	00 31	[15..8]	[+20 dB ... –12 dB]	0 dB	29
Treble headphone channel	00 32	[15..8]	[+15 dB ... –12 dB]	0 dB	30
Loudness headphone channel	00 33	[15..8]	[0 dB ... +17 dB]	0 dB	31
Loudness filter characteristic		[7..0]	[NORMAL, SUPER_BASS]	NORMAL	
Volume SCART2 output channel	00 40	[15..8]	[+12 dB ... –114 dB, MUTE]	00 _{hex}	33
SCART2 source select	00 41	[15..8]	[FM, NICAM, SCART, I ² S1, I ² S2]	FM	26
SCART2 channel matrix		[7..0]	[SOUNDA, SOUNDB, STEREO, MONO...]	SOUNDA	26

Table 3–5: List of MSP 34x0G Read Registers

Read Register	Address (hex)	Bits	Description and Adjustable Range	See Page
I²C Subaddress = 11_{hex} ; Registers are <i>not</i> writable				
STANDARD RESULT	00 7E	[15..0]	Result of Automatic Standard Detection (see Table 3–7) (MSP 3410G, MSP 3440G, MSP 3450G only)	23
STATUS	02 00	[15..0]	Monitoring of internal settings e.g. Stereo, Mono, Mute etc. .	23
I²C Subaddress = 13_{hex} ; Registers are <i>not</i> writable				
Quasi peak readout left	00 19	[15..0]	[00 _{hex} ... 7FFF _{hex}]16 bit two's complement	35
Quasi peak readout right	00 1A	[15..0]	[00 _{hex} ... 7FFF _{hex}]16 bit two's complement	35
MSP hardware version code	00 1E	[15..8]	[00 _{hex} ... FF _{hex}]	35
MSP major revision code		[7..0]	[00 _{hex} ... FF _{hex}]	35
MSP product code	00 1F	[15..8]	[00 _{hex} ... FF _{hex}]	35
MSP ROM version code		[7..0]	[00 _{hex} ... FF _{hex}]	35

3.3.2. Description of User Registers

Table 3–6: Standard Codes for STANDARD SELECT register

MSP Standard Code (Data in hex)	TV Sound Standard	Sound Carrier Frequencies	MSP 34x0G Version
Automatic Standard Detection			
00 01	Start Automatic Standard Detection		3410, 3430, 3440, 3450
Standard Selection			
00 02	M-Dual FM-Stereo	4.5/4.724212	3410, 3440, 3450
00 03	B/G -Dual FM-Stereo ¹⁾	5.5/5.7421875	3410, 3450
00 04	D/K1-Dual FM-Stereo ²⁾	6.5/6.2578125	
00 05	D/K2-Dual FM-Stereo ²⁾	6.5/6.7421875	
00 06	D/K -FM-Mono with HDEV3 ³⁾ , not detectable by Automatic Standard Detection, for China HDEV3 ³⁾ SAT-Mono (i.e. Eutelsat, s. Table 6–15)	6.5	
00 08	B/G -NICAM-FM ¹⁾	5.5/5.85	3410, 3450
00 09	L -NICAM-AM	6.5/5.85	
00 0A	I -NICAM-FM	6.0/6.552	
00 0B	D/K -NICAM-FM ²⁾	6.5/5.85	
00 0C	D/K -NICAM-FM with HDEV2 ⁴⁾ , not detectable by Automatic Standard Detection, for China	6.5/5.85	
00 20	M-BTSC-Stereo	4.5	3430, 3440, 3450
00 21	M-BTSC-Mono + SAP		
00 30	M-EIA-J Japan Stereo	4.5	3440, 3450
00 40	FM-Stereo Radio	10.7	3430, 3440, 3450
00 50	SAT-Mono (s. Table 6–15)	6.5	3410, 3450
00 51	SAT-Stereo (s. Table 6–15)	7.02/7.20	3410, 3450
00 60	SAT ADR (Astra Digital Radio)	7.2	3410, 3450
¹⁾ In case of Automatic Sound Select, the B/G-codes 3 _{hex} and 8 _{hex} are equivalent. ²⁾ In case of Automatic Sound Select, the D/K-codes 4 _{hex} , 5 _{hex} and B _{hex} are equivalent. ³⁾ HDEV3: Max. FM deviation must not exceed 540 kHz ⁴⁾ HDEV2: Max. FM deviation must not exceed 360 kHz			

3.3.2.1. STANDARD SELECT Register

The TV sound standard of the MSP 34x0G demodulator is determined by the STANDARD SELECT Register. There are two ways to use the STANDARD SELECT Register:

- Setting up the demodulator for a TV sound standard by sending the corresponding standard code with a single I²C-Bus transmission.
- Starting the Automatic Standard Detection for terrestrial TV standards. This is the most comfortable way to set up the demodulator (not for MSP 3430G). Within 0.5 s, the detection and set-up of the actual TV sound standard is performed. The detected standard can be read out of the STANDARD RESULT register by the control processor. This feature is recommended for the primary set-up of a TV set. Outputs should be muted during Automatic Standard Detection.

The Standard Codes are listed in Table 3–6.

Selecting a TV sound standard via the STANDARD SELECT register initializes the demodulator. This includes: AGC, tuning frequency, band-pass filters, demodulation mode (FM, AM, or NICAM), carrier mute, deemphasis, and identification mode.

If a present sound standard is impossible for a specific MSP version, it switches to the analog mono sound of this standard. In that case, stereo or bilingual processing will not be possible.

For a complete setup of the TV sound processing from analog IF input to the source selection, the following transmissions are necessary: MODUS register, STANDARD SELECT register, prescale values, FM matrix.

Note: The FM matrix is set automatically if Automatic Sound Select is active (MODUS[0]=1). In this case, the FM matrix will be initialized with “Sound A Mono”. During operation, the FM matrix will be automatically selected according to the actual identification information.

For reasons of software compatibility to the MSP 34x0D, an expert mode is available. A detailed description of the expert mode can be found on page 73.

3.3.2.2. STANDARD RESULT Register

If Automatic Standard Detection is selected in the STANDARD SELECT register, status and result of the Automatic Standard Detection process can be read out of the STANDARD RESULT register. The possible results are based on the mentioned Standard Code and are listed in Table 3–7.

In cases where no sound standard has been detected (no standard present, too much noise, strong interferers, etc.) the STANDARD RESULT register contains 00 00_{hex}. In that case, the controller has to start further actions (for example, set the standard according to a preference list or by manual input).

As long as the STANDARD RESULT register contains a value greater than 07 FF_{hex}, the Automatic Standard Detection is still active. During this period, the MODUS and STANDARD SELECT register must not be written. The STATUS register will be updated when the Automatic Standard Detection has finished.

If a present sound standard is impossible for a specific MSP version, it detects and switches to the analog mono sound of this standard.

Example:

The MSPs 3430G and 3440G will detect a B/G-NICAM signal as standard 3 and will switch to the analog FM-Mono sound.

Table 3–7: Results of the Automatic Standard Detection

Broadcasted Sound Standard	STANDARD RESULT Register Read 007E _{hex}
Automatic Standard Detection could not find a sound standard	0000 _{hex}
B/G-FM	0003 _{hex}
B/G-NICAM	0008 _{hex}
I	000A _{hex}
FM-Radio	0040 _{hex}
M-Korea M-Japan M-BTSC	0002 _{hex} (if MODUS[14,13]=00)
	0020 _{hex} (if MODUS[14,13]=01)
	0030 _{hex} (if MODUS[14,13]=10)
L-AM D/K1 D/K2	0009 _{hex} (if MODUS[12]=0)
	0004 _{hex} (if MODUS[12]=1)
L-NICAM D/K-NICAM	0009 _{hex} (if MODUS[12]=0)
	000B _{hex} (if MODUS[12]=1)
Automatic Standard Detection still active	>07FF _{hex}

3.3.2.3. Write Registers on I²C Subaddress 10_{hex}Table 3–8: Write Registers on I²C Subaddress 10_{hex}

Register Address	Function	Name
STANDARD SELECTION		
00 20 _{hex}	STANDARD SELECTION Register Defines TV Sound or FM-Radio Standard bit [15:0] 00 01 _{hex} start Automatic Standard Detection 00 02 _{hex} Standard Codes (see Table 3–6)) ... 00 60 _{hex}	STANDARD_SEL
MODUS		
00 30 _{hex}	MODUS Register General MSP 34x0G Options bit [0] 0/1 off/on: Automatic Sound Select bit [1] 0/1 disable/enable STATUS change indication by means of the digital I/O pin D_CTR_I/O_1 Necessary condition: MODUS[3] = 0 (active) bit [2] 0 undefined, must be 0 bit [3] 0 state of digital output pins D_CTR_I/O_0 and _1 active: D_CTR_I/O_0 and _1 are output pins (can be set by means of the ACB register. see also: MODUS[1]) 1 tristate: D_CTR_I/O_0 and _1 are input pins (level can be read out of STATUS[4,3]) bit [4] 0/1 active/tristate state of I ² S output pins bit [5] 0/1 master/slave mode of I ² S interface (must be set to 0 (= Master) in case of NICAM mode) bit [6] 0/1 Sony/Philips format of I ² S word strobe bit [7] 0/1 active/tristate state of audio clock output pin AUD_CL_OUT bit [8] 0/1 ANA_IN_1+/ANA_IN_2+; select analog sound IF input pin bit [11:9] 0 undefined, must be 0 Preference in Automatic Standard Detection: bit [12] 0 detected 6.5 MHz carrier is interpreted as: ¹⁾ 0 standard L (SECAM) 1 standard D/K1, D/K2 or D/K NICAM bit [14:13] 0 detected 4.5 MHz carrier is interpreted as: ¹⁾ 0 standard M (Korea) 1 standard M (BTSC) 2 standard M (Japan) bit [15] 0 undefined, must be 0	MODUS
¹⁾ Valid at the next start of Automatic Standard Detection.		

3.3.2.4. Read Registers on I²C Subaddress 11_{hex}

Table 3–9: Read Registers on I²C Subaddress 11_{hex}

Register Address	Function	Name
STANDARD RESULT		
00 7E _{hex}	STANDARD RESULT Register Readback of the detected TV Sound or FM-Radio Standard bit [15:0] 00 00 _{hex} Automatic Standard Detection could not find a sound standard 00 02 _{hex} MSP Standard Codes (see Table 3–7) ... 00 40 _{hex} >07 FF _{hex} Automatic Standard Detection still active	STANDARD_RES
STATUS		
02 00 _{hex}	STATUS Register Contains all user relevant internal information about the status of the MSP bit [0] undefined bit [1] 0 detected primary carrier (Mono or MPX carrier) 1 no primary carrier detected bit [2] 0 detected secondary carrier (2nd A2 or SAP carrier) 1 no secondary carrier detected bit [3] 0/1 low/high level of digital I/O pin D_CTR_I/O_0 bit [4] 0/1 low/high level of digital I/O pin D_CTR_I/O_1 bit [5,9] 00 analog sound standard (FM or AM) active 01 not obtainable 10 digital sound (NICAM) available (MSP 3410G and MSP 3450G only) 11 bad reception condition of digital sound (NICAM) due to: a. high error rate b. unimplemented sound code c. data transmission only bit [6] 0/1 mono/stereo indication bit [7] 0/1 “1” indicates independent mono sound (only for NICAM on MSP 3410G and MSP 3450G) bit [8] 0/1 “1” indicates bilingual sound mode or SAP present bit [15:10] undefined If STATUS change indication is activated by means of MODUS[1]: Each change in the STATUS register sets the digital I/O pin D_CTR_I/O_1 to high level. Reading the STATUS register resets D_CTR_I/O_1.	STATUS

3.3.2.5. Write Registers on I²C Subaddress 12_{hex}Table 3–10: Write Registers on I²C Subaddress 12_{hex}

Register Address	Function	Name
PREPROCESSING		
00 0E _{hex}	FM/AM Prescale Defines the input prescale value for the demodulated FM or AM signal bit [15:8] 00 _{hex} off (RESET condition) FM mode given FM deviation leads to internal full scale bit [15:8] 7F _{hex} 28 kHz 48 _{hex} 50 kHz 30 _{hex} 75 kHz 24 _{hex} 100 kHz 18 _{hex} 150 kHz 13 _{hex} 180 kHz (limit) FM high deviation mode (HDEV2, MSP Standard Code = C _{hex}) bit [15:8] 30 _{hex} 150 kHz 14 _{hex} 360 kHz (limit) FM very high deviation mode (HDEV3, MSP Standard Code = 6) bit [15:8] 20 _{hex} 450 kHz 1A _{hex} 540 kHz (limit) Satellite FM with adaptive deemphasis bit [15:8] 10 _{hex} recommendation AM mode (MSP Standard Code = 9) bit [15:8] 7C _{hex} recommendation for SIF input levels from 0.1 V _{pp} to 0.8 V _{pp} (Due to the AGC switched on, the AM-output level remains stable and independent of the actual SIF-level in the mentioned input range)	PRE_FM

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name
(continued)	FM Matrix Modes	FM_MATRIX
00 0E _{hex}	<p>Defines the dematrix function for the demodulated FM signal</p> <p>bit [7:0] 00_{hex} no matrix (used for bilingual and unmatrixed stereo sound) 01_{hex} German stereo (Standard B/G) 02_{hex} Korean stereo (also used for BTSC, EIA-J and FM Radio) 03_{hex} sound A mono (left and right channel contain the mono sound of the FM/AM mono carrier)</p> <p>In case of Automatic Sound Select, the FM Matrix Mode is set automatically, i.e. the low-part of any I²C transmission to the register 00 0E_{hex} is ignored.</p> <p>To enable a Forced Mono Mode for all analog stereo systems by overriding the internal pilot or identification evaluation, the following steps must be transmitted:</p> <ol style="list-style-type: none"> 1. MODUS with bit[0] = 0 (Automatic Sound Select off) 2. FM Presc./Matrix with FM Matrix = Sound A Mono (SAP: Sound B Mono) 3. Select FM/AM source channel, with channel matrix set to “Stereo” (transparent) 	
00 10 _{hex}	<p>NICAM Prescale</p> <p>Defines the input prescale value for the digital NICAM signal</p> <p>bit [15:8] 00_{hex} off 20_{hex} 0 dB gain 5A_{hex} 9 dB gain (recommendation) 7F_{hex} +12 dB gain (maximum gain)</p>	PRE_NICAM
00 16 _{hex} 00 12 _{hex}	<p>I2S1 Prescale I2S2 Prescale</p> <p>Defines the input prescale value for digital I²S input signals</p> <p>bit [15:8] 00_{hex} off 10_{hex} 0 dB gain (recommendation) 7F_{hex} +18 dB gain (maximum gain)</p>	PRE_I2S1 PRE_I2S2
00 0D _{hex}	<p>SCART Input Prescale</p> <p>Defines the input prescale value for the analog SCART input signal</p> <p>bit [15:8] 00_{hex} off 19_{hex} 0 dB gain (2 V_{RMS} input to digital full scale) 7F_{hex} +14 dB gain (400 mV_{RMS} input to digital full scale)</p>	PRE_SCART

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name
SOURCE SELECT AND OUTPUT CHANNEL MATRIX		
00 08 _{hex} 00 09 _{hex} 00 0A _{hex} 00 41 _{hex} 00 0B _{hex} 00 0C _{hex}	<p>Source for:</p> <p>Loudspeaker Output Headphone Output SCART1 DA Output SCART2 DA Output I²S Output Quasi-Peak Detector</p> <p>bit [15:8] 0 “FM/AM”: demodulated FM or AM mono signal</p> <p>1 “Stereo or A/B”: demodulator Stereo or A/B signal (in manual mode, this source is identical to the NICAM source in the MSP 3410D)</p> <p>3 “Stereo or A”: demodulator Stereo Sound or Language A (only defined for Automatic Sound Select)</p> <p>4 “Stereo or B”: demodulator Stereo Sound or Language B (only defined for Automatic Sound Select)</p> <p>2 SCART input</p> <p>5 I²S1 input</p> <p>6 I²S2 input</p> <p>For demodulator sources, see Table 2–2.</p>	SRC_MAIN SRC_AUX SRC_SCART1 SRC_SCART2 SRC_I2S SRC_QPEAK
00 08 _{hex} 00 09 _{hex} 00 0A _{hex} 00 41 _{hex} 00 0B _{hex} 00 0C _{hex}	<p>Matrix Mode for:</p> <p>Loudspeaker Output Headphone Output SCART1 DA Output SCART2 DA Output I²S Output Quasi-Peak Detector</p> <p>bit [7:0] 00_{hex} Sound A Mono (or Left Mono) 10_{hex} Sound B Mono (or Right Mono) 20_{hex} Stereo (transparent mode) 30_{hex} Mono (sum of left and right inputs divided by 2)</p> <p>In Automatic Sound Select mode, the demodulator source channels are set according to Table 2–2. Therefore, the matrix modes of the corresponding output channels should be set to “Stereo” (transparent).</p>	MAT_MAIN MAT_AUX MAT_SCART1 MAT_SCART2 MAT_I2S MAT_QPEAK

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name																
LOUDSPEAKER AND HEADPHONE PROCESSING																		
00 00 _{hex} 00 06 _{hex}	<p>Volume Loudspeaker Volume Headphone</p> <p>bit [15:8] volume table with 1 dB step size</p> <p>7F_{hex} +12 dB (maximum volume) 7E_{hex} +11 dB ... 74_{hex} +1 dB 73_{hex} 0 dB 72_{hex} -1 dB ... 02_{hex} -113 dB 01_{hex} -114 dB 00_{hex} Mute (reset condition) FF_{hex} Fast Mute</p> <p>bit [7:5] higher resolution volume table</p> <p>0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table</p> <p>bit [3:0] clipping mode</p> <p>0 reduce volume 1 reduce tone control 2 compromise mode</p> <p>With large scale input signals, positive volume settings may lead to signal clipping.</p> <p>The MSP 34x0G loudspeaker and headphone volume function is divided into a digital and an analog section. With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. To turn volume on again, the volume step that has been used before Fast Mute was activated must be transmitted.</p> <p>If the clipping mode is set to “Reduce Volume”, the following rule is used: To prevent severe clipping effects with bass, treble, or equalizer boosts, the internal volume is automatically limited to a level where, in combination with either bass, treble, or equalizer setting, the amplification does not exceed 12 dB.</p> <p>If the clipping mode is “Reduce Tone Control”, the bass or treble value is reduced if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced, where amplification together with volume exceeds 12 dB.</p> <p>If the clipping mode is “Compromise Mode”, the bass or treble value and volume are reduced half and half if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced half and half, where amplification together with volume exceeds 12 dB.</p> <p>Example:</p> <table><tr><td></td><td><u>Vol.: +6 dB</u></td><td><u>Bass: +9 dB</u></td><td><u>Treble: +5 dB</u></td></tr><tr><td>Red. Volume</td><td>3</td><td>9</td><td>5</td></tr><tr><td>Red. Tone Con.</td><td>6</td><td>6</td><td>5</td></tr><tr><td>Compromise</td><td>4.5</td><td>7.5</td><td>5</td></tr></table>		<u>Vol.: +6 dB</u>	<u>Bass: +9 dB</u>	<u>Treble: +5 dB</u>	Red. Volume	3	9	5	Red. Tone Con.	6	6	5	Compromise	4.5	7.5	5	VOL_MAIN VOL_AUX
	<u>Vol.: +6 dB</u>	<u>Bass: +9 dB</u>	<u>Treble: +5 dB</u>															
Red. Volume	3	9	5															
Red. Tone Con.	6	6	5															
Compromise	4.5	7.5	5															

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 29 _{hex}	Automatic Volume Correction (AVC) Loudspeaker Channel bit [15:12] 00 _{hex} AVC off (and reset internal variables) 08 _{hex} AVC on bit [11:8] 08 _{hex} 8 sec decay time 04 _{hex} 4 sec decay time 02 _{hex} 2 sec decay time 01 _{hex} 20 ms decay time Note: To reset the internal variables, the AVC should be switched off and then on again during any channel or source change. For standard applications, the recommended decay time is 4 sec. Note: AVC should not be used in any Dolby Prologic mode (with DPL 35xx), except in PANORAMA or 3D-PANORAMA mode, when only the loudspeaker output is active.	AVC
00 01 _{hex} 00 30 _{hex}	Balance Loudspeaker Channel Balance Headphone Channel bit [3:0] Balance Mode 0 _{hex} linear 1 _{hex} logarithmic bit [15:8] Linear Mode 7F _{hex} Left muted, Right 100% 7E _{hex} Left 0.8%, Right 100% ... 01 _{hex} Left 99.2%, Right 100% 00 _{hex} Left 100%, Right 100% FF _{hex} Left 100%, Right 99.2% ... 82 _{hex} Left 100%, Right 0.8% 81 _{hex} Left 100%, Right muted bit [15:8] Logarithmic Mode 7F _{hex} Left –127 dB, Right 0 dB 7E _{hex} Left –126 dB, Right 0 dB ... 01 _{hex} Left –1 dB, Right 0 dB 00 _{hex} Left 0 dB, Right 0 dB FF _{hex} Left 0 dB, Right –1 dB ... 81 _{hex} Left 0 dB, Right –127 dB 80 _{hex} Left 0 dB, Right –128 dB Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected.	BAL_MAIN BAL_AUX

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 20 _{hex}	Tone Control Mode Loudspeaker Channel bit [15:8] 00 _{hex} bass and treble is active FF _{hex} equalizer is active Defines whether Bass/Treble or Equalizer is activated for the loudspeaker channel. Bass and Equalizer cannot work simultaneously. If Equalizer is used, Bass, and Treble coefficients must be set to zero and vice versa.	TONE_MODE
00 02 _{hex} 00 31 _{hex}	Bass Loudspeaker Channel Bass Headphone Channel bit [15:8] normal range 60 _{hex} +12 dB 58 _{hex} +11 dB ... 08 _{hex} +1 dB 00 _{hex} 0 dB F8 _{hex} –1 dB ... A8 _{hex} –11 dB A0 _{hex} –12 dB bit [15:8] extended range 7F _{hex} +20 dB 78 _{hex} +18 dB 70 _{hex} +16 dB 68 _{hex} +14 dB Higher resolution is possible: an LSB step in the normal range results in a gain step of about 1/8 dB, in the extended range about 1/4 dB. With positive bass settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain.	BASS_MAIN BASS_AUX

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 03 _{hex} 00 32 _{hex}	Treble Loudspeaker Channel Treble Headphone Channel bit [15:8] 78 _{hex} +15 dB 70 _{hex} +14 dB ... 08 _{hex} +1 dB 00 _{hex} 0 dB F8 _{hex} –1 dB ... A8 _{hex} –11 dB A0 _{hex} –12 dB Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB. With positive treble settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain.	TREB_MAIN TREB_AUX
00 21 _{hex} 00 22 _{hex} 00 23 _{hex} 00 24 _{hex} 00 25 _{hex}	Equalizer Loudspeaker Channel Band 1 (below 120 Hz) Equalizer Loudspeaker Channel Band 2 (center: 500 Hz) Equalizer Loudspeaker Channel Band 3 (center: 1.5 kHz) Equalizer Loudspeaker Channel Band 4 (center: 5 kHz) Equalizer Loudspeaker Channel Band 5 (above: 10 kHz) bit [15:8] 60 _{hex} +12 dB 58 _{hex} +11 dB ... 08 _{hex} +1 dB 00 _{hex} 0 dB F8 _{hex} –1 dB ... A8 _{hex} –11 dB A0 _{hex} –12 dB Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB. With positive equalizer settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain.	EQUAL_BAND1 EQUAL_BAND2 EQUAL_BAND3 EQUAL_BAND4 EQUAL_BAND5

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name														
00 04 _{hex} 00 33 _{hex}	<p>Loudness Loudspeaker Channel</p> <p>Loudness Headphone Channel</p> <p>bit [15:8] Loudness Gain</p> <table><tr><td>44_{hex}</td><td>+17 dB</td></tr><tr><td>40_{hex}</td><td>+16 dB</td></tr><tr><td>...</td><td></td></tr><tr><td>04_{hex}</td><td>+1 dB</td></tr><tr><td>00_{hex}</td><td>0 dB</td></tr></table> <p>bit [7:0] Loudness Mode</p> <table><tr><td>00_{hex}</td><td>normal (constant volume at 1 kHz)</td></tr><tr><td>04_{hex}</td><td>Super Bass (constant volume at 2 kHz)</td></tr></table> <p>Higher resolution of Loudness Gain is possible: An LSB step results in a gain step of about 1/4 dB.</p> <p>Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the 1-kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain.</p> <p>The corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.</p>	44 _{hex}	+17 dB	40 _{hex}	+16 dB	...		04 _{hex}	+1 dB	00 _{hex}	0 dB	00 _{hex}	normal (constant volume at 1 kHz)	04 _{hex}	Super Bass (constant volume at 2 kHz)	LOUD_MAIN LOUD_AUX
44 _{hex}	+17 dB															
40 _{hex}	+16 dB															
...																
04 _{hex}	+1 dB															
00 _{hex}	0 dB															
00 _{hex}	normal (constant volume at 1 kHz)															
04 _{hex}	Super Bass (constant volume at 2 kHz)															

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name
00 05 _{hex}	<p>Spatial Effects Loudspeaker Channel</p> <p>bit [15:8] Effect Strength</p> <p>7F_{hex} Enlargement 100%</p> <p>3F_{hex} Enlargement 50%</p> <p>...</p> <p>01_{hex} Enlargement 1.5%</p> <p>00_{hex} Effect off</p> <p>FF_{hex} reduction 1.5%</p> <p>...</p> <p>C0_{hex} reduction 50%</p> <p>80_{hex} reduction 100%</p> <p>bit [7:4] Spatial Effect Mode</p> <p>0_{hex} Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). (Mode A)</p> <p>2_{hex} Stereo Basewidth Enlargement (SBE) only. (Mode B)</p> <p>bit [3:0] Spatial Effect High-Pass Gain</p> <p>0_{hex} max. high-pass gain</p> <p>2_{hex} 2/3 high-pass gain</p> <p>4_{hex} 1/3 high-pass gain</p> <p>6_{hex} min. high-pass gain</p> <p>8_{hex} automatic</p> <p>There are several spatial effect modes available:</p> <p>In mode A (low byte = 00_{hex}), the spatial effect depends on the source mode. If the incoming signal is mono, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. The strength of the effect is controllable by the upper byte. A negative value reduces the stereo image. A strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large screen TV sets, a more moderate spatial effect is recommended.</p> <p>In mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.</p> <p>It is worth mentioning, that all spatial effects affect amplitude and phase response. With the lower 4 bits, the frequency response can be customized. A value of 0_{hex} yields a flat response for center signals (L = R), but a high-pass function for L or R only signals. A value of 6_{hex} has a flat response for L or R only signals, but a low-pass function for center signals. By using 8_{hex}, the frequency response is automatically adapted to the sound material by choosing an optimal high-pass gain.</p>	SPAT_MAIN

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name
SUBWOOFER OUTPUT CHANNEL		
00 2C _{hex}	Subwoofer Level Adjustment bit [15:8] 00 _{hex} 0 dB FF _{hex} −1 dB ... E3 _{hex} −29 dB E2 _{hex} −30 dB ... 80 _{hex} Mute	SUBW_LEVEL
00 2D _{hex}	Subwoofer Corner Frequency bit [15:8] 5...40 corner frequency in 10-Hz steps (range: 50...400 Hz) Subwoofer Complementary High-Pass Filter bit [7:0] 00 _{hex} loudspeaker channel unfiltered 01 _{hex} a complementary high-pass is processed in the loud- speaker output channel	SUBW_FREQ SUBW_HP
SCART OUTPUT CHANNEL		
00 07 _{hex} 00 40 _{hex}	Volume SCART1 Output Channel Volume SCART2 Output Channel bit [15:8] volume table with 1 dB step size 7F _{hex} +12 dB (maximum volume) 7E _{hex} +11 dB ... 74 _{hex} +1 dB 73 _{hex} 0 dB 72 _{hex} −1 dB ... 02 _{hex} −113 dB 01 _{hex} −114 dB 00 _{hex} Mute (reset condition) bit [7:5] higher resolution volume table 0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table bit [4:0] 01 _{hex} this must be 01 _{hex}	VOL_SCART1 VOL_SCART2

Table 3–10: Write Registers on I²C Subaddress 12_{hex}, continued

Register Address	Function	Name
SCART SWITCHES AND DIGITAL I/O PINS		
00 13 _{hex}	<p>ACB Register</p> <p>Defines the level of the digital output pins and the position of the SCART switches</p> <p>bit [15] 0/1 low/high of digital output pin D_CTR_I/O_0 (MODUS[3]=0)</p> <p>bit [14] 0/1 low/high of digital output pin D_CTR_I/O_1 (MODUS[3]=0)</p> <p>bit [13:5] SCART DSP Input Select</p> <p> xxx00xx0 SCART1 to DSP input (RESET position)</p> <p> xxx01xx0 MONO to DSP input (Sound A Mono must be selected in the channel matrix mode for the corresponding output channels)</p> <p> xxx10xx0 SCART2 to DSP input</p> <p> xxx11xx0 SCART3 to DSP input</p> <p> xxx00xx1 SCART4 to DSP input</p> <p> xxx11xx1 mute DSP input</p> <p>bit [13:5] SCART1 Output Select</p> <p> xx00xxx0x SCART3 input to SCART1 output (RESET position)</p> <p> xx01xxx0x SCART2 input to SCART1 output</p> <p> xx10xxx0x MONO input to SCART1 output</p> <p> xx11xxx0x SCART1 DA to SCART1 output</p> <p> xx00xxx1x SCART2 DA to SCART1 output</p> <p> xx01xxx1x SCART1 input to SCART1 output</p> <p> xx10xxx1x SCART4 input to SCART1 output</p> <p> xx11xxx1x mute SCART1 output</p> <p>bit [13:5] SCART2 Output Select</p> <p> 00xxxx0xx SCART1 DA to SCART2 output (RESET position)</p> <p> 01xxxx0xx SCART1 input to SCART2 output</p> <p> 10xxxx0xx MONO input to SCART2 output</p> <p> 00xxxx1xx SCART2 DA to SCART2 output</p> <p> 01xxxx1xx SCART2 input to SCART2 output</p> <p> 10xxxx1xx SCART3 input to SCART2 output</p> <p> 11xxxx1xx SCART4 input to SCART2 output</p> <p> 11xxxx0xx mute SCART2 output</p> <p>The RESET position becomes active at the time of the first write transmission on the control bus to the audio processing part. By writing to the ACB register first, the RESET state can be redefined.</p>	ACB_REG
BEEPER		
00 14 _{hex}	<p>Beeper Volume and Frequency</p> <p>bit [15:8] Beeper Volume</p> <p> 00_{hex} off</p> <p> 7F_{hex} maximum volume</p> <p>bit [7:0] Beeper Frequency</p> <p> 01_{hex} 16 Hz (lowest)</p> <p> 40_{hex} 1 kHz</p> <p> FF_{hex} 4 kHz</p>	BEEPER

3.3.2.6. Read Registers on I²C Subaddress 13_{hex}

Table 3–11: Read Registers on I²C Subaddress 13_{hex}

Register Address	Function	Name
QUASI-PEAK DETECTOR READOUT		
00 19 _{hex} 00 1a _{hex}	Quasi-Peak Detector Readout Left Quasi-Peak Detector Readout Right bit [15..0] 0 _{hex} ... 7FFF _{hex} values are 16 bit two's complement (only positive)	QPEAK_L QPEAK_R
MSP 34X0G VERSION READOUT REGISTERS		
00 1E _{hex}	MSP Hardware Version Code bit [15..8] 01 _{hex} MSP 34x0G - A2 A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint. MSP Major Revision Code bit [7..0] 07 _{hex} MSP 34x0G - A2 The major revision code of the MSP 3410G is 7.	MSP_HARD MSP_REVISION
00 1F _{hex}	MSP Product Code bit [15..8] 0A _{hex} MSP 3MSP 3410G - A2 1E _{hex} MSP 3430G - A2 28 _{hex} MSP 3440G - A2 32 _{hex} MSP 3450G - A2 By means of the MSP-Product Code, the control processor is able to decide which TV sound standards have to be considered. MSP ROM Version Code bit [7..0] 41 _{hex} MSP 34x0G - A1 42 _{hex} MSP 34x0G - A2 A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new MSP 34x0G versions according to this number. To avoid compatibility problems with MSP 3410B and MSP 34x0D, an offset of 40 _{hex} is added to the ROM version code of the chip's imprint.	MSP_PRODUCT MSP_ROM

3.4. Programming Tips

This section describes the preferred method for initializing the MSP 34x0G. The initialization is grouped into four sections: analog signal path, demodulator input, input processing for SCART and I²S, and output processing. See Fig. 2–1 on page 8 for a complete signal flow.

SCART Signal Path

1. Select analog input for the SCART baseband processing (SCART DSP Input Select) by means of the ACB register.
2. Select the source for each analog SCART output (SCART Output Select) by means of the ACB register.

Demodulator Input

For a complete setup of the TV sound processing from analog IF input to the source selection, the following steps must be performed:

1. Set MODUS register to the preferred mode and Sound IF input.
2. Write STANDARD SELECT register.
3. Choose preferred prescale (FM and NICAM) values.

If Automatic Sound Select is not active, the following step has to be done repeatedly:

4. Choose FM matrix according to the sound mode indicated in the STATUS register.

SCART and I²S Inputs

1. Select preferred prescale for SCART.
2. Select preferred prescale for I²S inputs (set to 0 dB after RESET).

Output Channels

1. Select the source channel and matrix for each output channel.
2. Set audio baseband processing.
3. Select volume for each output channel.

3.5. Examples of Minimum Initialization Codes

Initialization of the MSP 34x0G according to these listings reproduces sound of the selected standard on the loudspeaker output. All numbers are hexadecimal. The examples have the following structure:

1. Perform an I²C controlled reset of the IC.
2. Write MODUS register (with Automatic Sound Select).
3. Write STANDARD SELECT register.
4. Set Prescale (FM and/or NICAM and dummy FM matrix).
5. Set Source Selection for loudspeaker channel (with matrix set to STEREO).
6. Set Volume loudspeaker channel to 0 dB.

3.5.1. B/G-FM (A2 or NICAM)

```
<80 00 80 00> // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 10 00 20 00 03> // Standard Select: A2 B/G or NICAM B/G
                        or
<80 10 00 20 00 08>
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
                        FM-Matrix = MONO/SOUNDA
<80 12 00 10 00 5A> // NICAM-Prescale = 5Ahex
<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB
```

3.5.2. BTSC-Stereo

```
<80 00 80 00> // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 10 00 20 00 20> // Standard Select: BTSC-STEREO
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
                        FM-Matrix = Sound A Mono
<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB
```

3.5.3. BTSC-SAP with SAP at Loudspeaker Channel

```
<80 00 80 00> // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 10 00 20 00 21> // Standard Select: BTSC-SAP
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
                        FM-Matrix = Sound A Mono
<80 12 00 08 04 20> // Source Sel. = (St or B) & Ch. Matr. = St
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB
```

3.5.4. FM-Stereo Radio

```

<80 00 80 00>      // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 10 00 20 00 40> // Standard Select: FM-STEREO
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
                    // FM-Matrix = Sound A Mono
<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB

```

3.5.5. Automatic Standard Detection

```

<80 00 80 00>      // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 10 00 20 00 01> // Standard Select:
                    // Automatic Standard Detection
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
                    // FM-Matrix = Sound A Mono
<80 12 00 10 00 5A> // NICAM-Prescale = 5Ahex
<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St
// Wait till STANDARD RESULT contains a value ≤ 07FF
// IF STANDARD RESULT contains 0000
// do some error handling
// ELSE
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB

```

3.5.6. Software Flow for Interrupt driven STATUS Check

If the D_CTR_I/O_1 pin of the MSP 34x0G is connected to an interrupt input pin of the controller, the following interrupt handler can be applied to be automatically called with each status change of the MSP 34x0G. The interrupt handler may adjust the TV display according to the new status information.

Interrupt Handler:

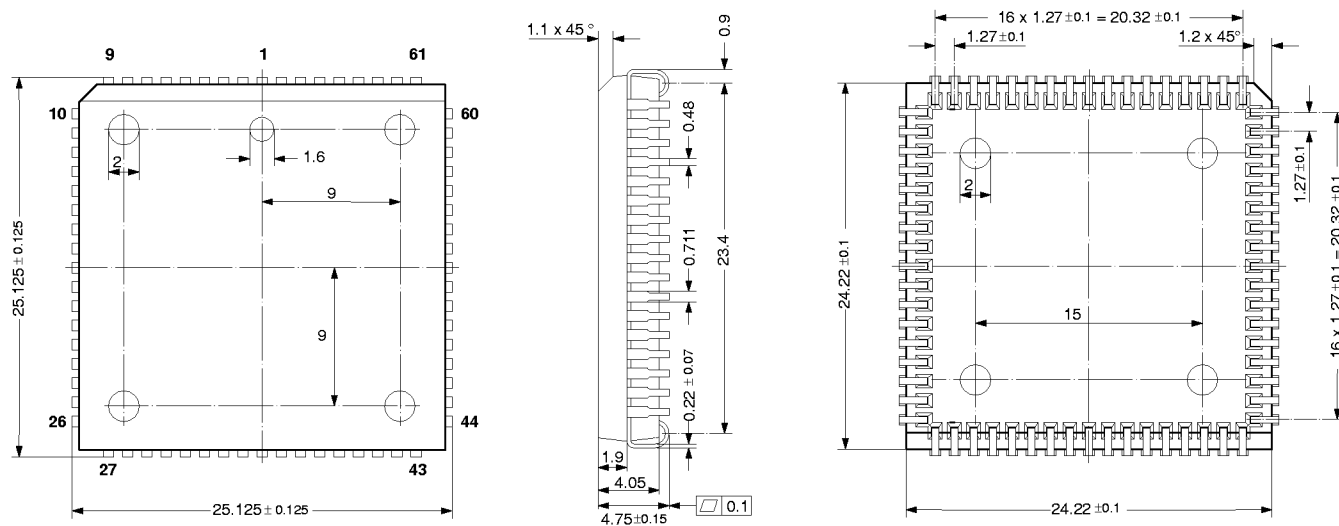
```

<80 11 02 00 <81 dd dd> // Read STATUS
// adjust TV display with given status information
// Return from Interrupt

```

4. Specifications

4.1. Outline Dimensions



SPGS7004-3/5E

Fig. 4-1:
68-Pin Plastic Leaded Chip Carrier Package
(**PLCC68**)
Weight approximately 4.8 g
Dimensions in mm

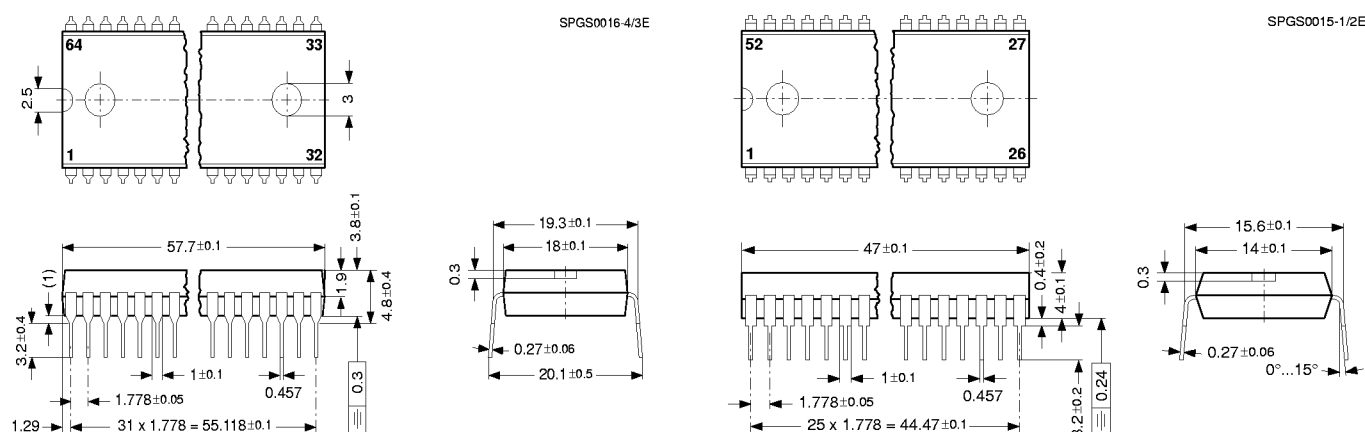
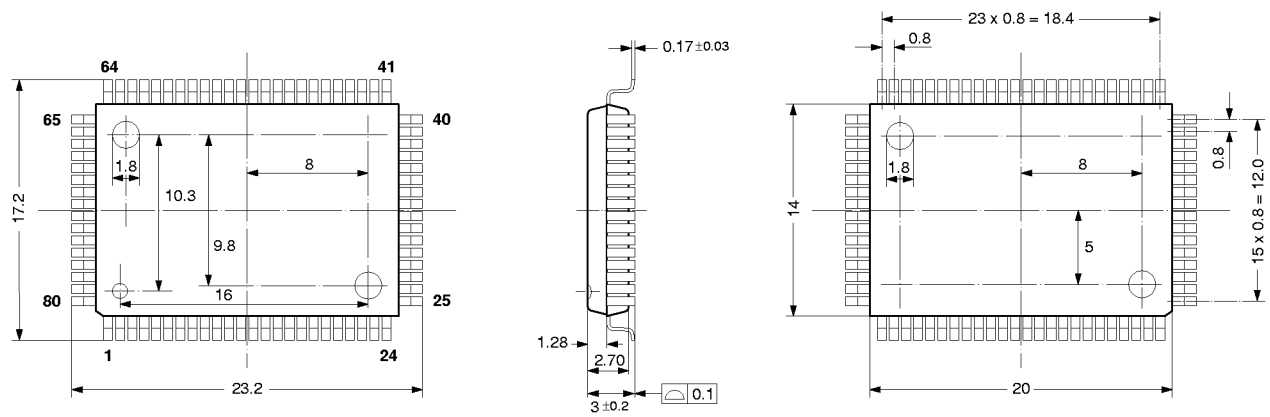


Fig. 4-2:
64-Pin Plastic Shrink Dual-Inline Package
(**PSDIP64**)
Weight approximately 9.0 g
Dimensions in mm

Fig. 4-3:
52-Pin Plastic Shrink Dual-Inline Package
(**PSDIP52**)
Weight approximately 5.5 g
Dimensions in mm



SPGS0025-1/1E

Fig. 4-4:
80-Pin Plastic Quad Flat Pack Package
(PQFP80)
Weight approximately 1.61 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant

LV = if not used, leave vacant

OBL = obligatory; connect as described in circuit diagram

DVSS: if not used, connect to DVSS

AHVSS: connect to AHVSS

Pin No.				Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin				
1	16	14	9	ADR_WS	OUT	LV	ADR word strobe
2	–	–	–	NC		LV	Not connected
3	15	13	8	ADR_DA	OUT	LV	ADR data output
4	14	12	7	I2S_DA_IN1	IN	LV	I ² S1 data input
5	13	11	6	I2S_DA_OUT	OUT	LV	I ² S data output
6	12	10	5	I2S_WS	IN/OUT	LV	I ² S word strobe
7	11	9	4	I2S_CL	IN/OUT	LV	I ² S clock
8	10	8	3	I2C_DA	IN/OUT	OBL	I ² C data
9	9	7	2	I2C_CL	IN/OUT	OBL	I ² C clock
10	8	–	1	NC		LV	Not connected
11	7	6	80	STANDBYQ	IN	OBL	Stand-by (low-active)
12	6	5	79	ADR_SEL	IN	OBL	I ² C Bus address select
13	5	4	78	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
14	4	3	77	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
15	3	–	76	NC		LV	Not connected
16	2	–	75	NC		LV	Not connected
17	–	–	–	NC		LV	Not connected
18	1	2	74	AUD_CL_OUT	OUT	LV	Audio clock output (18.432 MHz)
19	64	1	73	TP		LV	Test pin
20	63	52	72	XTAL_OUT	OUT	OBL	Crystal oscillator
21	62	51	71	XTAL_IN	IN	OBL	Crystal oscillator
22	61	50	70	TESTEN	IN	OBL	Test pin
23	60	49	69	ANA_IN2+	IN	LV	IF input 2 (if ANA_IN1+ is used only, connect to AVSS with 50 pF capacitor)
24	59	48	68	ANA_IN–	IN	LV	IF common

Pin No.				Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin				
25	58	47	67	ANA_IN1+	IN	LV	IF input 1
26	57	46	66	AVSUP		OBL	Analog power supply +5 V
–	–	–	65	AVSUP		OBL	Analog power supply +5 V
–	–	–	64	NC		LV	Not connected
–	–	–	63	NC		LV	Not connected
27	56	45	62	AVSS		OBL	Analog ground
–	–	–	61	AVSS		OBL	Analog ground
28	55	44	60	MONO_IN	IN	LV	Mono input
–	–	–	59	NC		LV	Not connected
29	54	43	58	VREFTOP		OBL	Reference voltage IF A/D converter
30	53	42	57	SC1_IN_R	IN	LV	SCART input 1 in, right
31	52	41	56	SC1_IN_L	IN	LV	SCART input 1 in, left
32	51	–	55	ASG1		AHVSS	Analog Shield Ground 1
33	50	40	54	SC2_IN_R	IN	LV	SCART input 2 in, right
34	49	39	53	SC2_IN_L	IN	LV	SCART input 2 in, left
35	48	–	52	ASG2		AHVSS	Analog Shield Ground 2
36	47	38	51	SC3_IN_R	IN	LV	SCART input 3 in, right
37	46	37	50	SC3_IN_L	IN	LV	SCART input 3 in, left
38	45	–	49	ASG4		AHVSS	Analog Shield Ground 4
39	44	–	48	SC4_IN_R	IN	LV	SCART input 4 in, right
40	43	–	47	SC4_IN_L	IN	LV	SCART input 4 in, left
41	–	–	46	NC		LV or AHVSS	Not connected
42	42	36	45	AGNDC		OBL	Analog reference voltage high voltage part
43	41	35	44	AHVSS		OBL	Analog ground
–	–	–	43	AHVSS		OBL	Analog ground
–	–	–	42	NC		LV	Not connected
–	–	–	41	NC		LV	Not connected
44	40	34	40	CAPL_M		OBL	Volume capacitor MAIN
45	39	33	39	AHVSUP		OBL	Analog power supply 8.0 V
46	38	32	38	CAPL_A		OBL	Volume capacitor AUX

Pin No.				Pin Name	Type	Connection (if not used)	Short Description
PLCC 68-pin	PSDIP 64-pin	PSDIP 52-pin	PQFP 80-pin				
47	37	31	37	SC1_OUT_L	OUT	LV	SCART output 1, left
48	36	30	36	SC1_OUT_R	OUT	LV	SCART output 1, right
49	35	29	35	VREF1		OBL	Reference ground 1 high voltage part
50	34	28	34	SC2_OUT_L	OUT	LV	SCART output 2, left
51	33	27	33	SC2_OUT_R	OUT	LV	SCART output 2, right
52	–	–	32	NC		LV	Not connected
53	32	–	31	NC		LV	Not connected
54	31	26	30	DACM_SUB	OUT	LV	Subwoofer output
55	30	–	29	NC		LV	Not connected
56	29	25	28	DACM_L	OUT	LV	Loudspeaker out, left
57	28	24	27	DACM_R	OUT	LV	Loudspeaker out, right
58	27	23	26	VREF2		OBL	Reference ground 2 high voltage part
59	26	22	25	DACA_L	OUT	LV	Headphone out, left
60	25	21	24	DACA_R	OUT	LV	Headphone out, right
–	–	–	23	NC		LV	Not connected
–	–	–	22	NC		LV	Not connected
61	24	20	21	RESETQ	IN	OBL	Power-on-reset
62	23	–	20	NC		LV	Not connected
63	22	–	19	NC		LV	Not connected
64	21	19	18	NC		LV	Not connected
65	20	18	17	I2S_DA_IN2	IN	LV	I ² S2-data input
66	19	17	16	DVSS		OBL	Digital ground
–	–	–	15	DVSS		OBL	Digital ground
–	–	–	14	DVSS		OBL	Digital ground
67	18	16	13	DVSUP		OBL	Digital power supply +5 V
–	–	–	12	DVSUP		OBL	Digital power supply +5 V
–	–	–	11	DVSUP		OBL	Digital power supply +5 V
68	17	15	10	ADR_CL	OUT	LV	ADR clock

¹⁾ Due to the compatibility with MSP 3410B, it is possible to connect with DVSS as well.

4.3. Pin Descriptions

Pin numbers refer to the 80-pin PQFP package

Pin 1, **NC** – Pin not connected.

Pin 2, **I2C_CL** – I²C Clock Input/Output (Fig. 4–10)
Via this pin, the I²C-bus clock signal has to be supplied. The signal can be pulled down by the MSP in case of wait conditions.

Pin 3, **I2C_DA** – I²C Data Input/Output (Fig. 4–10)
Via this pin, the I²C-bus data is written to or read from the MSP.

Pin 4, **I2S_CL** – I²S Clock Input/Output (Fig. 4–13)
Clock line for the I²S bus. In master mode, this line is driven by the MSP; in slave mode, an external I²S clock has to be supplied.

Pin 5, **I2S_WS** – I²S Word Strobe Input/Output (Fig. 4–13)
Word strobe line for the I²S bus. In master mode, this line is driven by the MSP; in slave mode, an external I²S word strobe has to be supplied.

Pin 6, **I2S_DA_OUT** – I²S Data Output (Fig. 4–9)
Output of digital serial sound data of the MSP on the I²S bus.

Pin 7, **I2S_DA_IN1** – I²S Data Input 1 (Fig. 4–11)
First input of digital serial sound data to the MSP via the I²S bus.

Pin 8, **ADR_DA** – ADR Bus Data Output (Fig. 4–9)
Output of digital serial data to the DRP 3510A via the ADR bus.

Pin 9, **ADR_WS** – ADR Bus Word Strobe Output (Fig. 4–9)
Word strobe output for the ADR bus.

Pin 10, **ADR_CL** – ADR Bus Clock Output (Fig. 4–9)
Clock line for the ADR bus.

Pins 11, 12, 13, **DVSUP*** – Digital Supply Voltage
Power supply for the digital circuitry of the MSP. Must be connected to a +5 V power supply.

Pins 14, 15, 16, **DVSS*** – Digital Ground
Ground connection for the digital circuitry of the MSP.

Pin 17, **I2S_DA_IN2** – I²S Data Input 2 (Fig. 4–11)
Second input of digital serial sound data to the MSP via the I²S bus.

Pins 18, 19, 20, **NC** – Pins not connected.

Pin 21, **RESETQ** – Reset Input (Fig. 4–11)
In the steady state, high level is required. A low level resets the MSP 34x0G.

Pins 22, 23, **NC** – Pins not connected.

Pins 24, 25, **DACA_R/L** – Headphone Outputs (Fig. 4–19)
Output of the headphone signal. A 1-nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected headphone volume.

Pin 26, **VREF2** – Reference Ground 2
Reference analog ground. This pin must be connected separately to the single ground point (AHVSS). VREF2 serves as a clean ground and should be used as the reference for analog connections to the loudspeaker and headphone outputs.

Pins 27, 28, **DACM_R/L** – Loudspeaker Outputs (Fig. 4–19)
Output of the loudspeaker signal. A 1-nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected loudspeaker volume.

Pin 29, **NC** – Pin not connected.

Pin 30, **DACM_SUB** – Subwoofer Output (Fig. 4–19)
Output of the subwoofer signal. A 1-nF capacitor to AHVSS must be connected to this pin. Due to the low frequency content of the subwoofer output, the value of the capacitor may be increased for better suppression of high-frequency noise. The DC offset on this pin depends on the selected loudspeaker volume.

■ Pins 31, 32 **NC** – Pin not connected.

Pins 33, 34, **SC2_OUT_R/L** – SCART2 Outputs (Fig. 4–21)
Output of the SCART2 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 35, **VREF1** – Reference Ground 1
Reference analog ground. This pin must be connected separately to the single ground point (AHVSS). VREF1 serves as a clean ground and should be used as the reference for analog connections to the SCART outputs.

Pins 36, 37, **SC1_OUT_R/L** – SCART1 Outputs (Fig. 4–21)
Output of the SCART1 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 38, **CAPLA** – Volume Capacitor Headphones (Fig. 4–16)
A 10-μF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for headphone volume changes in order to suppress audible plops.

The value of the capacitor can be lowered to 1- μ F if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pin 39, **AHVSUP*** – Analog Power Supply High Voltage

Power is supplied via this pin for the analog circuitry of the MSP (except IF input). This pin must be connected to the +8 V supply.

Pin 40, **CAPLM** – Volume Capacitor Loudspeakers (Fig. 4–16)

A 10- μ F capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for loudspeaker volume changes in order to suppress audible pops. The value of the capacitor can be lowered to 1 μ F if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pins 41, 42, **NC** – Pins not connected.

Pins 43, 44, **AHVSS*** – Analog Power Supply High Voltage

Ground connection for the analog circuitry of the MSP (except IF input).

Pin 45, **AGNDC** – Internal Analog Reference Voltage

This pin serves as the internal ground connection for the analog circuitry (except IF input). It must be connected to the VREF pins with a 3.3- μ F and a 100-nF capacitor in parallel. This pins shows a DC level of typically 3.73 V.

Pin 46, **NC** – Pin not connected.

Pins 47, 48, **SC4_IN_L/R** – SCART4 Inputs (Fig. 4–18)

The analog input signal for SCART4 is fed to this pin. Analog input connection must be AC-coupled.

Pin 49, **ASG4** – Analog Shield Ground 4

Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 50, 51, **SC3_IN_L/R** – SCART3 Inputs (Fig. 4–18)

The analog input signal for SCART3 is fed to this pin. Analog input connection must be AC-coupled.

Pin 52, **ASG2** – Analog Shield Ground 2

Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 53, 54 **SC2_IN_L/R** – SCART2 Inputs (Fig. 4–18)

The analog input signal for SCART2 is fed to this pin. Analog input connection must be AC-coupled.

Pin 55, **ASG1** – Analog Shield Ground 1

Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 56, 57 **SC1_IN_L/R** – SCART1 Inputs (Fig. 4–18)

The analog input signal for SCART1 is fed to this pin. Analog input connection must be AC-coupled.

Pin 58, **VREFTOP** – Reference Voltage IF A/D Converter (Fig. 4–15)

Via this pin, the reference voltage for the IF A/D converter is decoupled. It must be connected to AVSS pins with a 10- μ F and a 100-nF capacitor in parallel. Traces must be kept short.

Pin 59, **NC** – Pin not connected.

Pin 60 **MONO_IN** – Mono Input (Fig. 4–18)

The analog mono input signal is fed to this pin. Analog input connection must be AC-coupled.

Pins 61, 62, **AVSS*** – Analog Power Supply Voltage

Ground connection for the analog IF input circuitry of the MSP.

Pins 63, 64, **NC** – Pins not connected.

Pins 65, 66, **AVSUP*** – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the MSP. This pin must be connected to the +5 V supply.

Pin 67, **ANA_IN1+** – IF Input 1 (Fig. 4–15)

The analog sound IF signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN1+ is internally connected to one input of a symmetrical op amp, ANA_IN- to the other.

Pin 68, **ANA_IN-** – IF Common (Fig. 4–15)

This pins serves as a common reference for ANA_IN1/2+ inputs.

Pin 69, **ANA_IN2+** – IF Input 2 (Fig. 4–15)

The analog sound if signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN2+ is internally connected to one input of a symmetrical op amp, ANA_IN- to the other.

Pin 70, **TESTEN** – Test Enable Pin (Fig. 4–11)

This pin enables factory test modes. For normal operation, it must be connected to ground.

Pins 71, 72 **XTAL_IN, XTAL_OUT** – Crystal Input and Output Pins (Fig. 4–14)

These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. An external clock can be fed into XTAL_IN. The audio clock output signal AUD_CL_OUT is derived from the oscillator. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point.

Pin 73, **TP** – This pin enables factory test modes. For normal operation, it must be left vacant.

Pin 74, **AUD_CL_OUT** – Audio Clock Output (Fig. 4–14)

This is the 18.432 main clock output.

Pins 75, 76, **NC** – Pins not connected.

Pins 77, 78, **D_CTR_I/O_1/0** – Digital Control Input/Output Pins (Fig. 4–13)

These pins serve as general purpose input/output pins. Pin D_CTR_I/O_1 can be used as an interrupt request pin to the controller.

Pin 79, **ADR_SEL** – I²C Bus Address Select (Fig. 4–12)

By means of this pin, one of three device addresses for the MSP can be selected. The pin can be connected to ground (I²C device addresses 80/81_{hex}), to +5 V supply (84/85_{hex}), or left open (88/89_{hex}).

Pin 80, **STANDBYQ** – Stand-by

In normal operation, this pin must be High. If the MSP 34x0G is switched off by first pulling STANDBYQ low and then (after >1 μs delay) switching off the 5 V, but keeping the 8-V power supply (**'Stand-by'-mode**), the SCART switches maintain their position and function.

*** Application Note:**

All ground pins should be connected to one low-resistive ground plane. All supply pins should be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, and AHVSUP to AHVSS are recommended as closely as possible to these pins. Decoupling of DVSUP and DVSS is most important. We recommend using more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended. In our application boards we use: 220 pF, 470 pF, 1.5 nF, and 10 μF. The capacitor with the lowest value should be placed nearest to the DVSUP and DVSS pins.

4.4. Pin Configurations

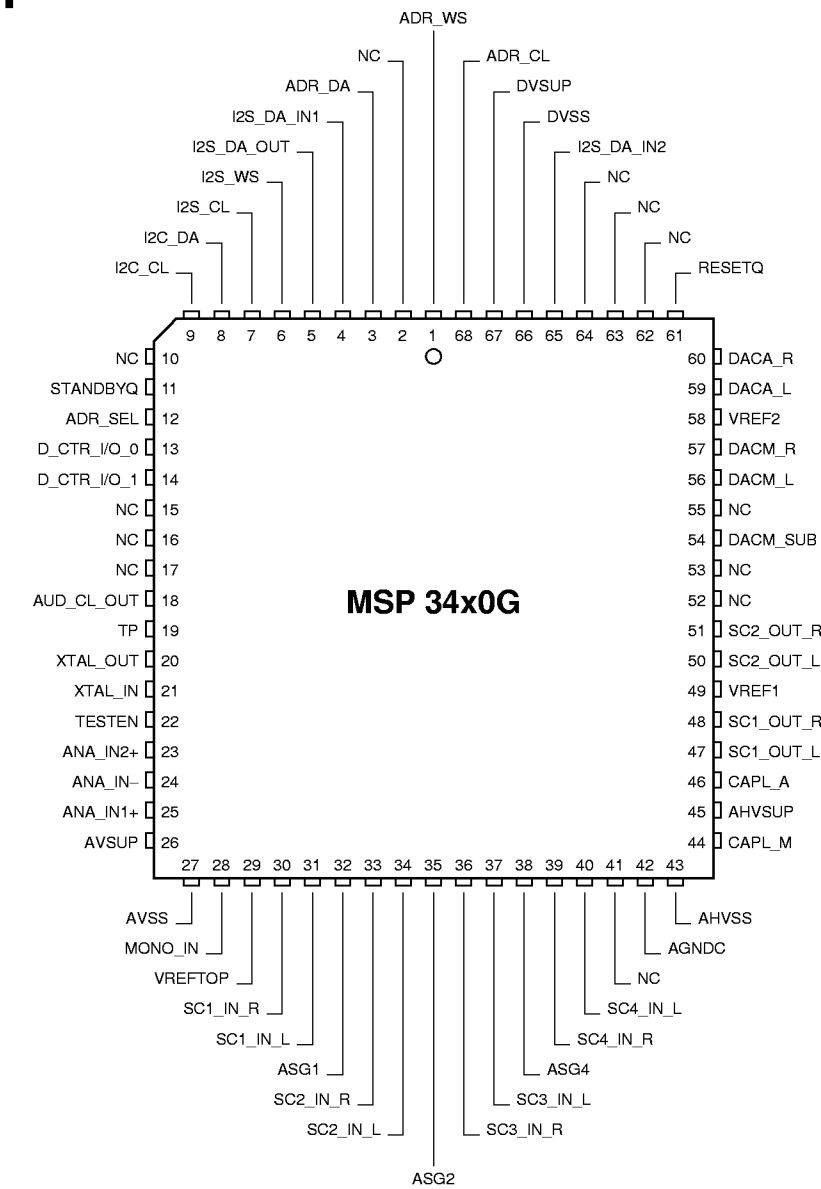


Fig. 4-5: 68-pin PLCC package

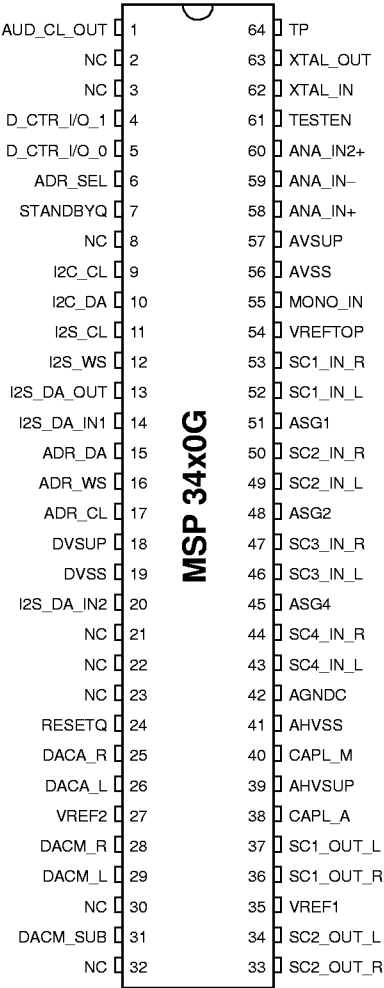


Fig. 4–6: 64-pin PSDIP package

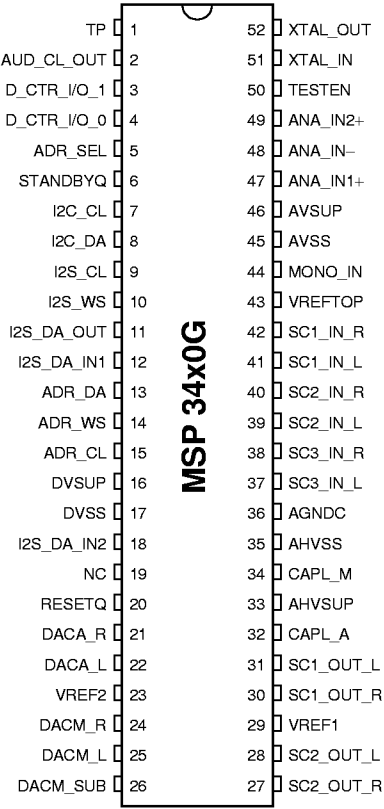


Fig. 4–7: 52-pin PSDIP package

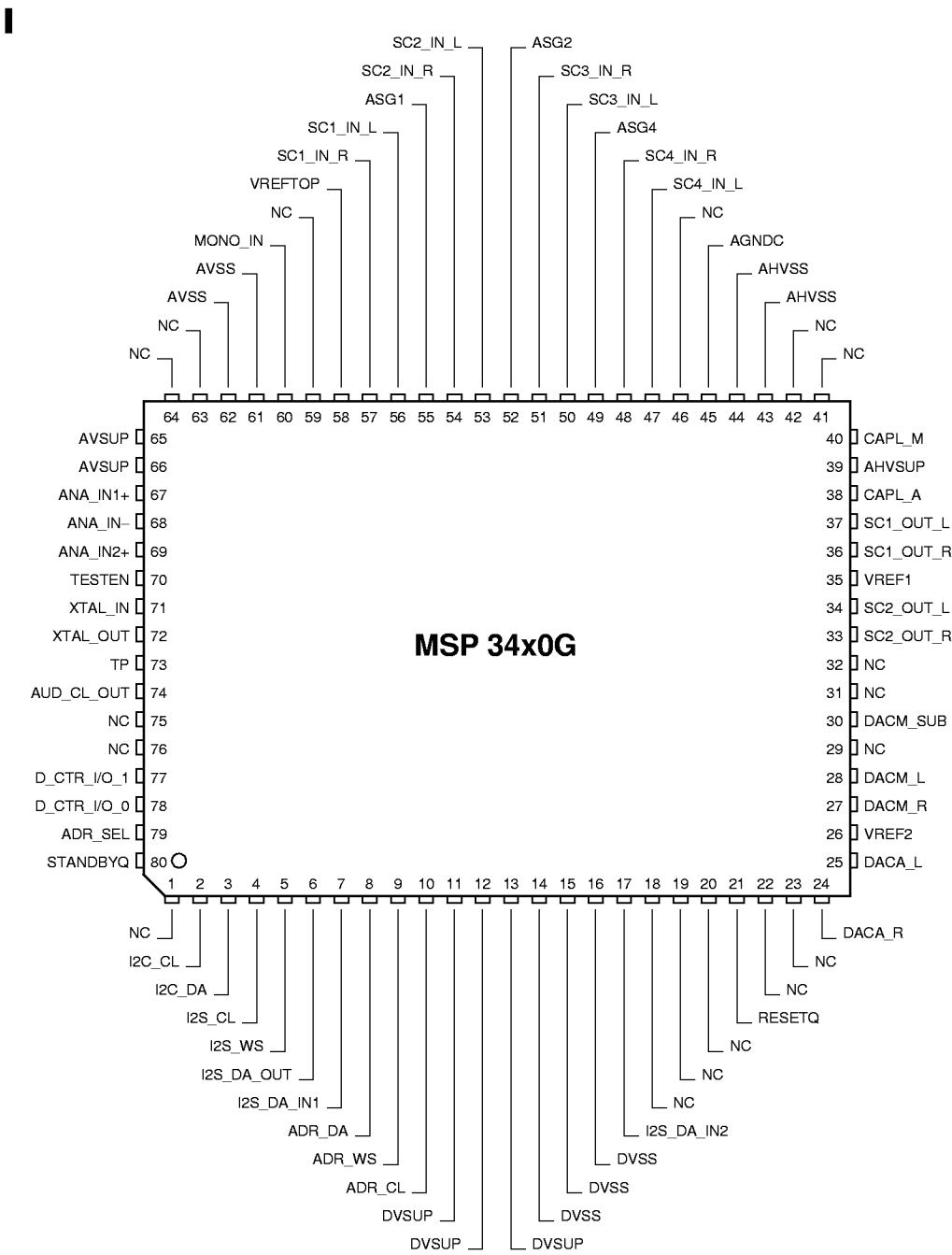


Fig. 4–8: 80-pin PQFP package

4.5. Pin Circuits

Pin numbers refer to the PQFP80 package.

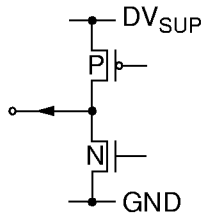


Fig. 4-9: Output Pins 6, 8, 9, and 10
(I2S_DA_OUT, ADR_DA, ADR_WS, ADR_CL)

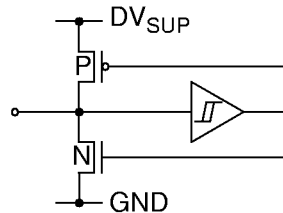


Fig. 4-13: Input/Output Pins 4, 5, 77, and 78
(I2S_CL, I2S_WS, D_CTR_I/O_1, D_CTR_I/O_0)

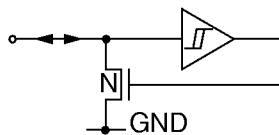


Fig. 4-10: Input/Output Pins 2 and 3
(I2C_CL, I2C_DA)

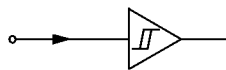


Fig. 4-11: Input Pins 7, 17, 21, 70, and 80
(I2S_DA_IN1, I2S_DA_IN2, RESETQ, TESTEN, STANDBYQ)

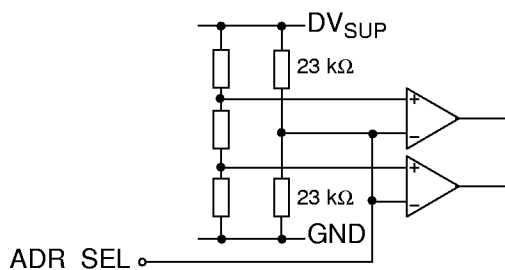


Fig. 4-12: Input Pin 79 (ADR_SEL)

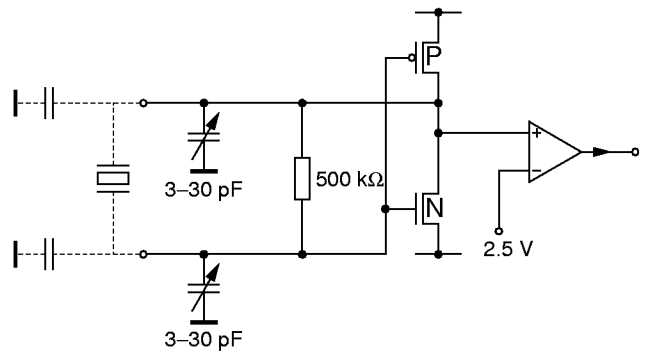


Fig. 4-14: Output/Input Pins 71, 72, and 74
(XTALIN, XTALOUT, AUD_CL_OUT)

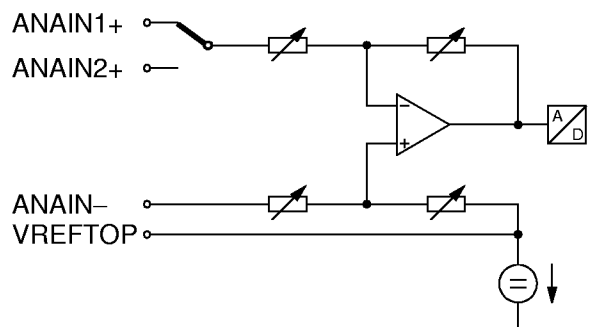


Fig. 4-15: Input Pins 58, 67, 68 and 69
(VREFTOP, ANA_IN1+, ANA_IN-, ANA_IN2+)

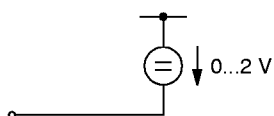


Fig. 4-16: Capacitor Pins 38 and 40 (CAPL_A, CAPL_M)

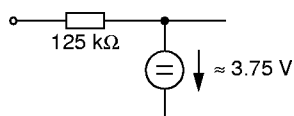


Fig. 4-20: Pin 45 (AGNDC)

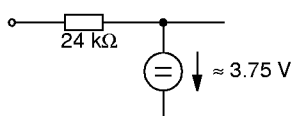


Fig. 4-17: Input Pin 60 (MONO_IN)

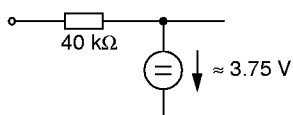


Fig. 4-18: Input Pins 47, 48, 50, 51, 53, 54, 56, and 57 (SC4-1_IN_L/R)

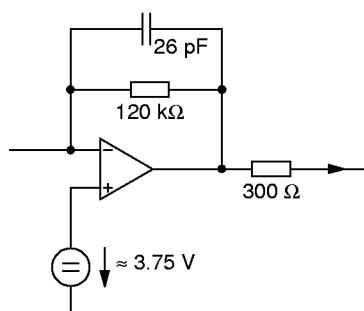


Fig. 4-21: Output Pins 33, 34, 36, and 37 (SC_2_OUT_R/L, SC_1_OUT_R/L)

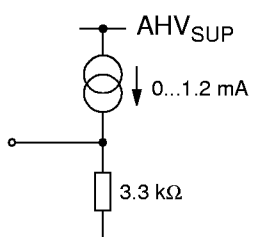


Fig. 4-19: Output Pins 24, 25, 27, 28 and 30 (DACA_R/L, DACM_R/L, DACM_SUB)

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	70	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP1}	First Supply Voltage	AHVSUP	–0.3	9.0	V
V_{SUP2}	Second Supply Voltage	DVSUP	–0.3	6.0	V
V_{SUP3}	Third Supply Voltage	AVSUP	–0.3	6.0	V
dV_{SUP23}	Voltage between AVSUP and DVSUP	AVSUP, DVSUP	–0.5	0.5	V
P_{TOT}	Power Dissipation PLCC68 PSDIP64 PSDIP52	AHVSUP, DVSUP, AVSUP		1200 1300 1200	mW mW mW
V_{Idig}	Input Voltage, all Digital Inputs		–0.3	$V_{SUP2}+0.3$	V
I_{Idig}	Input Current, all Digital Pins	–	–20	+20	mA ¹⁾
V_{Iana}	Input Voltage, all Analog Inputs	SCn_IN_s, ²⁾ MONO_IN	–0.3	$V_{SUP1}+0.3$	V
I_{Iana}	Input Current, all Analog Inputs	SCn_IN_s, ²⁾ MONO_IN	–5	+5	mA ¹⁾
I_{Oana}	Output Current, all SCART Outputs	SCn_OUT_s ²⁾	3), 4)	3), 4)	
I_{Oana}	Output Current, all Analog Outputs except SCART Outputs	DACp_s ²⁾	3)	3)	
I_{Cana}	Output Current, other pins connected to capacitors	CAPL_p, ²⁾ AGNDC	3)	3)	
¹⁾ positive value means current flowing into the circuit ²⁾ “n” means “1”, “2”, “3”, or “4”, “s” means “L” or “R”, “p” means “M” or “A” ³⁾ The Analog Outputs are short-circuit proof with respect to First Supply Voltage and Ground. ⁴⁾ Total chip power dissipation must not exceed absolute maximum rating.					

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions ($T_A = 0$ to $70\text{ }^{\circ}\text{C}$)**4.6.2.1. General Recommended Operating Conditions**

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP1}	First Supply Voltage (8-V Operation)	AHVSUP	7.6	8.0	8.4	V
	First Supply Voltage (5-V Operation)		4.75	5.0	5.25	V
V_{SUP2}	Second Supply Voltage	DVSUP	4.75	5.0	5.25	V
V_{SUP3}	Third Supply Voltage	AVSUP	4.75	5.0	5.25	V
t_{STBYQ1}	STANDBYQ Setup Time before Turn-off of Second Supply Voltage	STANDBYQ, DVSUP	1			μs

4.6.2.2. Analog Input and Output Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
C_{AGNDC}	AGNDC-Filter-Capacitor	AGNDC	-20%	3.3		μF
	Ceramic Capacitor in Parallel		-20%	100		nF
C_{inSC}	DC-Decoupling Capacitor in front of SCART Inputs	$\text{SCn_IN_s}^{1)}$	-20%	330		nF
V_{inSC}	SCART Input Level				2.0	V_{RMS}
V_{inMONO}	Input Level, Mono Input	MONO_IN			2.0	V_{RMS}
R_{LSC}	SCART Load Resistance	$\text{SCn_OUT_s}^{1)}$	10			k Ω
C_{LSC}	SCART Load Capacitance				6.0	nF
C_{VMA}	Main/AUX Volume Capacitor	CAPL_M, CAPL_A		10		μF
C_{FMA}	Main/AUX Filter Capacitor	DACM_s, DACA_s ¹⁾	-10%	1	+10%	nF

¹⁾ "n" means "1", "2", or "3", "s" means "L" or "R", "p" means "M" or "A"

4.6.2.3. Recommendations for Analog Sound IF Input Signal

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
C _{VREFTOP}	VREFTOP-Filter-Capacitor	VREFTOP	–20 %	10		μF
	Ceramic Capacitor in Parallel		–20 %	100		nF
F _{IF_FMTV}	Analog Input Frequency Range for TV Applications	ANA_IN1+, ANA_IN2+, ANA_IN–	0		9	MHz
F _{IF_FMRADIO}	Analog Input Frequency for FM-Radio Applications			10.7		MHz
V _{IF_FM}	Analog Input Range FM/NICAM		0.1	0.8	3	V _{pp}
V _{IF_AM}	Analog Input Range AM/NICAM		0.1	0.45	0.8	V _{pp}
R _{FMNI}	Ratio: NICAM Carrier/FM Carrier (unmodulated carriers) BG: I:		–20 –23	–7 –10	0 0	dB dB
R _{AMNI}	Ratio: NICAM Carrier/AM Carrier (unmodulated carriers)		–25	–11	0	dB
R _{FM}	Ratio: FM-Main/FM-Sub Satellite			7		dB
R _{FM1/FM2}	Ratio: FM1/FM2 German FM-System			7		dB
R _{FC}	Ratio: Main FM Carrier/ Color Carrier		15	–	–	dB
R _{FV}	Ratio: Main FM Carrier/ Luma Components		15	–	–	dB
PR _{IF}	Passband Ripple		–	–	±2	dB
SUP _{HF}	Suppression of Spectrum above 9.0 MHz (not for FM Radio)		15		–	dB
FM _{MAX}	Maximum FM-Deviation (approx.) normal mode HDEV2: high deviation mode HDEV3: very high deviation mode				±180 ±360 ±540	kHz kHz kHz

4.6.2.4. Crystal Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Crystal Recommendations for Master-Slave Application						
General Recommendations						
f _P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f _{TOL}	Accuracy of Adjustment		−20		+20	ppm
D _{TEM}	Frequency Variation versus Temperature		−20		+20	ppm
R _R	Series Resistance			8	25	Ω
C ₀	Shunt (Parallel) Capacitance			6.2	7.0	pF
C ₁	Motional (Dynamic) Capacitance		19	24		fF
Load Capacitance Recommendations						
C _L	External Load Capacitance ¹⁾	XTAL_IN, XTAL_OUT	PSDIP PLCC PQFP	1.5 3.3 to be defined		pF pF pF
f _{CL}	Required Open Loop Clock Frequency (T _{amb} = 25 °C)		18.431		18.433	MHz
Crystal Recommendations for FM / NICAM Applications (No Master-Slave Mode possible)						
General Recommendations						
f _P	Parallel Resonance Frequency at 12 pF Load Capacitance			18.432		MHz
f _{TOL}	Accuracy of Adjustment		−30		+30	ppm
D _{TEM}	Frequency Variation versus Temperature		−30		+30	ppm
R _R	Series Resistance			8	25	Ω
C ₀	Shunt (Parallel) Capacitance			6.2	7.0	pF
C ₁	Motional (Dynamic) Capacitance		15			fF
Load Capacitance Recommendations						
C _L	External Load Capacitance ¹⁾	XTAL_IN, XTAL_OUT	PSDIP PLCC PQFP	1.5 3.3 to be defined		pF pF pF
f _{CL}	Required Open Loop Clock Frequency (T _{amb} = 25 °C)		18.4305		18.4335	MHz
¹⁾ External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation. The higher the capacitors, the lower the resulting clock frequency. The nominal free running frequency should match 18.432 MHz as closely as possible. Due to different layouts of customer PCBs, the matching capacitor size should be defined in the application. The suggested values (1.5 pF/3.3 pF) are figures based on experience with various PCB layouts.						

[illegible]

4.6.3. Characteristics

at $T_A = 0$ to $70\text{ }^{\circ}\text{C}$, $f_{\text{CLOCK}} = 18.432\text{ MHz}$, $V_{\text{SUP1}} = 7.6$ to 8.4 V , $V_{\text{SUP2}} = 4.75$ to 5.25 V for min./max. values
 at $T_A = 60\text{ }^{\circ}\text{C}$, $f_{\text{CLOCK}} = 18.432\text{ MHz}$, $V_{\text{SUP1}} = 8\text{ V}$, $V_{\text{SUP2}} = 5\text{ V}$ for typical values,
 T_J = Junction Temperature
 MAIN (M) = Loudspeaker Channel, AUX (A) = Headphone Channel

4.6.3.1. General Characteristics

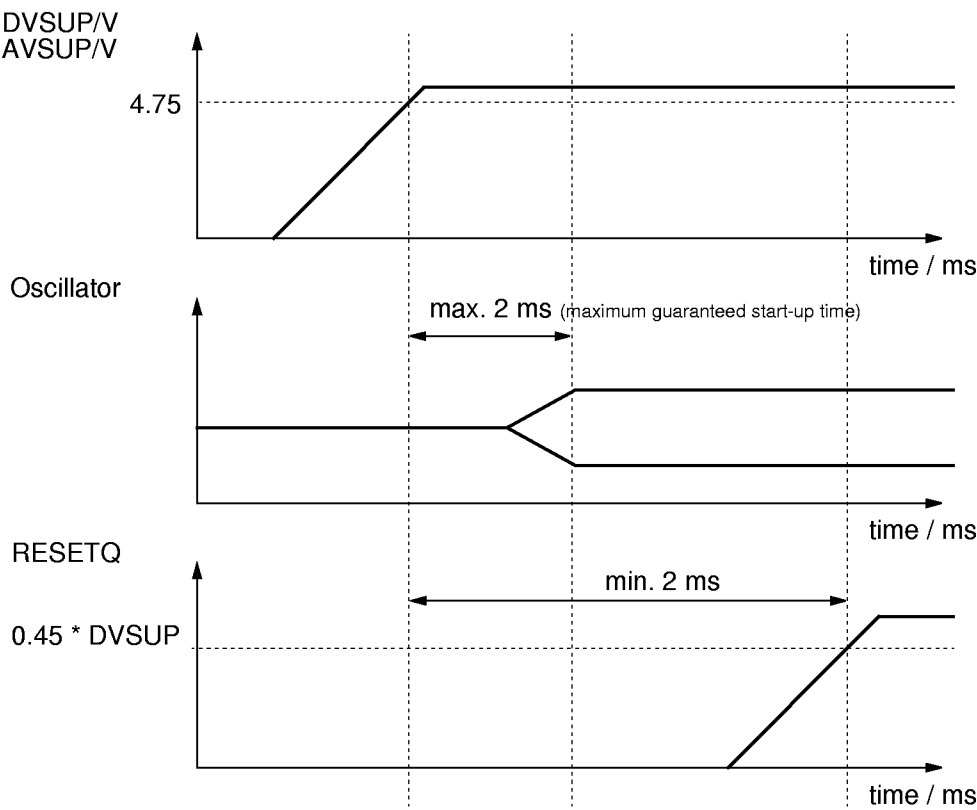
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply							
I _{SUP1A}	First Supply Current (active) (8-V Operation) Analog Volume for Main and Aux at 0 dB Analog Volume for Main and Aux at –30 dB	AHVSUP	9.6 6.3	17.1 11.2	24.6 16.1	mA mA	
	First Supply Current (active) (5-V Operation) Analog Volume for Main and Aux at 0 dB Analog Volume for Main and Aux at –30 dB		6.4 4.2	11.4 7.5	16.4 10.7	mA mA	
I _{SUP2A}	Second Supply Current (active)	DVSUP	86	95	102	mA	
I _{SUP3A}	Third Supply Current (active)	AVSUP	15	25	35	mA	
I _{SUP1S}	First Supply Current (8-V Operation) (standby mode) at T _j = 27 °C	AHVSUP	3.5	5.6	7.7	mA	STANDBYQ = low
	First Supply Current (5-V Operation) (standby mode) at T _j = 27 °C		2.3	3.7	5.1	mA	STANDBYQ = low
Clock							
f _{CLOCK}	Clock Input Frequency	XTAL_IN		18.432		MHz	
D _{CLOCK}	Clock High to Low Ratio		45		55	%	
t _{JITTER}	Clock Jitter (Verification not provided in Production Test)				50	ps	
V _{xtalDC}	DC-Voltage Oscillator			2.5		V	
t _{Startup}	Oscillator Startup Time at VDD Slew-rate of 1 V/1 μs	XTAL_IN, XTAL_OUT		0.4	2	ms	
V _{ACLKAC}	Audio Clock Output AC Voltage	AUD_CL_OUT	1.2	1.8		V _{pp}	load = 40 pF
V _{ACLKDC}	Audio Clock Output DC Voltage		0.4		0.6	V _{SUP3}	I _{max} = 0.2 mA
r _{outHF_ACL}	HF Output Resistance			140		W	

4.6.3.2. Digital Inputs, Digital Outputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Inputs Levels							
V _{DIGIL}	Digital Input Low Voltage	STANDBYQ, ADR_SEL, TESTEN			0.2	V _{SUP2}	
V _{DIGIH}	Digital Input High Voltage		0.8			V _{SUP2}	
Z _{DIGI}	Input Impedance				5	pF	
I _{DLEAK}	Digital Input Leakage Current	STANDBYQ, TESTEN	−1		1	μA	0 V < U _{INPUT} < DVSUP
I _{ADRSEL}	Input Current Address Select Pin	ADR_SEL	−500	−220		μA	U _{ADR_SEL} = DVSS
				220	500	μA	U _{ADR_SEL} = DVSUP
V _{DIGILDCTR}	Digital Control Input Low Voltage	D_CTR_I/O_0 D_CTR_I/O_1			0.2	V _{SUP2}	D_CTR_I/O_0/1 : tri-state
V _{DIGIHDCTR}	Digital Control Input High Voltage		0.8			V _{SUP2}	
Z _{DIGIDCTR}	Input Impedance Digital Control Input				5	pF	
I _{DLEAKDCTR}	Digital Control Input Pins Leakage Current		-1		1	μA	0 V < U _{INPUT} < DVSUP D_CTR_I/O_0/1 : tri-state
Digital Output Levels							
V _{DCTRL}	Digital Output Low Voltage	D_CTR_I/O_0 D_CTR_I/O_1			0.4	V	IDDCTR = 1 mA
V _{DCTROH}	Digital Output High Voltage		4.0			V	IDDCTR = −1 mA

4.6.3.3. Reset Input and Power-Up

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
RESETQ Input Levels							
V_{REIL}	Reset Input High-Low and Low-High Transition Voltage	RESETQ	0.45		0.8	V_{SUP2}	
Z_{RES}	Input Impedance Reset Input				5	pF	
I_{RES}	Reset Input Pin Leakage Current		-1		1	μA	$0\text{ V} < U_{INPUT} < DVSUP$

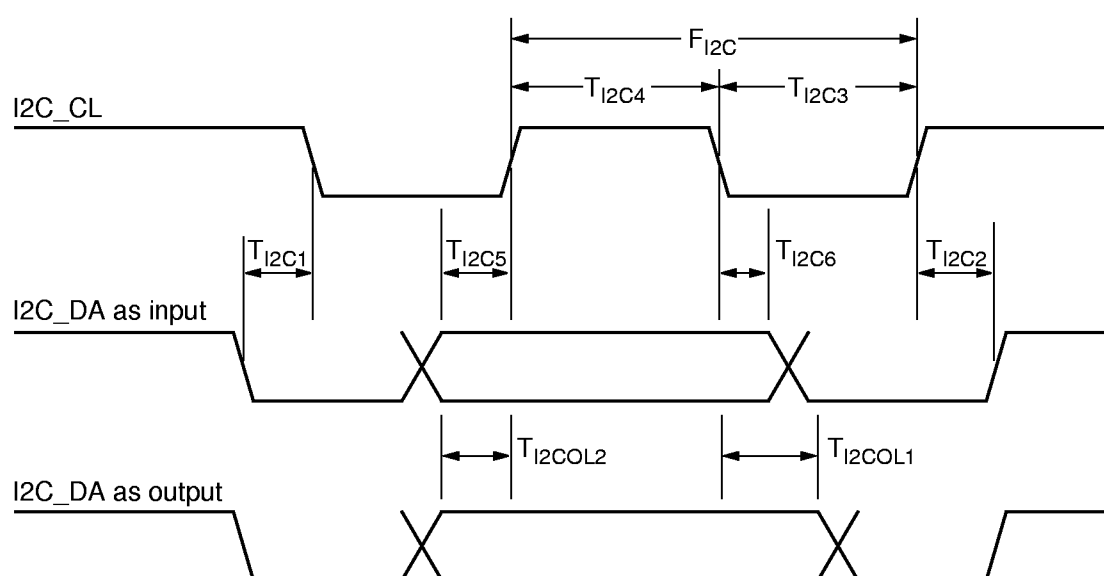


Note: The reset should stay at low level as long as the oscillator has not yet started. This requires a reset delay of >2 ms

Fig. 4-22: Power-up sequence

4.6.3.4. I²C-Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V _{I2CIL}	I ² C-BUS Input Low Voltage	I2C_CL, I2C_DA	0.6		0.3	V _{SUP2}	
V _{I2CIH}	I ² C-BUS Input High Voltage					V _{SUP2}	
f _{I2C}	I ² C-BUS Frequency	I2C_CL			1.0	MHz	
t _{I2C1}	I ² C START Condition Setup Time	I2C_CL, I2C_DA	120			ns	
t _{I2C2}	I ² C STOP Condition Setup Time		120			ns	
t _{I2C3}	I ² C-Clock Low Pulse Time	I2C_CL	500			ns	
t _{I2C4}	I ² C-Clock High Pulse Time		500			ns	
t _{I2C5}	I ² C-Data Setup Time before Rising Edge of Clock	I2C_CL, I2C_DA	55			ns	
t _{I2C6}	I ² C-Data Hold Time after Falling Edge of Clock		55			ns	
V _{I2COL}	I ² C-Data Output Low Voltage	I2C_CL, I2C_DA			0.4	V	I _{I2COL} = 3 mA
I _{I2COH}	I ² C-Data Output High Leakage Current				1.0	μA	V _{I2COH} = 5 V
t _{I2COL1}	I ² C-Data Output Hold Time after Falling Edge of Clock	I2C_DA, I2C_CL	15			ns	
t _{I2COL2}	I ² C-Data Output Setup Time before Rising Edge of Clock		100			ns	f _{I2C} = 1 MHz

Fig. 4-23: I²C bus timing diagram

4.6.3.5. I²S-Bus Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V _{I2SIL}	I ² S-Data Input Low Voltage	I2S_DA_IN1/2			0.25	V _{SUP2}	
V _{I2SIH}	I ² S-Data Input High Voltage		0.75			V _{SUP2}	
Z _{I2SI}	Input Impedance				5	pF	
I _{DLEAKI2SI}	Digital Input Leakage Current		−1		1	μA	0 V < U _{INPUT} < DVSUP
t _{I2S1}	I ² S-Data Input Setup Time before Rising Edge of Clock	I2S_DA_IN1/2, I2S_CL	20			ns	
t _{I2S2}	I ² S-Data Input Hold Time after Falling Edge of Clock		0			ns	
V _{I2SIDL}	I ² S-Input Low Voltage when MSP in I ² S-Slave-Mode	I2S_CL, I2S_WS			0.25	V _{SUP2}	
V _{I2SIDH}	I ² S-Input High Voltage when MSP in I ² S-Slave-Mode		0.75			V _{SUP2}	
f _{I2SCL}	I ² S-Clock Input Frequency when MSP in I ² S-Slave-Mode	I2S_CL		1.024		MHz	
R _{I2SCL}	I ² S-Clock Input Ratio when MSP in I ² S-Slave-Mode		0.9		1.1		
f _{I2SWS}	I ² S-Word Strobe Input Frequency when MSP in I ² S-Slave Mode	I2S_WS		32.0		kHz	
t _{I2SWS1}	I ² S-Word Strobe Input Setup Time before Rising Edge of Clock when MSP in I ² S-Slave-Mode	I2S_WS, I2S_CL	60			ns	
t _{I2SWS2}	I ² S-Word Strobe Input Hold Time after Falling Edge of Clock when MSP in I ² S-Slave-Mode		0			ns	
I _{DLEAKI2S}	Digital Input Leakage Current		−1		1	μA	0 V < U _{INPUT} < DVSUP I ² S slave mode
V _{I2SOL}	I ² S Output Low Voltage	I2S_WS, I2S_CL, I2S_DA_OUT			0.4	V	I _{I2SOL} = 1 mA
V _{I2SOH}	I ² S Output High Voltage		4.0			V	I _{I2SOH} = −1 mA
f _{I2SCL}	I ² S-Clock Output Frequency	I2S_CL		1024		kHz	NICAM-PLL closed
f _{I2SWS}	I ² S-Word Strobe Output Frequency	I2S_WS		32.0		kHz	NICAM-PLL closed
t _{I2S1/I2S2}	I ² S-Clock High/Low-Ratio	I2S_CL	0.9	1.0	1.1		
t _{I2S3}	I ² S-Data Setup Time before Rising Edge of Clock	I2S_CL, I2S_DA_OUT	200			ns	C _L = 30 pF
t _{I2S4}	I ² S-Data Hold Time after Falling Edge of Clock				180	ns	C _L = 30 pF
t _{I2S5}	I ² S-Word Strobe Setup Time before Rising Edge of Clock	I2S_CL, I2S_WS	200			ns	C _L = 30 pF
t _{I2S6}	I ² S-Word Strobe Hold Time after Falling Edge of Clock				180	ns	C _L = 30 pF

The diagram illustrates the timing relationship between the I2S interface signals: $I2S_WS$, $I2S_CL$, $I2S_DAIN$, and $I2S_DAOUT$.

Top Section: Shows the overall timing. $I2S_WS$ is a periodic signal with frequency F_{I2SWS} . $I2S_CL$ is a clock signal. $I2S_DAIN$ and $I2S_DAOUT$ are data signals, each consisting of a 16-bit left channel and a 16-bit right channel. The data signals are labeled with $R\ LSB$, $L\ MSB$, $L\ LSB$, and $R\ MSB$. The mode is programmable by $MODUS[6]$, with PHILIPS Mode and SONY Mode indicated.

Detail A: Shows the relationship between $I2S_WS$ and $I2S_CL$. The timing parameters T_{I2SWS1} and T_{I2SWS2} are indicated.

Detail B: Shows the relationship between $I2S_WS$ and $I2S_DAIN$. The timing parameters T_{I2S5} and T_{I2S6} are indicated.

Detail C: Shows the relationship between $I2S_WS$ and $I2S_DAOUT$. The timing parameters T_{I2S1} , T_{I2S2} , T_{I2S3} , and T_{I2S4} are indicated.

Fig. 4–24: I²S bus timing diagram

4.6.3.6. Analog Baseband Inputs and Outputs, AGNDC

[illegible]

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Audio Analog-to-Digital-Converter							
V _{AI} CL	Effective Analog Input Clipping Level for Analog-to-Digital-Conversion (8-V Operation)	SCn_IN_s, ¹⁾ MONO_IN	2.00		2.25	V _{RMS}	f _{signal} = 1 kHz
	Effective Analog Input Clipping Level for Analog-to-Digital-Conversion (5-V Operation)		1.13		1.51	V _{RMS}	
SCART Outputs							
R _{outSC}	SCART Output Resistance at T _j = 27 °C from T _A = 0 to 70 °C	SCn_OUT_s ¹⁾	200 200	330	460 500	Ω Ω	f _{signal} = 1 kHz, I = 0.1 mA
dV _{OUTSC}	Deviation of DC-Level at SCART Output from AGND C Voltage		−70		+70	mV	
A _{SCtoSC}	Gain from Analog Input to SCART Output	SCn_IN_s, ¹⁾ MONO_IN → SCn_OUT_s ¹⁾	−1.0		+0.5	dB	f _{signal} = 1 kHz
f _{rSCtoSC}	Frequency Response from Analog Input to SCART Output Bandwidth: 0 to 20000 Hz		−0.5		+0.5	dB	with resp. to 1 kHz
V _{outSC}	Effective Signal Level at SCART-Output during full-scale Digital Input Signal from DSP (8-V Operation)	SCn_OUT_s ¹⁾	1.8	1.9	2.0	V _{RMS}	f _{signal} = 1 kHz
	Effective Signal Level at SCART-Output during full-scale Digital Input Signal from DSP (5-V Operation)		1.17	1.27	1.37	V _{RMS}	
Main and AUX Outputs							
R _{outMA}	Main/AUX Output Resistance at T _j = 27 °C from T _A = 0 to 70 °C	DACp_s ¹⁾	2.1 2.1	3.3	4.6 5.0	kΩ kΩ	f _{signal} = 1 kHz, I = 0.1 mA
V _{outDCMA}	DC-Level at Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at −30 dB (8-V Operation)		1.80	2.04 61	2.28	V mV	
	DC-Level at Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at −30 dB (5-V Operation)		1.12	1.36 40	1.60	V mV	
V _{outMA}	Effective Signal Level at Main/AUX-Output during full-scale Digital Input Signal from DSP for Analog Volume at 0 dB (8-V Operation)		1.23	1.37	1.51	V _{RMS}	f _{signal} = 1 kHz
	Effective Signal Level at Main/AUX-Output during full-scale Digital Input Signal from DSP for Analog Volume at 0 dB (5-V Operation)		0.76	0.90	1.04	V _{RMS}	
1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”							

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R _{IFIN}	Input Impedance	ANA_IN1+, ANA_IN2+, ANA_IN–	1.5 6.8	2 9.1	2.5 11.4	kΩ kΩ	Gain AGC = 20 dB Gain AGC = 3 dB
DC _{VREFTOP}	DC Voltage at VREFTOP	VREFTOP	2.4	2.6	2.7	V	
DC _{ANA_IN}	DC Voltage on IF Inputs	ANA_IN1+, ANA_IN2+, ANA_IN–	1.3	1.5	1.7	V	
XTALK _{KIF}	Crosstalk Attenuation	ANA_IN1+, ANA_IN2+, ANA_IN–	40			dB	f _{signal} = 1 MHz Input Level = –2 dBr
BW _{IF}	3 dB Bandwidth		10			MHz	
AGC	AGC Step Width			0.85		dB	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
PSRR: Rejection of Noise on AHVSUP at 1 kHz							
PSRR	AGNDc	AGNDc		80		dB	
	From Analog Input to DSP	MONO_IN, SCn_IN_s ¹⁾)		70		dB	
	From Analog Input to SCART Output	MONO_IN, SCn_IN_s ¹⁾ , SCn_OUT_s ¹⁾)		70		dB	
	From DSP to SCART Output	SCn_OUT_s ¹⁾)		60		dB	
	From DSP to MAIN/AUX Output	DACp_s ¹⁾)		80		dB	

¹⁾ “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

4.6.3.9. Analog Performance

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Specifications for 8-V Operation							
SNR	Signal-to-Noise Ratio						
	from Analog Input to DSP	MONO_IN, SCn_IN_s ¹⁾	85	88		dB	Input Level = −20 dB with resp. to V _{AICL} , f _{sig} = 1 kHz, equally weighted 20 Hz... 16 kHz ²⁾
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s ¹⁾ → SCn_OUT_s ¹⁾	93	96		dB	Input Level = −20 dB, f _{sig} = 1 kHz, equally weighted 20 Hz... 20 kHz
	from DSP to SCART Output	SCn_OUT_s ¹⁾	85	88		dB	Input Level = −20 dB, f _{sig} = 1 kHz, equally weighted 20 Hz... 15 kHz ³⁾
	from DSP to Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at −30 dB	DACp_s ¹⁾	85 78	88 83		dB dB	Input Level = −20 dB, f _{sig} = 1 kHz, equally weighted 20 Hz... 15 kHz ³⁾
THD	Total Harmonic Distortion						
	from Analog Input to DSP	MONO_IN, SCn_IN_s ¹⁾		0.01	0.03	%	Input Level = −3 dBr with resp. to V _{AICL} , f _{sig} = 1 kHz, equally weighted 20 Hz... 16 kHz ²⁾
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s ¹⁾		0.01	0.03	%	Input Level = −3 dBr, f _{sig} = 1 kHz, equally weighted 20 Hz... 20 kHz
	from DSP to SCART Output	SCn_OUT_s ¹⁾		0.01	0.03	%	Input Level = −3 dBr, f _{sig} = 1 kHz, equally weighted 20 Hz... 16 kHz ³⁾
	from DSP to Main or AUX Output	DACA_s, DACM_s ¹⁾		0.01	0.03	%	Input Level = −3 dBr, f _{sig} = 1 kHz, equally weighted 20 Hz... 16 kHz ³⁾

¹⁾ “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

²⁾ DSP measured at I²S-Output

³⁾ DSP Input at I²S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Specifications for 5-V Operation							
SNR	Signal-to-Noise Ratio						
	from Analog Input to DSP	MONO_IN, SCn_IN_s ¹⁾	82	85		dB	Input Level = −20 dB with resp. to V _{AICL} , f _{sig} = 1 kHz, equally weighted 20 Hz... 16 kHz ²⁾
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s ¹⁾ → SCn_OUT_s ¹⁾	90	93		dB	Input Level = −20 dB, f _{sig} = 1 kHz, equally weighted 20 Hz... 20 kHz
	from DSP to SCART Output	SCn_OUT_s ¹⁾	82	85		dB	Input Level = −20 dB, f _{sig} = 1 kHz, equally weighted 20 Hz... 15 kHz ³⁾
	from DSP to Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at −30 dB	DACp_s ¹⁾	82 75	85 80		dB dB	Input Level = −20 dB, f _{sig} = 1 kHz, equally weighted 20 Hz... 15 kHz ³⁾
THD	Total Harmonic Distortion						
	from Analog Input to DSP	MONO_IN, SCn_IN_s ¹⁾		0.03	0.1	%	Input Level = −3 dBr with resp. to V _{AICL} , f _{sig} = 1 kHz, equally weighted 20 Hz... 16 kHz ²⁾
	from Analog Input to SCART Output	MONO_IN, SCn_IN_s → SCn_OUT_s ¹⁾			0.1	%	Input Level = −3 dBr, f _{sig} = 1 kHz, equally weighted 20 Hz... 20 kHz
	from DSP to SCART Output	SCn_OUT_s ¹⁾			0.1	%	Input Level = −3 dBr, f _{sig} = 1 kHz, equally weighted 20 Hz... 16 kHz ³⁾
	from DSP to Main or AUX Output	DACA_s, DACM_s ¹⁾			0.1	%	Input Level = −3 dBr, f _{sig} = 1 kHz, equally weighted 20 Hz... 16 kHz ³⁾

1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

2) DSP measured at I²S-Output

3) DSP Input at I²S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
XTALK Specifications for 8-V and 5-V Operation							
XTALK	Crosstalk Attenuation – PLCC68 – PSDIP64						Input Level = –3 dB, f _{sig} = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ
	between left and right channel within SCART Input/Output pair (L→R, R→L) SCn_IN → SCn_OUT ¹⁾						equally weighted 20 Hz...20 kHz
		PLCC68	80			dB	
		PSDIP64	80			dB	
	SC1_IN or SC2_IN → DSP ¹⁾	PLCC68	80			dB	2)
		PSDIP64	80			dB	
	SC3_IN → DSP ¹⁾	PLCC68	80			dB	
		PSDIP64	80			dB	
	DSP → SCn_OUT ¹⁾	PLCC68	80			dB	3)
		PSDIP64	80			dB	
	between left and right channel within Main or AUX Output pair DSP → DACp ¹⁾						equally weighted 20 Hz...16 kHz
		PLCC68	80			dB	3)
		PSDIP64	75			dB	
	between SCART Input/Output pairs ¹⁾ D = disturbing program O = observed program D: MONO/SCn_IN → SCn_OUT O: MONO/SCn_IN → SCn_OUT ¹⁾						(equally weighted 20 Hz...20 kHz same signal source on left and right disturbing channel, effect on each observed output channel
		PLCC68	100			dB	2)
		PSDIP64	100			dB	
	D: MONO/SCn_IN → SCn_OUT or unsel.	PLCC68	100			dB	
	O: MONO/SCn_IN → DSP ¹⁾	PSDIP64	95			dB	3)
	D: MONO/SCn_IN → SCn_OUT	PLCC68	100			dB	
	O: DSP → SCn_OUT ¹⁾	PSDIP64	100			dB	
	D: MONO/SCn_IN → unselected O: DSP → SC1_OUT ¹⁾	PLCC68	100			dB	3)
		PSDIP64	100			dB	
	Crosstalk between Main and AUX Output pairs DSP → DACp ¹⁾						(equally weighted 20 Hz...16 kHz) ³⁾ same signal source on left and right disturbing channel, effect on each observed output channel
XTALK	Crosstalk from Main or AUX Output to SCART Output and vice versa D = disturbing program O = observed program						(equally weighted 20 Hz...20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel
	D: MONO/SCn_IN/DSP → SCn_OUT	PLCC68	85			dB	
	O: DSP → DACp ¹⁾	PSDIP64	80			dB	SCART output load resistance 10 kΩ
	D: MONO/SCn_IN/DSP → SCn_OUT	PLCC68	90			dB	
	O: DSP → DACp ¹⁾	PSDIP64	85			dB	SCART output load resistance 30 kΩ
	D: DSP → DACp	PLCC68	100			dB	3)
	O: MONO/SCn_IN → SCn_OUT ¹⁾	PSDIP64	95			dB	
	D: DSP → DACM	PLCC68	100			dB	
	O: DSP → SCn_OUT ¹⁾	PSDIP64	95			dB	

1) "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

2) DSP measured at I²S-Output

3) DSP Input at I²S-Input

4.6.3.10. Sound Standard Dependent Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
NICAM Characteristics (MSP Standard Code = 8)							
dV _{NICAMOUT}	Tolerance of Output Voltage of NICAM Baseband Signal	DACp_s, SCn_OUT_s ¹⁾	−1.5		+1.5	dB	2.12 kHz, Modulator input level = 0 dBref
S/N _{NICAM}	S/N of NICAM Baseband Signal		72			dB	NICAM: −6 dB, 1 kHz, RMS unweighted 0 to 15 kHz, Vol = 9 dB NIC_Presc = 7Fh Output level 1 V _{RMS} at DACp_s
THD _{NICAM}	Total Harmonic Distortion + Noise of NICAM Baseband Signal				0.1	%	2.12 kHz, Modulator input level = 0 dBref
BER _{NICAM}	NICAM: Bit Error Rate				1	10 ^{−7}	FM+NICAM, norm conditions
fR _{NICAM}	NICAM Frequency Response , 20...15000 Hz		−1.0		+1.0	dB	Modulator input level = −12 dB dBref; RMS
XTALK _{NICAM}	NICAM Crosstalk Attenuation (Dual)		80			dB	
SEP _{NICAM}	NICAM Channel Separation (Stereo)	80				dB	
FM Characteristics (MSP Standard Code = 3)							
dV _{FMOUT}	Tolerance of Output Voltage of FM Demodulated Signal	DACp_s, SCn_OUT_s ¹⁾	−1.5		+1.5	dB	1 FM-carrier, 50 μs, 1 kHz, 40 kHz deviation; RMS
S/N _{FM}	S/N of FM Demodulated Signal		73			dB	1 FM-carrier 5.5 MHz, 50 μs, 1 kHz, 40 kHz deviation; RMS, unweighted 0 to 15 kHz (for S/N); full input range, FM-Prescale = 46 h, Vol = 0 dB → Output Level 1 V _{RMS} at DACp_s
THD _{FM}	Total Harmonic Distortion + Noise of FM Demodulated Signal				0.1	%	
fR _{FM}	FM Frequency Responses, 20...15000 Hz		−1.0		+1.0	dB	1 FM-carrier 5.5 MHz, 50 μs, Modulator input level = −14.6 dBref; RMS
XTALK _{FM}	FM Crosstalk Attenuation (Dual)		80			dB	2 FM-carriers 5.5/5.74 MHz, 50 μs, 1 kHz, 40 kHz deviation; Bandpass 1 kHz
SEP _{FM}	FM Channel Separation (Stereo)	DACp_s, SCn_OUT_s ¹⁾	50			dB	2 FM-carriers 5.5/5.74 MHz, 50 μs, 1 kHz, 40 kHz deviation; RMS
AM Characteristics (MSP Standard Code = 9)							
S/N _{AM}	S/N of AM Demodulated Signal	DACp_s, SCn_OUT_s ¹⁾	48			dB	SIF input range: 0.1–0.8 V _{pp} ; AM = 70%, 1 kHz, RMS unweighted (S/N); 0 to 15 kHz, FM/AM-Prescale = 3C _{hex} , Vol = 0 dB → Output level: 0.5 V _{RMS} at DACp_s FM+NICAM, norm conditions
THD _{AM}	Total Harmonic Distortion + Noise of AM Demodulated Signal				0.3	%	

¹⁾ “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “Loudspeaker (Main)” or “Headphone (AUX)”

²⁾ DSP measured at I²S-Output

³⁾ DSP Input at I²S-Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
BTSC Characteristics (MSP Standard Code = 20 _{hex} , 21 _{hex})							
S/N _{BTSC}	S/N of BTSC Stereo Signal S/N of BTSC-SAP Signal	DACp_s, SCn_OUT_s ¹⁾	68 57			dB dB	1 kHz L or R or SAP, 100% modulation, 75 μs deemphasis, RMS unweighted 0 to 15 kHz
THD _{BTSC}	THD+N of BTSC Stereo Signal THD+N of BTSC SAP Signal				0.1 0.8	% %	1 kHz L or R or SAP, 100% 75 μs EIM ²⁾ , DBX NR, RMS unweighted 0 to 15 kHz
fR _{BTSC}	Frequency Response of BTSC Stereo, 50 Hz...12 kHz Frequency Response of BTSC-SAP, 50 Hz...9 kHz		−0.3 −0.6		0.2 0.6	dB dB	L or R or SAP, 1%...66% EIM ²⁾ , DBX NR
XTALK _{BTSC}	Stereo → SAP SAP → Stereo		78 80			dB dB	1 kHz L or R or SAP, 100% modulation, 75 μs deemphasis, Bandpass 1 kHz
Sep _{BTSC}	Stereo Separation 50 Hz...10 kHz 50 Hz...12 kHz		35 30			dB dB	L or R 1%...66% EIM ²⁾ , DBX NR
EIA-J Characteristics (MSP Standard Code = 30 _{hex})							
S/N _{EIAJ}	S/N of EIA-J Stereo Signal S/N of EIAJ Sub-Channel	DACp_s, SCn_OUT_s ¹⁾	62 62			dB dB	1 kHz L or R, 100% modulation, 75 μs deemphasis, RMS unweighted 0 to 15 kHz
THD _{EIAJ}	THD+N of EIA-J Stereo Signal THD+N of EIA-J Sub-Channel				0.2 0.3	% %	
fR _{EIAJ}	Frequency Response of EIA-J Stereo, 50 Hz...12 kHz Frequency Response of EIA-J Sub-Channel, 50 Hz...12 kHz		−0.2 -0.3		0.6 1.2	dB dB	100% modulation, 75 μs deemphasis
XTALK _{EIAJ}	Main → SUB Sub → MAIN		66 80			dB dB	1 kHz L or R, 100% modulation, 75 μs deemphasis, Bandpass 1 kHz
SEP _{EIAJ}	Stereo Separation 50 Hz...5 kHz 50 Hz...10 kHz		35 28			dB dB	EIA-J Stereo Signal, L or R 100% modulation
FM-Radio Characteristics (MSP Standard Code = 40 _{hex})							
S/N _{UKW}	S/N of FM-Radio Stereo Signal	DACp_s, SCn_OUT_s ¹⁾	70			dB	1 kHz L or R, 100% modulation, 75 μs deemphasis, RMS unweighted 0 to 15 kHz
THD _{UKW}	THD+N of FM-Radio Stereo Signal				0.1	%	
fR _{UKW}	Frequency Response of FM-Radio Stereo 50 Hz...12 kHz 50 Hz...15 kHz		−0.1 −1.0		+0.1 +0.1	dB dB	L or R, 1%...100% modulation, 75 μs deemphasis
Sep _{UKW}	Stereo Separation 50 Hz...15 kHz		45			dB	

1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

2) EIM refers to 75-μs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-μs preemphasis network.

5. Appendix A: Overview of TV-Sound Standards

5.1. NICAM 728

Table 5–1: Summary of NICAM 728 sound modulation parameters

Specification	I	B/G	L		D/K	
Carrier frequency of digital sound	6.552 MHz	5.85 MHz	5.85 MHz		5.85 MHz	
Transmission rate	728 kbit/s					
Type of modulation	Differentially encoded quadrature phase shift keying (DQPSK)					
Spectrum shaping Roll-off factor	by means of Roll-off filters					
	1.0	0.4	0.4		0.4	
Carrier frequency of analog sound component	6.0 MHz FM mono	5.5 MHz FM mono	6.5 MHz AM mono terrestrial cable		6.5 MHz FM mono	
Power ratio between vision carrier and analog sound carrier	10 dB	13 dB	10 dB	16 dB	13 dB	
Power ratio between analog and modulated digital sound carrier	10 dB	7 dB	17 dB	11 dB	China/ Hungary	Poland
					12 dB	7 dB

Table 5–2: Summary of NICAM 728 sound coding characteristics

Characteristics	Values
Audio sampling frequency	32 kHz
Number of channels	2
Initial resolution	14 bit/sample
Companding characteristics	near instantaneous, with compression to 10 bits/sample in 32-samples (1 ms) blocks
Coding for compressed samples	2's complement
Preemphasis	CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz)
Audio overload level	+12 dBm measured at the unity gain frequency of the preemphasis network (2 kHz)

5.2. A2-Systems

Table 5–3: Key parameters for A2 Systems of Standards B/G, D/K, and M

Characteristics	Sound Carrier FM1			Sound Carrier FM2		
TV-Sound Standard	B/G	D/K	M	B/G	D/K	M
Carrier frequency in MHz	5.5	6.5	4.5	5.7421875	6.2578125 6.7421875	4.724212
Vision/sound power difference	13 dB			20 dB		
Sound bandwidth	40 Hz to 15 kHz					
Preemphasis	50 μs		75 μs	50 μs		75 μs
Frequency deviation (nom/max)	±27/±50 kHz		±17/±25 kHz	±27/±50 kHz		±15/±25 kHz
Transmission Modes						
Mono transmission	mono			mono		
Stereo transmission	(L+R)/2		(L+R)/2	R		(L–R)/2
Dual sound transmission	language A			language B		
Identification of Transmission Mode						
Pilot carrier frequency				54.6875 kHz		55.0699 kHz
Max. deviation portion				±2.5 kHz		
Type of modulation / modulation depth				AM / 50%		
Modulation frequency				mono: unmodulated stereo: 117.5 Hz dual: 274.1 Hz		149.9 Hz 276.0 Hz

5.3. BTSC-Sound System

Table 5–4: Key parameters for BTSC-Sound Systems

	Aural Carrier	BTSC-MPX-Components				
		(L+R)	Pilot	(L–R)	SAP	Prof. Ch.
Carrier frequency ($f_h = 15.734$ kHz)	4.5 MHz	Baseband	f_h	$2 f_h$	$5 f_h$	$6.5 f_h$
Sound bandwidth in kHz		0.05 - 15		0.05 - 15	0.05 - 12	0.05 - 3.4
Preemphasis		75 μ s		DBX	DBX	150 μ s
Max. deviation to Aural Carrier	73 kHz (total)	25 kHz ¹⁾	5 kHz	50 kHz ¹⁾	15 kHz	3 kHz
Max. Freq. Deviation of Subcarrier Modulation Type				AM	10 kHz FM	3 kHz FM
¹⁾ Sum does not exceed 50 kHz due to interleaving effects						

5.4. Japanese FM Stereo System (EIA-J)

Table 5–5: Key parameters for Japanese FM-Stereo Sound System EIA-J

	Aural Carrier FM	EIA-J-MPX-Components		
		(L+R)	(L–R)	Identification
Carrier frequency ($f_h = 15.793$ kHz)	4.5 MHz	Baseband	$2 f_h$	$3.5 f_h$
Sound bandwidth		0.05 - 15 kHz	0.05 - 15 kHz	–
Preemphasis		75 μ s	75 μ s	none
Max. deviation portion to Aural Carrier	47 kHz	25 kHz	20 kHz	2 kHz
Max. Freq. Deviation of Subcarrier Modulation Type			10 kHz FM	60% AM
Transmitter-sided delay		20 μ s	0 μ s	0 μ s
Mono transmission		L+R	–	unmodulated
Stereo transmission		L+R	L–R	982.5 Hz
Bilingual transmission		Language A	Language B	922.5 Hz

5.5. FM Satellite Sound

Table 5–6: Key parameters for FM Satellite Sound

Carrier Frequency	Maximum FM Deviation	Sound Mode	Bandwidth	Deemphasis
6.5 MHz	85	Mono	15 kHz	50 μs
7.02/7.20 MHz	50	Mono/Stereo/Bilingual	15 kHz	adaptive
7.38/7.56 MHz	50	Mono/Stereo/Bilingual	15 kHz	adaptive
7.74/7.92 MHz	50	Mono/Stereo/Bilingual	15 kHz	adaptive

5.6. FM-Stereo Radio

Table 5–7: Key parameters for FM-Stereo Radio Systems

	Aural Carrier	FM-Radio-MPX-Components			
		(L+R)	Pilot	(L–R)	RDS/ARI
Carrier frequency ($f_p = 15.734$ kHz)	10.7 MHz	Baseband	f_p	$2 f_p$	$3 f_h$
Sound bandwidth in kHz		0.05 - 15		0.05 - 15	
Preemphasis: – USA – Europe		75 μs 50 μs		75 μs 50 μs	
Max. deviation to Aural Carrier	73 kHz (100%)	45%	10%	45%	5%

6. Appendix B: Expert/Compatibility Mode

To adapt the modes of the STANDARD SELECT register to individual requirements and for reasons of **compatibility to the MSP 34x0D**, the MSP 34x0G offers an Expert/Compatibility Mode, which provides sophisticated programming of the MSP 34x0G.

Using the STANDARD SELECT register generally provides a more economic way to program the MSP 34x0G and will result in optimal behavior. **Therefore, it is not recommended to use the Expert/Compatibility mode.** Only in those cases, where compatibility with MSP 34x0D is strictly required, should the Expert/Compatibility mode be used.

Note: In case of Automatic Sound Select (MODUS[0]=1), any modifications of the demodulator write registers listed below, except AUTO_FM/AM are ignored.

6.1. Demodulator Write and Read Registers for Expert/Compatibility Mode

Table 6–1: Demodulator Write Registers; Subaddress: 10_{hex}; these registers are not readable!

Demodulator Write Registers	Address (hex)	MSP-Version	Description	Reset Mode	Page
AUTO_FM/AM	00 21	3410, 3450 ¹⁾	1. MODUS[0]=1 (Automatic Sound Select): Switching Level threshold of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception 2. MODUS[0]=0 (Manual Mode): Activation and configuration of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception	00 00	75
AD_CV	00 BB	all	SIF-input selection, configuration of AGC, and Carrier-Mute Function	00 00	76
MODE_REG	00 83	3410, 3450 ¹⁾	Controlling of MSP-Demodulator and Interface options. As soon as this register is applied, the MSP 34x0G works in the MSP 34x0D compatibility mode . Warning: In this mode, BTSC, EIA-J, and FM-Radio are disabled. Only MSP 34x0D features are available; the use of MODUS and STATUS register is not allowed. The MSP 34x0G is reset to the normal mode by first programming the MODUS register followed by transmitting a valid standard code to the STANDARD SELECTION register.	00 00	77
FIR1 FIR2	00 01 00 05		FIR1-filter coefficients channel 1 (6 · 8 bit) FIR2-filter coefficients channel 2 (6 · 8 bit), + 3 · 8 bit offset (total 72 bit)	00 00	79
DCO1_LO DCO1_HI DCO2_LO DCO2_HI	00 93 00 9B 00 A3 00 AB		Increment channel 1 Low Part Increment channel 1 High Part Increment channel 2 Low Part Increment channel 2 High Part	00 00	79
PLL_CAPS	00 1F		Not of interest for the customer Switchable PLL capacitors to tune open-loop frequency	00 00	82

¹⁾ not in BTSC, EIA-J, and FM-Radio mode

Table 6–2: Demodulator Read Registers; Subaddress: 11_{hex}; these registers are not writable!

Demodulator Read Registers	Address (hex)	MSP-Version	Description	Page
C_AD_BITS	00 23	3410, 3450	NICAM-Sync bit, NICAM-C-Bits, and three LSBs of additional data bits	81
ADD_BITS	00 38		NICAM: bit [10:3] of additional data bits	81
CIB_BITS	00 3E		NICAM: CIB1 and CIB2 control bits	81
ERROR_RATE	00 57		NICAM error rate, updated with 182 ms	82
PLL_CAPS	02 1F		Not for customer use	82
AGC_GAIN	02 1E		Not for customer use	82

6.2. DSP Write and Read Registers for Expert/Compatibility Mode

Table 6–3: DSP-Write Registers; Subaddress: 12_{hex}, all registers are readable as well

Write Register	Address (hex)	Bits	Operational Modes and Adjustable Range	Reset Mode	Page
Volume SCART1 channel: Ctrl. mode	00 07	[7..0]	[Linear mode / logarithmic mode]	00 _{hex}	83
FM Fixed Deemphasis	00 0F	[15..8]	[OFF, 50 μs, 75 μs]	OFF	83
FM Adaptive Deemphasis		[7..0]	[OFF, WP1]	OFF	83
Identification Mode	00 15	[7..0]	[B/G, M]	B/G	84
FM DC Notch	00 17	[7..0]	[ON, OFF]	ON	84
Volume SCART2 channel: Ctrl. mode	00 40	[7..0]	[Linear mode / logarithmic mode]	00 _{hex}	83

Table 6–4: DSP Read Registers; Subaddress: 13_{hex}, all registers are not writable

Additional Read Registers	Address (hex)	Bits	Output Range	Page
Stereo detection register for A2 Stereo Systems	00 18	[15..8]	[80 _{hex} ... 7F _{hex}] 8 bit two's complement	84
DC level readout FM1/Ch2-L	00 1b	[15..0]	[8000 _{hex} ... 7FFF _{hex}] 16 bit two's complement	84
DC level readout FM2/Ch1-R	00 1c	[15..0]	[8000 _{hex} ... 7FFF _{hex}] 16 bit two's complement	84

6.3. Expert/Compatibility Mode: Description of Demodulator Write Registers

6.3.1. Automatic Switching between NICAM and Analog Sound

In case of bad NICAM reception or loss of the NICAM-carrier, the MSP 34x0G offers an Automatic Switching (fall back) to the analog sound (FM/AM-Mono), without the necessity of the controller reading and evaluating any parameters. If a proper NICAM signal returns, switching back to this source is performed automatically as well. The feature evaluates the NICAM ERROR_RATE and switches, if necessary, all output channels which are assigned to the NICAM source, to the analog source, and vice versa.

An appropriate hysteresis algorithm avoids oscillating effects (see Fig. 6–1). STATUS[9] and C_AD_BITS[11] (Addr: 0023 hex) provide information about the actual NICAM-FM/AM-status.

6.3.1.1. Function in Automatic Sound Select Mode

The Automatic Sound Select feature (MODUS[0]=1) includes the procedure mentioned above. By default, the internal ERROR_RATE threshold is set to 700_{dez}. i.e. :

- NICAM → analog Sound if ERROR_RATE > 700
- analog Sound → NICAM if ERROR_RATE < 700/2

The ERROR_RATE value of 700 corresponds to a BER of approximately $5.46 \cdot 10^{-3}/s$.

Individual configuration of the threshold can be done using Table 6–5, whereby the bits 0 and 11 of AUTO_FM are ignored. It is recommended to use the internal setting used by the standard selection.

The optimum NICAM sound can be assigned to the MSP output channels by selecting one of the “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels.

6.3.1.2. Function in Manual Mode

If the manual mode (MODUS[0]=0) is required, the activation and configuration of the Automatic Switching feature has to be done as described in Table 6–5. Note, that the channel matrix of the corresponding output channels must be set according to the NICAM mode and need not to be changed in the FM/AM-fallback case.

Example:

Required threshold = 500: bits [10:1]=00 1111 1010

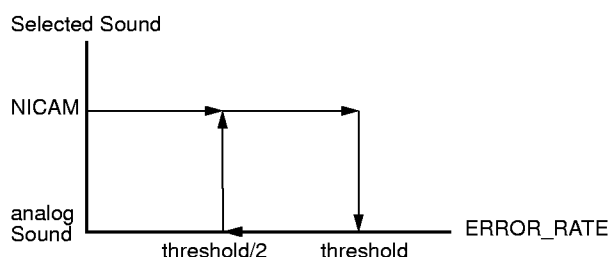


Fig. 6–1: Hysteresis for Automatic Switching

Table 6–5: Coding of Automatic NICAM/Analog Sound Switching; Reset Status: Mode 0

Mode	Description	AUTO_FM [11:0] Addr. = 00 21 _{hex}	ERROR_RATE- Threshold/dez	Source Select: Input at NICAM Path ¹⁾
0	Compatible to MSP 3410B, i.e. automatic switching is disabled	Bit [0] = 0 Bits [10:1] = 0 Bit [11] = 0	none	always NICAM; Mute in case of no NICAM available
1	Automatic Switching with internal threshold (Default, if Automatic Sound Select is on)	Bit [0] = 1 Bit [10:1] = 0 Bit [11] = 0	700	NICAM or FM/AM, depending on ERROR_RATE
2	Automatic Switching with external threshold (Customizing of Automatic Sound Select)	Bit [0] = 1 Bit [10:1] = 25..1000 = threshold/2 Bit [11] = 0	set by customer; recommended range: 50....2000	
3	Forced analog mono mode, i.e. Automatic Switching is disabled (Customizing of Automatic Sound Select)	Bit [0] = 1 Bit [10:1] = 0 Bit [11] = 1	none	always FM/AM
¹⁾ In case of Automatic Sound Select (MODUS[0] = 1), the NICAM path may be assigned to “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels (see Table 2–2 on page 11).				
In case of Automatic Sound Select (MODUS[0] = 1), bit [0] of AUTO_FM is ignored				

6.3.2. Register AD_CV

The use of this register is no longer recommended. Use it only in cases where compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x0G.

Table 6–6: AD_CV Register; reset status: all bits are “0”

AD_CV (00 BB _{hex})			Automatic setting by STANDARD SELECT Register	
Bit	Function	Settings	2-8, 0A-60 _{hex}	9
[0]	not used	must be set to 0	0	0
[1–6]	Reference level in case of Automatic Gain Control = on (see Table 6–7). Constant gain factor when Automatic Gain Control = off (see Table 6–8).		101000	100011
[7]	Determination of Automatic Gain or Constant Gain	0 = constant gain 1 = automatic gain	1	1
[8]	Selection of Sound IF source (identical to MODUS[8])	0 = ANA_IN1+ 1 = ANA_IN2+	X	X
[9]	MSP-Carrier-Mute Feature	0 = off: no mute 1 = on: mute as described in section 2.2.2.	1	0
[10–15]	not used	must be set to 0	0	0
X : not affected while choosing the TV sound standard by means of the STANDARD SELECT Register				

Table 6–7: Reference Values for Active AGC (AD_CV[7] = 1)

Application	Input Signal Contains	AD_CV [6:1] Ref. Value	AD_CV [6:1] in Integer	Range of Input Signal at pin ANA_IN1+ and ANA_IN2+
Terrestrial TV				
– FM Standards	1 or 2 FM Carriers	101000	40	0.10 – 3 V _{pp} ¹⁾
– NICAM/FM	1 FM and 1 NICAM Carrier	101000	40	0.10 – 3 V _{pp} ¹⁾
– NICAM/AM	1 AM and 1 NICAM Carrier	100011	35	0.10 – 1.4 V _{pp} (recommended: 0.10 – 0.8 V _{pp})
– NICAM only	1 NICAM Carrier only	010100	20	0.05 – 1.0 V _{pp}
SAT	1 or more FM Carriers	100011	35	0.10 – 3 V _{pp} ¹⁾
ADR	FM and ADR carriers	see DRP 3510A data sheet		
1) For signals above 1.4 V _{pp} , the minimum gain of 3 dB is switched, and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 V _{pp} , if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N ratio of about 10 dB may appear.				

Table 6–8: AD_CV parameters for Constant Input Gain (AD_CV[7]=0)

Step	AD_CV [6:1] Constant Gain	Gain	Input Level at pin ANA_IN1+ and ANA_IN2+
0	000000	3.00 dB	maximum input level: 3 V _{pp} (FM) or 1 V _{pp} (NICAM) ¹⁾
1	000001	3.85 dB	
2	000010	4.70 dB	
3	000011	5.55 dB	
4	000100	6.40 dB	
5	000101	7.25 dB	
6	000110	8.10 dB	
7	000111	8.95 dB	
8	001000	9.80 dB	
9	001001	10.65 dB	
10	001010	11.50 dB	
11	001011	12.35 dB	
12	001100	13.20 dB	
13	001101	14.05 dB	
14	001110	14.90 dB	
15	001111	15.75 dB	
16	010000	16.60 dB	
17	010001	17.45 dB	
18	010010	18.30 dB	
19	010011	19.15 dB	
20	010100	20.00 dB	maximum input level: 0.14 V _{pp}

¹⁾ For signals above 1.4 V_{pp}, the minimum gain of 3 dB is switched and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 V_{pp}, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N ratio of about 10 dB may appear.

6.3.3. Register MODE_REG

Note: The use of this register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x0G.

As soon as this register is applied, the MSP 34x0G works in the **MSP 34x0D Compatibility Mode**. In this mode: **BTSC, EIA-J, and FM-Radio are disabled**. Only MSP 34x0D features are available; the use of MODUS and STATUS register is not allowed. The MSP 34x0G is reset to the normal mode by first programming the MODUS register, followed by transmitting a valid standard code to the STANDARD SELECTION register.

The register 'MODE_REG' contains the control bits determining the operation mode of the MSP 34x0G in the MSP 34x0D Compatibility Mode; Table 6–9 explains all bit positions.

Table 6–9: Control word 'MODE_REG'; reset status: all bits are "0"

MODE_REG 00 83 _{hex}				Automatic setting by STANDARD SELECT Register		
Bit	Function	Comment	Definition	2 - 5	8, A, B	9
[0]	not used		0 : must be used	0	0	0
[1]	DCTR_TRI	Digital control out 0/1 tri-state	0 : active 1 : tri-state	X	X	X
[2]	I2S_TRI	I ² S outputs tri-state (I2S_CL, I2S_WS, I2S_DA_OUT)	0 : active 1 : tri-state	X	X	X
[3]	I ² S Mode ¹⁾	Master/Slave mode of the I ² S bus	0 : Master 1 : Slave	X	X	X
[4]	I2S_WS Mode	WS due to the Sony or Philips-Format	0 : Sony 1 : Philips	X	X	X
[5]	Audio_CL_OUT	Switch Audio_Clock_Output to tri-state	0 : on 1 : tri-state	X	X	X
[6]	NICAM ¹⁾	Mode of MSP-Ch1	0 : FM 1 : Nicam	0	1	1
[7]	not used		0 : must be used	0	0	0
[8]	FM AM	Mode of MSP-Ch2	0 : FM 1 : AM	0	0	1
[9]	HDEV	High Deviation Mode (channel matrix must be sound A)	0 : normal 1 : high deviation mode	0	0	0
[11:10]	not used		0 : must be used	0	0	0
[12]	MSP-Ch1 Gain	see also Table 6–11	0 : Gain = 6 dB 1 : Gain = 0 dB	0	0	0
[13]	FIR1-Filter Coeff. Set	see also Table 6–11	0 : use FIR1 1 : use FIR2	1	0	0
[14]	ADR	Mode of MSP-Ch1/ ADR-Interface	0 : normal mode/tri-state 1 : ADR-mode/active	0	0	0
[15]	AM-Gain	Gain for AM Demodulation	0 : 0 dB (default. of MSPB) 1 : 12 dB (recommended)	1	1	1
¹⁾ In case of NICAM operation, I ² S-slave mode is not possible. In case of I ² S-slave mode, no synchronization to NICAM is allowed.				X: not affected by short-programming		

Table 6–10: Loading sequence for FIR-coefficients

FIR1 00 01 _{hex} (MSP-Ch1: NICAM/FM2)			
No.	Symbol Name	Bits	Value
1	NICAM/FM2_Coeff. (5)	8	see Table 6–11
2	NICAM/FM2_Coeff. (4)	8	
3	NICAM/FM2_Coeff. (3)	8	
4	NICAM/FM2_Coeff. (2)	8	
5	NICAM/FM2_Coeff. (1)	8	
6	NICAM/FM2_Coeff. (0)	8	
FIR2 00 05 _{hex} (MSP-Ch2: FM1/AM)			
No.	Symbol Name	Bits	Value
1	IMREG1	8	04 _{hex}
2	IMREG1 / IMREG2	8	40 _{hex}
3	IMREG2	8	00 _{hex}
4	FM/AM_Coef (5)	8	see Table 6–11
5	FM/AM_Coef (4)	8	
6	FM/AM_Coef (3)	8	
7	FM/AM_Coef (2)	8	
8	FM/AM_Coef (1)	8	
9	FM/AM_Coef (0)	8	

6.3.4. FIR-Parameter, Registers FIR1 and FIR2

Note: The use of this register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x0G.

Data-shaping and/or FM/AM bandwidth limitation is performed by a pair of linear phase Finite Impulse Response filters (FIR-filter). The filter coefficients are programmable and are either configured automatically by the STANDARD SELECT register or written manually by the control processor via the control bus. Two not necessarily different sets of coefficients are required: one for MSP-Ch1 (NICAM or FM2) and one for MSP-Ch2 (FM1 = FM-mono). In Table 6–11 several coefficient sets are proposed.

To load the FIR-filters, the following data values are to be transferred **8 bits at a time embedded LSB-bound in a 16-bit word**.

The loading sequences must be obeyed. To change a coefficient set, the complete block FIR1 or FIR2 must be transmitted.

Note: For compatibility with MSP 3410B, IMREG1 and IMREG2 have to be transmitted. The value for IMREG1 and IMREG2 is 004. Due to the partitioning to 8-bit units, the values 04_{hex}, 40_{hex}, and 00_{hex} arise.

6.3.5. DCO-Registers

Note: The use of this register is no longer recommended. It should be used only in cases where software-compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x0G.

When selecting a TV-sound standard by means of the STANDARD SELECT register, all frequency tuning is performed automatically.

If manual setting of the tuning frequency is required, a set of 24-bit registers determining the mixing frequencies of the quadrature mixers can be written manually into the IC. In Table 6–12, some examples of DCO registers are listed. It is necessary to divide them up into low part and high part. The formula for the calculation of the registers for any chosen IF frequency is as follows:

$$\text{INCR}_{\text{dez}} = \text{int}(f/\text{fs} \cdot 2^{24})$$

with: int = integer function

f = IF frequency in MHz

f_s = sampling frequency (18.432 MHz)

Conversion of INCR into hex-format and separation of the 12-bit low and high parts lead to the required register values (DCO1_HI or _LO for MSP-Ch1, DCO2_HI or LO for MSP-Ch2).

Table 6–11: 8-bit FIR-coefficients (decimal integer) for MSP 34x0D; reset status: all coefficients are “0”

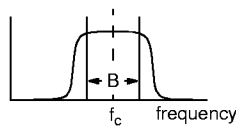
Coefficients for FIR1 00 01 _{hex} and FIR2 00 05 _{hex}														
	Terrestrial TV Standards							<div>FM - Satellite</div> <div>FIR filter corresponds to a band-pass with a band-width of B = 130 to 500 kHz</div> <div></div>						
	B/G-, D/K-NICAM-FM		I-NICAM-FM		L-NICAM-AM		B/G-, D/K-, M-Dual FM	130 kHz	180 kHz	200 kHz	280 kHz	380 kHz	500 kHz	Auto-search
Coef(l)	FIR1	FIR2	FIR1	FIR2	FIR1	FIR2	FIR2	FIR2	FIR2	FIR2	FIR2	FIR2	FIR2	FIR2
0	−2	3	2	3	−2	−4	3	73	9	3	−8	−1	−1	−1
1	−8	18	4	18	−8	−12	18	53	18	18	−8	−9	−1	−1
2	−10	27	−6	27	−10	−9	27	64	28	27	4	−16	−8	−8
3	10	48	−4	48	10	23	48	119	47	48	36	5	2	2
4	50	66	40	66	50	79	66	101	55	66	78	65	59	59
5	86	72	94	72	86	126	72	127	64	72	107	123	126	126
Mode-REG[12]	0		0		0		0	1	1	1	1	1	1	0
Mode-REG[13]	0		0		0		1	1	1	1	1	1	1	0
For compatibility, except for the FIR2-AM and the Autosearch-sets, the FIR-filter programming as used for the MSP 3410B is also possible.														
ADR coefficients are listed in the DRP data sheet.														

Table 6–12: DCO registers for the MSP 34x0G; reset status: DCO_HI/LO = “0000”

DCO1_LO 00 93 _{hex} , DCO1_HI 00 9B _{hex} ; DCO2_LO 00 A3 _{hex} , DCO2_HI 00 AB _{hex}					
Freq. MHz	DCO_HI/hex	DCO_LO/hex	Freq. MHz	DCO_HI/hex	DCO_LO/hex
4.5	03E8	000			
5.04	0460	0000	5.76	0500	0000
5.5	04C6	038E	5.85	0514	0000
5.58	04D8	0000	5.94	0528	0000
5.7421875	04FC	00AA			
6.0	0535	0555	6.6	05BA	0AAA
6.2	0561	0C71	6.65	05C5	0C71
6.5	05A4	071C	6.8	05E7	01C7
6.552	05B0	0000			
7.02	0618	0000	7.2	0640	0000
7.38	0668	0000	7.56	0690	0000

6.4. Expert/Compatibility Mode: Description of Demodulator Read Registers

Note: The use of these register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the STATUS register provides a more economic way to program the MSP 34x0G and to retrieve information from the IC.

All registers except C_AD_BITS are 8 bits wide. They can be read out of the RAM of the MSP 34x0G if the MSP 34x0D compatibility mode is required.

All transmissions take place in 16-bit words. The valid 8-bit data are the 8 LSBs of the received data word.

If the Automatic Sound Select feature is not used, the NICAM or FM-identification parameters must be read and evaluated by the controller in order to enable appropriate switching of the channel select matrix of the baseband processing part. The FM-identification registers are described in section 6.6.1. To handle the NICAM-sound and to observe the NICAM-quality, at least the registers C_AD_BITS and ERROR_RATE must be read and evaluated by the controller. Additional data bits and CIB bits, if supplied by the NICAM transmitter, can be obtained by reading the registers ADD_BITS and CIB_BITS.

6.4.1. NICAM Mode Control/Additional Data Bits Register

NICAM operation mode control bits and A[2:0] of the additional data bits.

Format:

MSB		C_AD_BITS 00 23 _{hex}							LSB
11	...	7	6	5	4	3	2	1	0
Auto_FM	...	A[2]	A[1]	A[0]	C4	C3	C2	C1	S

Important: “S” = Bit[0] indicates correct NICAM-synchronization (S = 1). If S = 0, the MSP 3410/3450G has not yet synchronized correctly to frame and sequence, or has lost synchronization. The remaining read registers are therefore not valid. The MSP mutes the NICAM output automatically and tries to synchronize again as long as MODE_REG[6] is set.

The operation mode is coded by C4-C1 as shown in Table 6–13.

Table 6–13: NICAM operation modes as defined by the EBU NICAM 728 specification

C4	C3	C2	C1	Operation Mode
0	0	0	0	Stereo sound (NICAMA/B), independent mono sound (FM1)
0	0	0	1	Two independent mono signals (NICAMA, FM1)
0	0	1	0	Three independent mono channels (NICAMA, NICAMB, FM1)
0	0	1	1	Data transmission only; no audio
1	0	0	0	Stereo sound (NICAMA/B), FM1 carries same channel
1	0	0	1	One mono signal (NICAMA). FM1 carries same channel as NICAMA
1	0	1	0	Two independent mono channels (NICAMA, NICAMB). FM1 carries same channel as NICAMA
1	0	1	1	Data transmission only; no audio
x	1	x	x	Unimplemented sound coding option (not yet defined by EBU NICAM 728 specification)
AUTO_FM: monitor bit for the AUTO_FM Status: 0: NICAM source is NICAM 1: NICAM source is FM				

Note: It is no longer necessary to read out and evaluate the C_AD_BITS. All evaluation is performed in the MSP and indicated in the STATUS register.

6.4.2. Additional Data Bits Register

Contains the remaining 8 of the 11 additional data bits. The additional data bits are not yet defined by the NICAM 728 system.

Format:

MSB		ADD_BITS 00 38 _{hex}						LSB
7	6	5	4	3	2	1	0	
A[10]	A[9]	A[8]	A[7]	A[6]	A[5]	A[4]	A[3]	

6.4.3. CIB Bits Register

CIB bits 1 and 2 (see NICAM 728 specifications).

Format:

MSB		CIB_BITS 00 3E _{hex}						LSB
7	6	5	4	3	2	1	0	
x	x	x	x	x	x	CIB1	CIB2	

6.4.4. NICAM Error Rate Register

ERROR_RATE	00 57 _{hex}
Error free	0000 _{hex}
maximum error rate	07FF _{hex}

Average error rate of the NICAM reception in a time interval of 182 ms, which should be close to 0. The initial and maximum value of ERROR_RATE is 2047. This value is also active if the NICAM bit of MODE_REG is not set. Since the value is achieved by filtering, a certain transition time (approx. 0.5 sec) is unavoidable. Acceptable audio may have error rates up to a value of 700 int. Individual evaluation of this value by the controller and an appropriate threshold may define the fallback mode from NICAM to FM/AM-Mono in case of poor NICAM reception.

The bit error rate per second (BER) can be calculated by means of the following formula:

$$\text{BER} = \text{ERROR_RATE} * 12.3 * 10^{-6} / \text{s}$$

6.4.5. PLL_CAPS Readback Register

It is possible to read out the actual setting of the PLL_CAPS. In standard applications, this register is not of interest for the customer.

PLL_CAPS	02 1F _{hex}
minimum frequency	0111 1111 7F _{hex}
nominal frequency	0101 0110 56 _{hex} RESET
maximum frequency	0000 0000 00 _{hex}

6.4.6. AGC_GAIN Readback Register

It is possible to read out the actual setting of AGC_GAIN in Automatic Gain Mode. In standard applications, this register is not of interest for the customer.

AGC_GAIN	02 1E _{hex}
max. amplification (20 dB)	0001 0100 14 _{hex}
min. amplification (3 dB)	0000 0000 00 _{hex}

6.4.7. Automatic Search Function for FM-Carrier Detection in Satellite Mode

The AM demodulation ability of the MSP 3410G and MSP 3450G offers the possibility to calculate the “field strength” of the momentarily selected FM carrier, which can be read out by the controller. In SAT receivers, this feature can be used to make automatic FM carrier search possible.

For this, the MSP has to be switched to AM-mode (MODE_REG[8]), FM-Prescale must be set to 7F_{hex} = +127_{dez}, and the FM DC notch (see section 6.5.7.) must be switched off. The sound-IF frequency range must now be “scanned” in the MSP-channel 2 by means of the programmable quadrature mixer with an appropriate incremental frequency (i.e. 10 kHz). After each incrementation, a field strength value is available at the quasi-peak detector output (quasi-peak detector source must be set to FM), which must be examined for relative maxima by the controller. This results in either continuing search or switching the MSP back to FM demodulation mode.

During the search process, the FIR2 must be loaded with the coefficient set “AUTOSEARCH”, which enables small bandwidth, resulting in appropriate field strength characteristics. The absolute field strength value (can be read out of “quasi-peak detector output FM1”) also gives information on whether a main FM carrier or a subcarrier was detected; and as a practical consequence, the FM bandwidth (FIR1/2) and the deemphasis (50 μs or adaptive) can be switched accordingly.

Due to the fact that a constant demodulation frequency offset of a few kHz leads to a DC level in the demodulated signal, further fine tuning of the found carrier can be achieved by evaluating the “DC Level Readout FM1”. Therefore, the FM DC Notch must be switched on, and the demodulator part must be switched back to FM-demodulation mode.

For a detailed description of the automatic search function, please refer to the corresponding MSP Windows software.

6.5. Expert/Compatibility Mode: Description of DSP Write Registers

6.5.1. Additional Channel Matrix Modes

Loudspeaker Matrix	00 08 _{hex}	L
Headphone Matrix	00 09 _{hex}	L
SCART1 Matrix	00 0a _{hex}	L
SCART2 Matrix	00 41 _{hex}	L
I ² S Matrix	00 0B _{hex}	L
Quasi-Peak Detector Matrix	00 0C _{hex}	L
SUM/DIFF	0100 0000	40 _{hex}
AB_XCHANGE	0101 0000	50 _{hex}
PHASE_CHANGE_B	0110 0000	60 _{hex}
PHASE_CHANGE_A	0111 0000	70 _{hex}
A_ONLY	1000 0000	80 _{hex}
B_ONLY	1001 0000	90 _{hex}

This table shows additional modes for the channel matrix registers.

The sum/difference mode can be used together with the quasi-peak detector to determine the sound material mode. If the difference signal on channel B (right) is near to zero, and the sum signal on channel A (left) is high, the incoming audio signal is mono. If there is a significant level on the difference signal, the incoming audio is stereo.

6.5.2. Volume Modes of SCART1/2 Outputs

Volume Mode SCART1	00 07 _{hex}	[3:0]
Volume Mode SCART2	00 40 _{hex}	[3:0]
linear	0000 RESET	0 _{hex}
logarithmic	0001	1 _{hex}

Linear Mode		
Volume SCART1	00 07 _{hex}	H
Volume SCART2	00 40 _{hex}	H
OFF	0000 0000 RESET	00 _{hex}
0 dB gain (digital full scale (FS) to 2 V _{RMS} output)	0100 0000	40 _{hex}
+6 dB gain (–6 dBFS to 2 V _{RMS} output)	0111 1111	7F _{hex}

6.5.3. FM Fixed Deemphasis

FM Deemphasis	00 0F _{hex}	H
50 μs	0000 0000 RESET	00 _{hex}
75 μs	0000 0001	01 _{hex}
OFF	0011 1111	3F _{hex}

6.5.4. FM Adaptive Deemphasis

FM Adaptive Deemphasis WP1	00 0F _{hex}	L
OFF	0000 0000 RESET	00 _{hex}
WP1	0011 1111	3F _{hex}

6.5.5. NICAM Deemphasis

A J17 Deemphasis is always applied to the NICAM signal. It is not switchable.

6.5.6. Identification Mode for A2 Stereo Systems

Identification Mode	00 15 _{hex}	L
Standard B/G (German Stereo)	0000 0000 RESET	00 _{hex}
Standard M (Korean Stereo)	0000 0001	01 _{hex}
Reset of Ident-Filter	0011 1111	3F _{hex}

To shorten the response time of the identification algorithm after a program change between two FM-Stereo capable programs, the reset of the ident-filter can be applied.

Sequence:

1. Program change
2. Reset ident-filter
3. Set identification mode back to standard B/G or M
4. Read stereo detection register

6.5.7. FM DC Notch

The DC compensation filter (FM DC Notch) for FM input can be switched off. This is used to speed up the automatic search function (see Section 6.4.7.). In normal FM-mode, the FM DC Notch should be switched on.

FM DC Notch	00 17 _{hex}	L
ON	0000 0000 Reset	00 _{hex}
OFF	0011 1111	3F _{hex}

6.6. Expert/Compatibility Mode: Description of DSP Read Registers

All readable registers are 16-bit wide. Transmissions via I²C bus have to take place in 16-bit words. Some of the defined 16-bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writable.

6.6.1. Stereo Detection Register for A2 Stereo Systems

Stereo Detection Register	00 18 _{hex}	H
Stereo Mode	Reading (two's complement)	
MONO	near zero	
STEREO	positive value (ideal reception: 7F _{hex})	
BILINGUAL	negative value (ideal reception: 80 _{hex})	

Note: It is no longer necessary to read out and evaluate the A2 identification level. All evaluation is performed in the MSP and indicated in the STATUS register.

6.6.2. DC Level Register

DC Level Readout FM1 (MSP-Ch2)	00 1b _{hex}	H+L
DC Level Readout FM2 (MSP-Ch1)	00 1c _{hex}	H+L
DC Level	[8000 _{hex} ... 7FFF _{hex}] values are 16 bit two's complement	

The DC level register measures the DC component of the incoming FM signals (FM1 and FM2). This can be used for seek functions in satellite receivers and for IF FM frequencies fine tuning. A too low demodulation frequency (DCO) results in a positive DC-level and vice versa. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant τ , defining the transition time of the DC Level Register, is approximately 28 ms.

6.7. Demodulator Source Channels in Manual Mode

6.7.1. Terrestrial Sound Standards

Table 6–14 shows the source channel assignment of the demodulated signals in case of manual mode for all terrestrial sound standards. See Table 2–2 for the assignment in the Automatic Sound Select mode. In manual mode for terrestrial sound standards, only two demodulator sources are defined.

6.7.2. SAT Sound Standards

Table 6–15 shows the source channel assignment of the demodulated signals for SAT sound standards.

Table 6–14: Manual Sound Select Mode for Terrestrial Sound Standards

				Source Channels of Sound Select Block	
Broadcasted Sound Standard	Selected MSP Standard Code	Broadcasted Sound Mode	FM Matrix	FM/AM (use 0 for channel select)	Stereo or A/B (use 1 for channel select)
B/G-FM D/K-FM M-Korea M-Japan	03 04, 05 02 30	MONO	Sound A Mono	Mono	Mono
		STEREO	German Stereo Korean Stereo	Stereo	Stereo
		BILINGUAL, Languages A and B	No Matrix	Left = A Right = B	Left = A Right = B
B/G-NICAM L-NICAM I-NICAM D/K-NICAM D/K-NICAM (with high deviation FM)	08 09 0A 0B 0C	NICAM not available or NICAM error rate too high	Sound A Mono	analog Mono	no sound with AUTO_FM: analog Mono
		MONO	Sound A Mono	analog Mono	NICAM Mono
		STEREO	Sound A Mono	analog Mono	NICAM Stereo
		BILINGUAL, Languages A and B	Sound A Mono	analog Mono	Left = NICAM A Right = NICAM B
M-BTSC	20	MONO	Sound A Mono	Mono	Mono
		STEREO	Korean Stereo	Stereo	Stereo
		MONO + SAP	Sound A Mono	Mono	Mono
		STEREO + SAP	Korean Stereo	Stereo	Stereo
	21	MONO	Sound A Mono	Mono	Mono
		STEREO			
		MONO + SAP	No Matrix	Left = Mono Right = SAP	Left = Mono Right = SAP
		STEREO + SAP			
FM-Radio	40	MONO	Sound A Mono	Mono	Mono
		STEREO	Korean Stereo	Stereo	Stereo

Table 6–15: Manual Sound Select Modes for SAT-Modes (FM Matrix is set automatically)

			Source Channels of Sound Select Block for SAT-Modes			
Broadcasted Sound Standard	Selected MSP Standard Code	Broadcasted Sound Mode	FM/AM (source select: 0)	Stereo or A/B (source select: 1)	Stereo or A (source select: 3)	Stereo or B (source select: 4)
FM SAT	6, 50 _{hex}	MONO	Mono	Mono	Mono	Mono
	51 _{hex}	STEREO	Stereo	Stereo	Stereo	Stereo
		BILINGUAL	Left = A (FM1) Right = B (FM2)	Left = A (FM1) Right = B (FM2)	A (FM1)	B (FM2)

6.8. Exclusions of Audio Baseband Features

In general, all functions can be switched independently. Two exceptions exist:

1. NICAM cannot be processed simultaneously with the FM2 channel.
2. FM adaptive deemphasis cannot be processed simultaneously with FM-identification.

6.9. Phase Relationship of Analog Outputs

The analog output signals: Loudspeaker, headphone, and SCART2 all have the same phases. The user does not need to correct output phases when using these analog outputs directly. The SCART1 output has opposite phase.

Using the I²S-outputs for other DSPs or D/A converters, care must be taken to adjust for the correct phase. If the attached coprocessor is one of the MSP family, the following schematics help to determine the phase relationship.

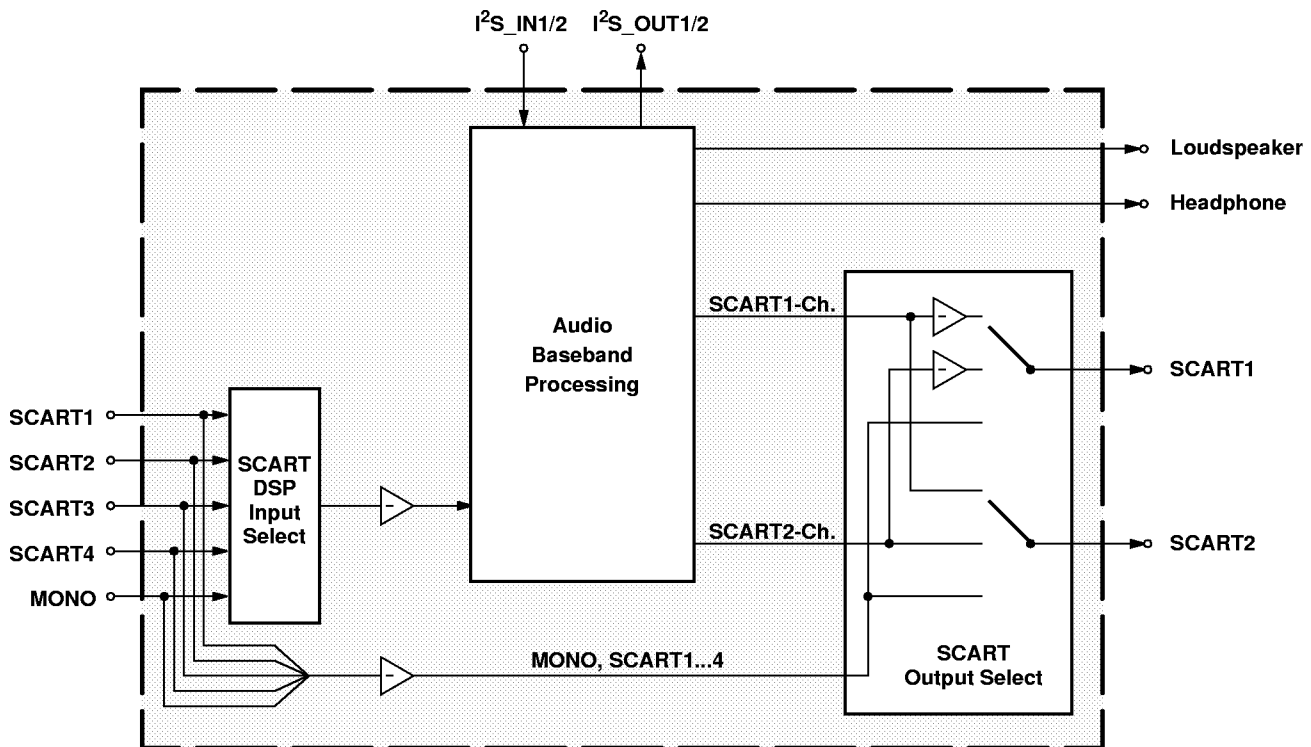


Fig. 6-2: Phase diagram of the MSPG

7. Appendix C: Incompatibility of MSP 34x0G-A2 or later to the MSP 3430G Version A1

There is one slight incompatibility between the MSP 3430G-A1 and all MSP 34x0G versions based on A2 or later, as for example the MSP 3440G-A2. The difference refers only to the Source Select Registers (see page 26). A2 or later versions have four addresses in Automatic Sound Select mode in order to provide greater flexibility. The A1 version uses only two addresses. Figure 7–1 and Tables 7–1, 7–2, and 7–3 define the differences.

Note: The channels “Stereo or A” and “Stereo or B” in A2 or later versions are identical to the “Automatic A” or “Automatic B” channels for the A1 version. This makes it easy to develop controller programs compatible to both versions. The A2 or later versions can be distinguished from the A1 version by reading the MSP ROM Version Code register (see page 35).

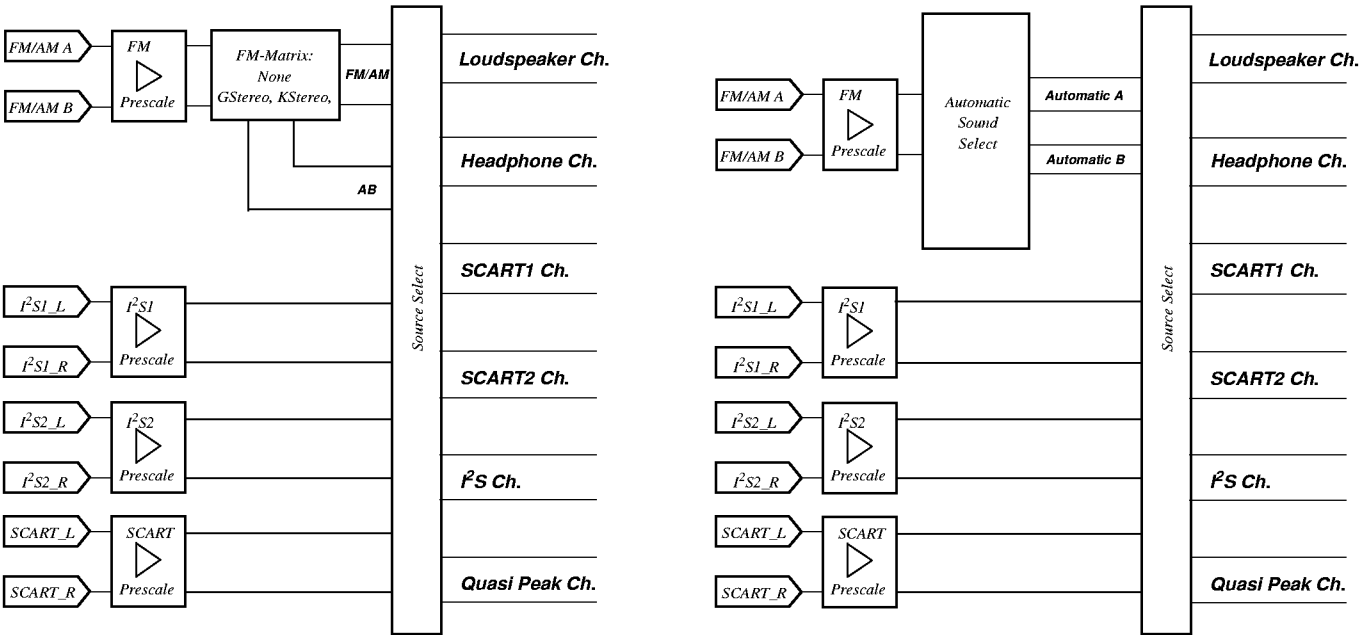


Fig. 7–1: Source Select Inputs for Automatic Sound Select = off (left) and = on (right) in MSP 3430G-A1

Table 7–1: Assignments of Source Select Inputs for manual (MSPD-Compatibility) Mode
(Version A1: left, A2 or later: right)

Received Standard (Table 3–6)	Version A1: Manual Mode (FM-Matrix = NOMATRIX)		Version A2 or later: Manual Mode (FM-Matrix = NOMATRIX)	
	FM/AM	AB	FM/AM	Stereo or A / B
BTSC “20 _{hex} ” FM-Radio “40 _{hex} ”				
L + R = MONO	Mono / undefined	Mono / undefined	Mono / undefined	Mono / undefined
STEREO	(L+R) / (L–R)	(L+R) / (L–R)	(L+R) / (L–R)	(L+R) / (L–R)
MONO + SAP	Mono / undefined	Mono / undefined	Mono / undefined	Mono / undefined
STEREO + SAP	(L+R) / (L–R)	(L+R) / (L–R)	(L+R) / (L–R)	(L+R) / (L–R)
BTSC “21_{hex}” (BTSC-SAP)				
L + R = MONO	Mono / undefined	Mono	Mono / undefined	Mono / undefined
STEREO	Mono / undefined	Mono	Mono / undefined	Mono / undefined
MONO + SAP	Mono / SAP	SAP / SAP	Mono / SAP	Mono / SAP
STEREO + SAP	Mono / SAP	SAP / SAP	Mono / SAP	Mono / SAP

Note: Instead of using addresses 00_{hex} and 01_{hex}, use the addresses 03_{hex}, 04_{hex} for version A2 or later. This gives the same results as in the A1 version in the Automatic Sound Selection mode.

Table 7–2: Assignments of Source Select Inputs for Automatic Sound Select Mode (A1 left, A2 or later right)

Received Standard (Table 3–6)	Version A1: Automatic Sound Select Mode (FM-Matrix is set automatically)		Version A2 or later: Automatic Sound Select Mode (FM-Matrix is set automatically)			
	Automatic A (00 _{hex})	Automatic B (01 _{hex})	FM/AM (00 _{hex})	Stereo or A/B (01 _{hex})	Stereo or Language A (03 _{hex})	Stereo or Language B (04 _{hex})
BTSC “20 _{hex} ” FM-Radio “40 _{hex} ”						
L + R = MONO	Mono	Mono	Mono	Mono	Mono	Mono
STEREO	Stereo	Stereo	Stereo	Stereo	Stereo	Stereo
MONO + SAP	Mono	Mono	Mono	Mono	Mono	Mono
STEREO + SAP	Stereo	Stereo	Stereo	Stereo	Stereo	Stereo
BTSC “21_{hex}” (BTSC-SAP)						
L + R = MONO	Mono	Mono	Mono	Mono	Mono	Mono
STEREO	Stereo	Stereo	Stereo	Stereo	Stereo	Stereo
MONO + SAP	Mono	SAP	Mono / SAP	Mono / SAP	Mono	SAP
STEREO + SAP	Mono	SAP	Mono / SAP	Mono / SAP	Mono	SAP

Table 7–3: Channel Source-Select Register

Loudspeaker Source		00 08_{hex}	H
Headphone Source		00 09_{hex}	H
SCART1 Source		00 0A_{hex}	H
SCART2 Source		00 41_{hex}	H
I²S Source		00 0B_{hex}	H
Quasi-Peak Detector Source		00 0C_{hex}	H
Manual Mode	Automatic Sound Select		
FM/AM	Automatic A	0000 0000 RESET	00 _{hex}
AB	Automatic B	0000 0001	01 _{hex}
none	none	0000 0011	03 _{hex}
none	none	0000 0100	04 _{hex}
SCART		0000 0010	02 _{hex}
I ² S1		0000 0101	05 _{hex}
I ² S2		0000 0110	06 _{hex}

8. Appendix D: MSP 34x0G Version History

MSP 3430G-A1

First release for BTSC-Stereo/SAP and FM-Radio. Slight incompatibility to Version A2 or later is explained in Appendix C: Incompatibility of MSP 34x0G-A2 or later to the MSP 3430G Version A1.

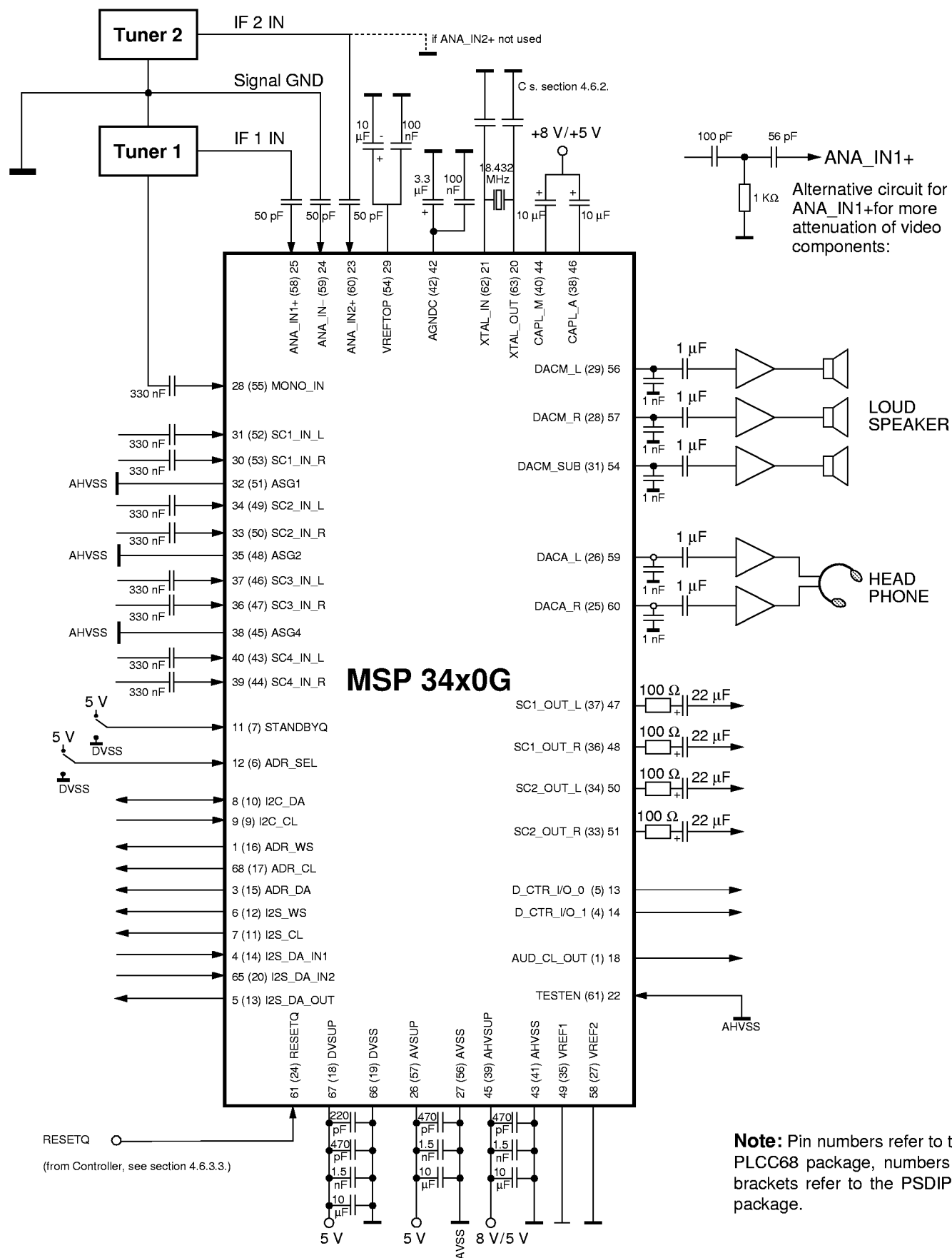
MSP 3440G-A2

Extended Automatic Sound Select feature (incompatible to Version A1).

Known restrictions:

- SAP detection unstable

9. Appendix E: Application Circuit



10. Data Sheet History

1. Preliminary data sheet: "MSP 34x0G Multistandard Sound Processor Family", Edition Sept. 30, 1998, 6251-476-1PD. First release of the preliminary data sheet.

2. Preliminary data sheet: "MSP 34x0G Multistandard Sound Processor Family", Edition Oct. 9, 1998, 6251-476-2PD. Second release of the preliminary data sheet. Major changes:

- Table 3–8 on page 22: MODUS Register bit [0] function changed
- Table 3–10 on page 30: Treble Headphone Channel register address changed, bit [15:8] hex and dB values changed
- Table 3–10 on page 33: Volume SCART1/2 Output Channel register address changed
- Table 6–14 on page 85: M-BTSC and RM-Radio description changed
- pin ASG3 changed to "not connected"

MICRONAS INTERMETALL GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@intermetall.de
Internet: <http://www.intermetall.de>

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Preliminary Data Sheet Supplement

Subject:	Version History / Failure Report for MSP 34xxG
Data Sheet Concerned:	MSP 34x0G 6251-476-2PD, Oct. 9, 1998
Supplement:	No. 2/ 6251-476-2PDS
Edition:	Feb. 25, 1999

Known Problems in MSP 34xxG

For a detailed description of the problems in the table below, please refer to the following sections.

MSP Version	SAP Detection	PAL-N Stereo Decoding	Startup Sequence	Stereo/SAP Detection Delay
3430G-A1	according Specification	no	ok	200 ms
3435G-A2	according Specification	no	ok	200 ms
3440G-A2	unreliable	no	ok	200 ms
3430G-A3	increased robustness	no	100 ms timing constraint	approx. 4 sec
3440G-A3	increased robustness	no	100 ms timing constraint	approx. 4 sec
3430G-A4	increased robustness	yes	ok	600 ms / 200 ms
3435G-A4	increased robustness	yes	ok	600 ms / 200 ms
3440G-A4	increased robustness	yes	ok	600 ms / 200 ms
3450G-B4	increased robustness	yes	ok	600 ms / 200 ms

1. SAP Detection**1.1. Robustness of the SAP Detection (A1, A2)**

The automatic SAP detection fails with signals having SAP carrier modulation below the specified limits of the BTSC System, as presented to the Federal Communications Commission by the Electronics Industries Association.

Up until now, this did not happen in any of the various worldwide fieldtests, but occurred in combination with an uncalibrated system in a TV manufacturer's lab.

Later MSP versions contain an SAP detection algorithm with increased robustness.

1.2. Unreliable SAP Detection (MSP3440G-A2 only)

Due to an internal error, the automatic SAP detection occasionally fails. Resultingly, the STATUS Bit[8] SAP/BIL is not reliable, as far as the existence of an SAP signal in BTSC modes 20_{hex} and 21_{hex} is concerned. The STATUS Bit[8] SAP/BIL is still valid in all other modes of the MSP 34xxG (A2-Korea, EIA-J).

The STATUS Bit[8] is used to automatically switch the sources for the Automatic Channels ST-A and ST-B in Mode 21_{hex} (BTSC-SAP). This does not work in the MSP34xxG-A2. Therefore, it is not recommended for the MSP34xxG-A2 to use the Automatic Sound Select function to switch from SAP to Stereo or Mono. The Automatic Sound Select function works well in mode 20_{hex} (Stereo ↔ Mono).

2. PAL-N Stereo Decoding Problem (A1, A2, A3)

In PAL-N, the PAL horizontal frequency ($f_h = 15.625$ kHz) is used to generate Pilot, Stereo, and SAP signals within an aural carrier at 4.5 MHz. In this system, the MSP versions A1, A2, and A3 are only able to decode Mono.

3. Startup Sequence Problems (A3)

If within 100 msec after reset of the MSP no short programming takes place, writing MODUS with AUTOMATIC ON (MODUS[0] = 1) partially resets the demodulator.

4. Stereo/SAP Detection Delay (A3)

In MSP34xxG-A3, the Stereo and SAP detection for BTSC starts with a delay of approximately 4 sec after changing the standard defined with the Short Programming command.

Later versions of the MSP have typical “Off” detection times of 200 ms. For increased robustness (see section 1.1. on page 1), the “On” detection time is increased to 600 ms.