CMOS 4-BIT MICROCONTROLLER

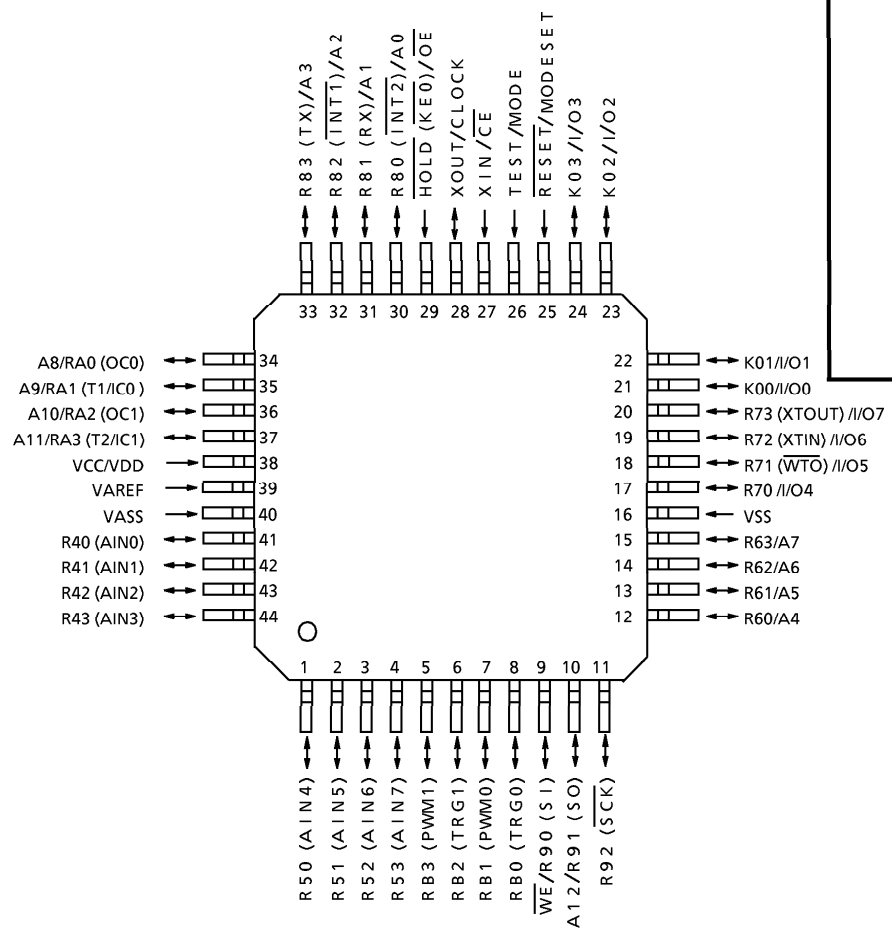
TMP47P885F

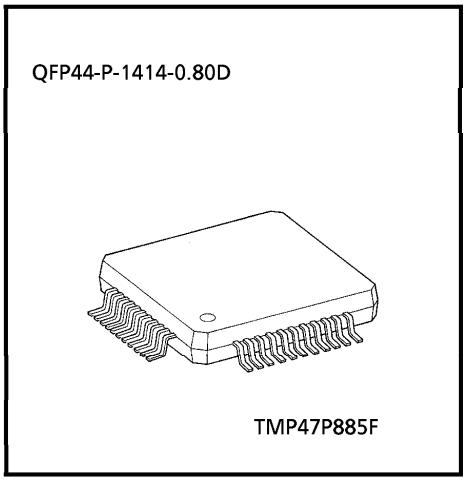
Designed for testing TMP47E885F-based systems, TMP47P885F is an LSI microcontroller with a built-in 8K-byte E²PROM as ROM. Using a PROM writer connecting adaptor socket, TMP47P885F can write/verify the same as MBM28C64.
TMP47P885F is pin-compatible with the mask-ROM TMP47E885F. The internal E²PROM of TMP47P885F can be programmed for the same operations as TMP47E885F.

PART No.	ROM	RAM	E²PROM	PACKAGE	ADAPTOR SOCKET
TMP47P885F	E²PROM 8192 × 8-bit	512 × 4-bit	64 × 8-bit	QFP44-P-1414-0.80D	BM1197

PIN ASSIGNMENT (TOPVIEW)

QFP44-P-1414-0.80D





980901EBP2

PIN FUNCTION

TMP47P885F supports MCU mode and E²PROM mode.

(1) MCU mode
This mode is pin-compatible with TMP47E885F. (Fix the TEST pin at low level.)

(2) E²PROM mode

PIN NAME	Input/Output	FUNCTION	Pin name (In MCU mode)
A12	Input	Program memory address input	R91
A11 to A8			RA3 to RA0
A7 to A4			R63 to R60
A3 to A0			R83 to R80
I/O7 to I/O4	Input/output	Program memory data input/output	R73 to R70
I/O3 to I/O0			K03 to K00
OE	Input	Output enable signal input	$\overline{\text{HOLD}}$
$\overline{\text{CE}}$		Chip enable signal input	XIN
$\overline{\text{WE}}$		Write enable signal input	R90
MODE	Input	E²PROM mode setting pin. Fix MODE at high level;	TEST
MODESET		MODESET at low level	$\overline{\text{RESET}}$
CLOCK	Input	External oscillator connecting pin	XOUT
VCC	Power supply	+ 5V	VDD
VSS		0V (GND)	VSS
R43 to R40	Input/output	For input processing, fix at low level.	
R53 to R50			
R92			
RB3 to RB0			
VAREF	Power supply	To protect ladder resistors, fix at VSS level.	
VASS			

OPERATIONAL DESCRIPTION

The following sections describe the hardware configuration and operation for TMP47P885F.
The internal mask ROM of TMP47E885F is used as E²PROM in TMP47P885F. Otherwise, structurally and functionally, TMP47P885F is identical to TMP47E885F.

1. Operating Mode

TMP47P885F supports MCU mode and E²PROM mode.

Mode \ Pin	MODE (TEST)	MODESET ($\overline{RESET}$)
MCU	L	*
E²PROM	H	L

L : 0V
H : 5V
* : don't care

Table 1-1. Operating Mode Setting

1.1 MCU Mode

Fixing the TEST pin at low level enters MCU mode.
The MCU mode operation is identical to TMP47E885F MCU mode operation. (As the TEST pin does not incorporate a pull-down resistor, TMP47P885F cannot be used with the TEST pin open.)

1.1.1 Program Memory

The program is stored in the same area as in TMP47E885F.

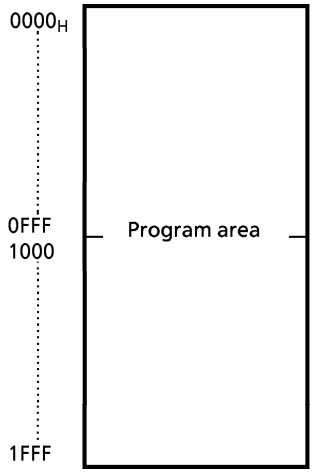


Figure 1-1. Program Area

1.1.2 Data Memory

TMP47P885F incorporates 512 x 4 bits of RAM data memory (equivalent to TMP47E885F).

1.1.3 Pin Input/Output Circuits

(1) Control pins
Apart from the TEST pin, which does not have a built-in pull-down resistor, all control pins are the same as those for TMP47E88F.

(2) Input/output ports
The input/output circuits for the I/O ports are the same as those for TMP47E885F.

1.2 E²PROM Mode (Used only for 8K byte E²PROM access)

Setting the MODE (TEST) pin to high level and the MODESET ($\overline{\text{RESET}}$) pin to low level enters E²PROM mode. Using a general-purpose PROM writer, in E²PROM mode data are written or verified. (Set the ROM type as equal to MBM28C64.)

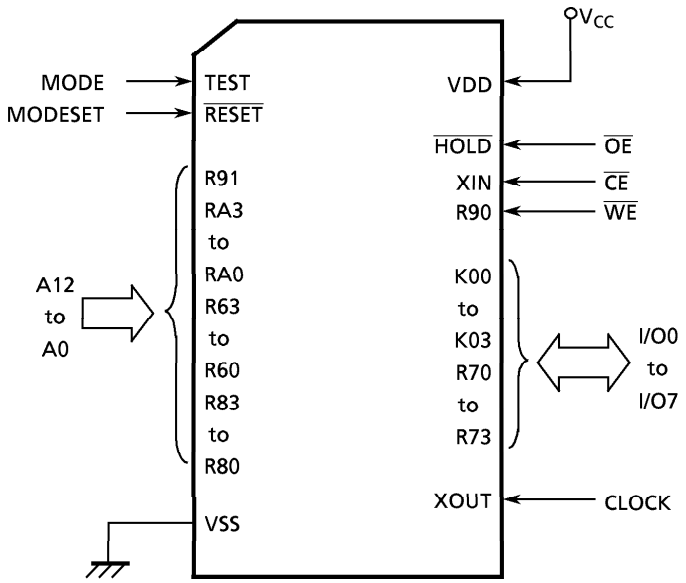


Figure 1-2. E²PROM Mode Settings

1.2.1 Operating Mode in E²PROM Mode

Mode \ Pin		$\overline{\text{CE}}$ (XIN)	$\overline{\text{OE}}$ ($\overline{\text{HOLD}}$)	$\overline{\text{WE}}$ (R90)	I/O	A	Operating state
Read	Data	L	L	H	D_{OUT}	Address	Operate
	Data polling				O7 = $\overline{\text{I7}}$, O0 to O6 = Hi-Z		Write
Standby		H	*	*	Hi-Z	*	Standby
Output disable		L	H	H			Operate
Write (single byte)		L	H	L	D_{IN}	Address	Write
Write inhibit (No.1)		*	L	*	—	—	—
Write inhibit (No.2)		*	*	H			
Batch	Write (all-byte)	L	HV	L	all L	*	Write
	Chip erase				all H		
	Security program				"FE_H"		

L : 0
H : 5V
HV : 12 to 15V
Hi-Z : High impedance
D_{IN} : Data input
D_{OUT} : Data output
* : don't care

Table 1-2. Operating Mode Settings (In E²PROM mode)

1.2.1.1 Read Mode ($\overline{CE}$ = $\overline{OE}$ = "L", $\overline{WE}$ = "H")

Setting the $\overline{CE}$ and $\overline{OE}$ pins to low level and the $\overline{WE}$ pin to high level enters read mode. Read mode has two functions: a data function to read internal data and a data polling function to detect termination of data write.

(1) Data function (Read data during normal operation)
When data are read during normal operation (except writing), the data at addresses specified by pins A0 to A12 are output to the I/O pins.

(2) Data polling function (Read data while writing data)
When data are read while writing data, the data being written ($\overline{I7}$) are output in inverted form to I/O pin 7. I/O pins 0 - 6 become high impedance.
This function enables detection of the termination of data write without using any additional external circuits.

Setting the $\overline{CE}$ or $\overline{OE}$ pin to high level sets the internal data bus and I/O pin to high impedance.

1.2.1.2 Standby Mode ($\overline{CE}$ = "H")

Setting the $\overline{CE}$ pin to high level enters standby mode. This mode disables the E^{2}PROM and sets the I/O pins to high level.

1.2.1.3 Output Disable Mode ($\overline{CE}$ = "L", $\overline{OE}$ = $\overline{WE}$ = "H")

Setting the $\overline{CE}$ pin to low level and the $\overline{OE}$ and $\overline{WE}$ pins to high level enters output disable mode. In this mode, E^{2}PROM operates but the I/O ports are at high impedance.

1.2.1.4 Write (Single Byte) Mode ($\overline{CE}$ = $\overline{WE}$ = "L", $\overline{OE}$ = "H")

Setting the $\overline{CE}$ and $\overline{WE}$ pins to low level and the $\overline{OE}$ pin to high level enters write (single byte) mode. In this mode, only a single byte of the I/O pin data is written to the address specified by pins A0 - A12. Address input is latched at the falling edge of pins $\overline{CE}$ or $\overline{WE}$. Conversely, data input is latched at the rising edge of pins $\overline{CE}$ or $\overline{WE}$. Therefore, there is no need to save the address or data during write. The write timing is determined by the timing for setting the $\overline{CE}$ or $\overline{WE}$ pin to low level ($\overline{CE}$ control or $\overline{WE}$ control).

(1) $\overline{CE}$ control
When the $\overline{OE}$ pin at high level and the $\overline{WE}$ pin at low level, set the $\overline{CE}$ pin to low level (data write at $\overline{CE}$ = L).

(2) $\overline{WE}$ control
When the $\overline{OE}$ pin at high level and the $\overline{CE}$ pin at low level, set the $\overline{WE}$ pin to low level (data write at $\overline{WE}$ = L).

1.2.1.5 Write (all-byte) function (No.1 : $\overline{OE}$ = "L", No.2 : $\overline{WE}$ = "H")

Setting the $\overline{OE}$ pin to low level enters write inhibit No.1 mode. Setting the $\overline{WE}$ pin to high level enters write inhibit No.2 mode. Data are not written in either of the write inhibit modes.

1.2.1.6 Batch Mode ($\overline{CE}$ = $\overline{WE}$ = "L", $\overline{OE}$ = "HV")

Setting the $\overline{CE}$ and $\overline{WE}$ pins to low level, and the $\overline{OE}$ pin to high voltage (12 - 15V) enters batch mode. Batch mode includes three functions: write (all-byte) function, chip erase function, which simultaneously erases all bytes, and security program function, which maintains data confidentiality by preventing data from being read after they are written.

(1) Write (all-byte) function (I/O0 to I/O7 = "L")
In batch mode, setting all the I/O pins set to low level and applying a low pulse to the $\overline{WE}$ pin writes all bytes at a time.

(2) Chip erase function (I/O0 to I/O7 = "H")
In batch mode, setting all the I/O pins set to high level and applying a low pulse to the $\overline{WE}$ pin erases all bytes at a time.

(3) Security program function (I/O0 to I/O7 = "FE_H")
In batch mode, applying a low pulse to the $\overline{WE}$ pin while outputting FE_H to the I/O pins disables subsequent data reads. After security program execution, only the chip erase function can be used. This function preserves data confidentiality.

1.2.2 E^2PROM Data Protection

E^2PROM has no data protection. To access the E^2PROM, set the registers of E^2PROM by the instruction. If TMP47P885F is operated out of the guaranteed range, data in the E^2PROM may be changed by the runaways of the CPU. Under the condition out of the guaranteed range, such as power on or power off, please use the power-on-reset circuit and reset IC to reset the MCU certainly.

1. After power on, keep active Reset until Vcc stabilized.
2. Do not power off during E^2PROM access.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER		SYMBOL	PIN	SPECIFICATION		UNIT
Power supply voltage		V_{DD}		– 0.3 to 6.5		V
Input voltage		V_{IN}		– 0.3 to V_{DD} + 0.3		V
Output voltage		V_{OUT1}	Ports R4, R5, R6, R7, R8, RA	– 0.3 to V_{DD} + 0.3		V
		V_{OUT2}	Ports R9, RB	– 0.3 to V_{DD} + 0.3		
Output current (per pin)		I_{OUT1}	Ports R4, R5, R6, R7, R8, RA	3.2		mA
		I_{OUT2}	Ports R9, RB (sink current)	3.2		
		I_{OUT3}	Ports R9, RB (source current)	1		
Output current (total for all pins)		ΣI_{OUT1}	Ports R4, R5, R6, R7, R8, RA	40		mA
		ΣI_{OUT2}	Ports R9, RB	20		
Power dissipation [Topr = + 85°C/ + 110°C]		PD		300		mW
Soldering temperature (time)		Tsld		260 (10s)		°C
Storage temperature		Tstg		– 55 to 150		°C
Operating temperature	Product version	Topr		T_L	T_H	°C
	Standard product			– 40	+ 85	

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, Topr = T_L to T_H)

PARAMETER	Symbol	PIN	CONDITION	Min.	Max.	UNIT
Power supply voltage	V_{DD}		At normal operation	4.5	5.5	V
			At slow operation	2.7		
			At hold operation	2.0		
High-level input voltage	V_{IH1}	Excluding hysteresis input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}	At slow and hold operations	$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Low-level input voltage	V_{IL1}	Excluding hysteresis input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}	At slow and hold operations	$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30	34	kHz

D.C. CHARACTERISTICS

(V_{SS} = 0V, Topr = T_L to T_H)

PARAMETER	SYMBOL	PINS	CONDITIONS		Min.	Typ.	Max.	UNIT
Hysteresis voltage	V_{HS}	Hysteresis Input			–	0.7	–	V
Input current	I_{IN1}	Ports $\overline{RESET}$, $\overline{HOLD}$, TEST, K0	V_{DD} = 5.5V, V_{IN} = 5.5V/0V		–	–	± 10	μA
	I_{IN2}	Ports R4 to RB						
resistance	R_{IN1}	$\overline{RESET}$			80	220	450	kΩ
	R_P	Ports R9, RB			3	10	35	
Output leak current	I_{LO}	Ports R4 to R8, RA	V_{DD} = 5.5V, V_{OUT} = 5.5V		–	–	+ 10	μA
High-level output voltage	V_{OH}	Ports R9, RB	V_{DD} = 4.5V, I_{OH} = – 60 μA		2.4	–	–	V
Low-level output voltage	V_{OL}	Ports R4 to RB	V_{DD} = 4.5V, I_{OL} = 1.6 mA		–	–	0.4	V
Low-level output current	I_{OL1}	Ports R4 to R8, RA	V_{DD} = 4.5V, V_{OL} = 1.0V		2.4	–	–	mA
	I_{OL2}	Ports R9, RB			2.4	–	–	
Power supply current at normal operation	I_{DD}	Except for E²PROM Erase / write	V_{DD} = 5.5V, fc = 4 MHz		–	3	6	mA
		During E²PROM Erase / write	V_{DD} = 5.5V, fc = 4 MHz		–	6	10	
Power supply current at slow operation	I_{DDS}		V_{DD} = 3.0V, fs = 32.768 kHz	Standard product	–	30	60	μA
Power supply current at hold operation	I_{DDH}		V_{DD} = 5.5V	Standard product	–	0.5	20	μA

Note 1 : Typ. values are based on Topr = 25 °C, V_{DD} = 5V

Note 2 : Input current : I_{IN1}, I_{IN2} : Excludes current due to built-in input (pull-up or pull-down) resistors.

Note 3 : Input current: I_{DD}, I_{DDH} : V_{IN} = 5.3V / 0.2V

Port R voltage level is assumed to be valid.

I_{DDS} : V_{IN} = 2.8V / 0.2V, low-frequency clock (XTIN, XTOUT connected) only oscillates.

A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5V to 5.5V, Topr = T_L to T_H)

PARAMETER	SYMBOL	CONDITIONS	Min.	Max.	UNIT
Instruction cycle time	t_{cy}	At normal operation	1.3	20	μs
		At slow operation	235	267	
High-level clock pulse width	t_{WCH}	External clock operation	80	–	ns
Low-level clock pulse width	t_{WCL}				
Reset pulse width	PW_{RSTL}	With stable oscillation	3	–	t_{cy}
External interrupt pulse width	PW_{EINT}		2	–	t_{cy}

A / D CONVERSION CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5V to 5.5V, Topr = T_L to T_H)

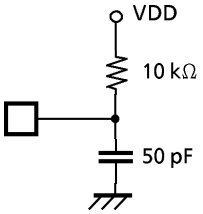
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Analog reference power supply voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog reference power supply voltage range	ΔV_{AREF}	V_{AREF} – V_{ASS}	2.5	–	–	V
Analog input voltage range	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog reference voltage power supply current	I_{REF}		–	0.5	1.0	mA
Non-linear error		V_{DD} = 5.0V, V_{SS} = 0.0V V_{AREF} = 5.000V V_{ASS} = 0.000V	–	–	± 1.5	LSB
Non-linear error			–	–	± 1.5	
Zero error			–	–	± 1.5	
Full-scale error			–	–	± 2	
Total error	t_{ADC}		–	26	–	t_{cy}
A/D conversion time	t_{AIN}	At fc = 4 MHz	–	4	–	μs

SIO CHARACTERISTICS

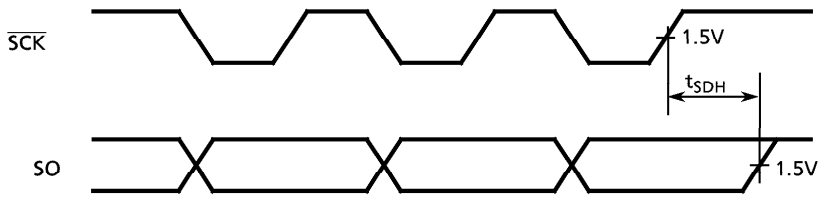
(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, Topr = T_L to T_H)

PARAMETER	SYMBOL	CONDITION	Min.	Max.	UNIT
Data transfer rate		When fc = 6 MHz, internal clock operates.	–	93750	bps
Shift data hold time	t_{SDH}		0.5 t_{cy} – 300	–	ns
External clock pulse width	PW_{SCKH}	External clock operates.	2	–	t_{cy}
	PW_{SCKL}				

Note : Shift data hold time :
$\overline{SCK}$, SO pin External circuit



Serial port (end of transmission)



TIMER/COUNTER CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, Topr = T_L to T_H)

PARAMETER	SYMBOL	CONDITION	Min.	Max.	UNIT
External count clock frequency	f_{CNT}	At normal operation	–	fc/16	Hz
		At slow operation	–	fs/16	
External input signal pulse width	PW_{TCIN}	At normal operation	4/fc	–	s
		At slow operation	4/fs	–	

PWM OUTPUT CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, Topr = T_L to T_H)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
PWM signal output frequency	f_{PWM}		–	–	fc/8192	Hz
Trigger signal input pulse width	PW_{TRG}		4/fc	–	–	s

64 byte E²PROM characteristics

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, Topr = T_L to T_H)

PARAMETER	SYMBOL	CONDITION		UNIT
Write time	t_{PW}		4.1 (Typ.)	ms
Erase time	t_{EW}		4.1 (Typ.)	ms
Number of overwrites		Topr = T_H	10^4 (Min.)	Times
Data hold characteristics		After executing 10^4 rewrites, Ta = 55 °C (average temperature)	10 (Min.)	Year

Note : Number of rewrites and data retention characteristics are intended as a guide to product capability.

D. C. CHARACTERISTICS (IN E²PROM MODE) (V_{SS} = 0V)

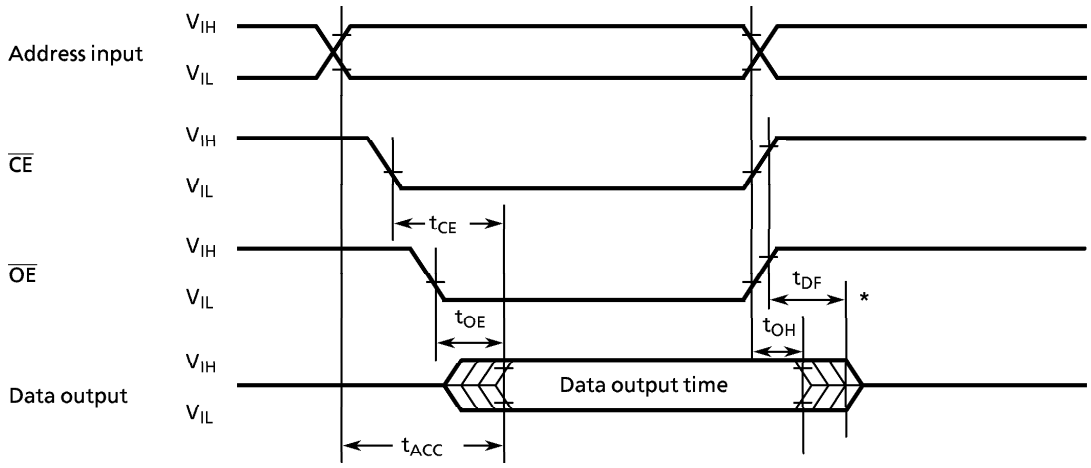
PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Input leak current	I_{LI}	TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{CC} = 5.5V, V_{IN} = 5.5V	– 10	–	10	μA
Output leak current	I_{LO}	Sink open drain port	V_{CC} = 5.5V, V_{OUT} = 5.5V	– 10	–	10	
V_{CC} power supply current (standby)	I_{SB1}		$\overline{CE}$ = V_{IH}, I/O = OPEN	–	0.2	1	mA
V_{CC} power supply current (standby)	I_{SB2}		$\overline{CE}$ = V_{CC} ± 0.3V, I/O = OPEN	–	10	100	μA
V_{CC} power supply current (operation)	I_{CC1}		$\overline{CE}$ = V_{IL}, I/O = OPEN	–	20	30	mA
V_{CC} power supply current (operation)	I_{CC2}		Cycle = Min., I/O = OPEN	–	20	30	
V_{CC} power supply current (write)	I_{CCW}		$\overline{WE}$ = ⌝⌟, $\overline{CE}$ = V_{IL}	–	20	30	
High-level input voltage	V_{IH}		V_{CC} = 4.5~5.5V	V_{CC}×0.7	–	V_{CC}+0.3	V
Low-level input voltage	V_{IL}		V_{CC} = 4.5~5.5V	– 0.1	–	V_{CC}×0.3	
High-level output voltage	V_{OH}		I_{OH} = – 400μA, V_{CC} = 4.5V	2.4	–	–	
Low-level output voltage	V_{OL}	Excluding XOUT	I_{OL} = 2.1mA	–	–	0.45	
Program inhibit V_{CC} voltage	V_{INH}			2.0	–	–	
Output enable pin voltage at chip erase	V_{OE}		V_{CC} = 4.5V~5.5V	12	–	15	
V_{CC} power supply current at chip erase	I_{CCE}		$\overline{OE}$ = V_{OE}, $\overline{CE}$ = $\overline{WE}$ = V_{IL}	–	–	60	mA
High potential detect input voltage	V_{IHP}		V_{CC} = 4.5V to 5.5V	8.0	–	–	V

A. C characteristics (In E²PROM mode) (V_{SS} = 0V, V_{DD} = 4.5 to 5.5V)

(1) Read Cycle

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address access time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	–	350	ns
From $\overline{CE}$ = L to data output	t_{CE}	$\overline{OE}$ = V_{IL}	–	–	350	
From $\overline{OE}$ = L to data output	t_{OE}	$\overline{CE}$ = V_{IL}	–	–	120	
From $\overline{CE}$ = H or $\overline{OE}$ = H to output floating	t_{DF}	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}	–	–	60	
Previous cycle data output hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	–	

(Timing chart) ($\overline{WE}$ = "H")



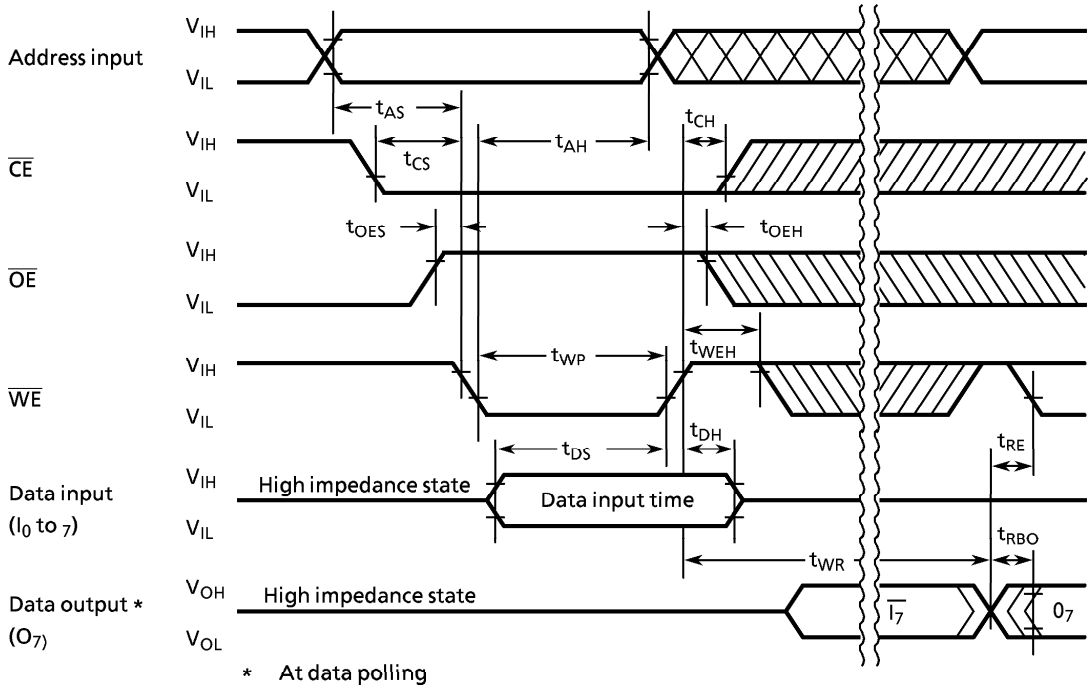
* t_{DF} is determined by whichever of the rising edges of $\overline{OE}$ or $\overline{CE}$ is faster. The level is determined when the output becomes high impedance.

(2) Write cycle (single byte)

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT
Address set-up time	t_{AS}	20	–	–	ns
Write set-up time	t_{CS}	0	–	–	
$\overline{OE}$ set-up time	t_{OES}	20	–	–	
Write pulse width	t_{WP}	100	–	–	
Address hold time	t_{AH}	50	–	–	
Data set-up time	t_{DS}	50	–	–	
Data hold time	t_{DH}	20	–	–	
Write hold time	t_{CH}	0	–	–	
$\overline{OE}$ hold time	t_{OEH}	20	–	–	
Write time	t_{WR}	–	–	10	ms
Write recover time	t_{RE}	50	–	–	ns
From program termination to output	t_{RBO}	–	–	100	
$\overline{WE}$ hold time	t_{WEH}	10	–	–	ns

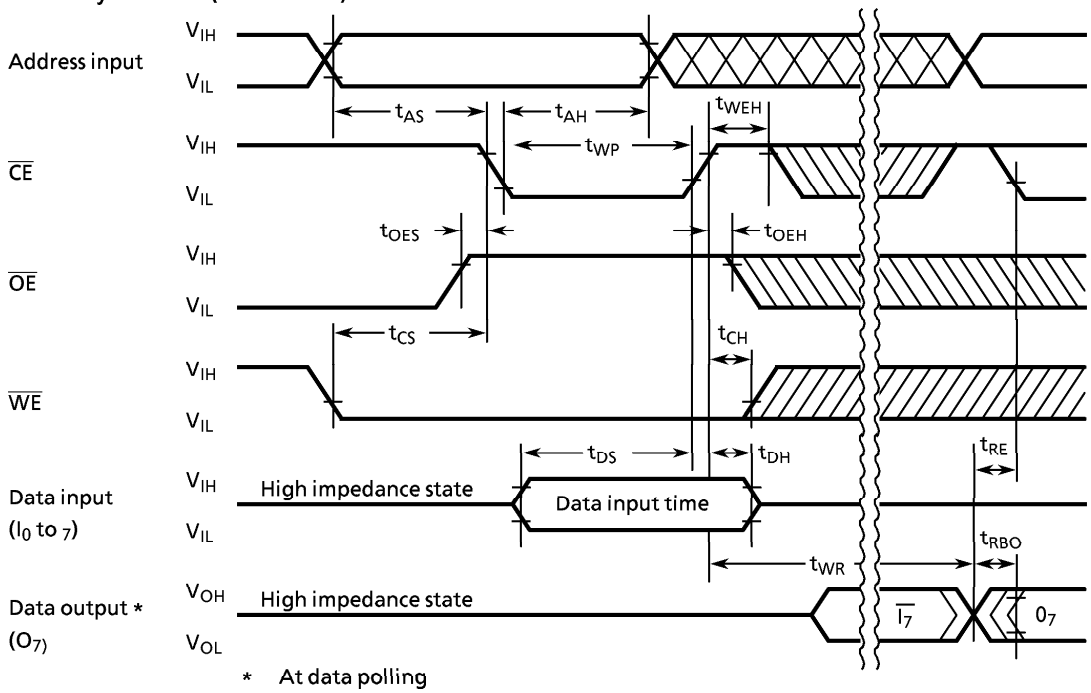
(Timing chart)

1. Write cycle No.1 ($\overline{WE}$ control)



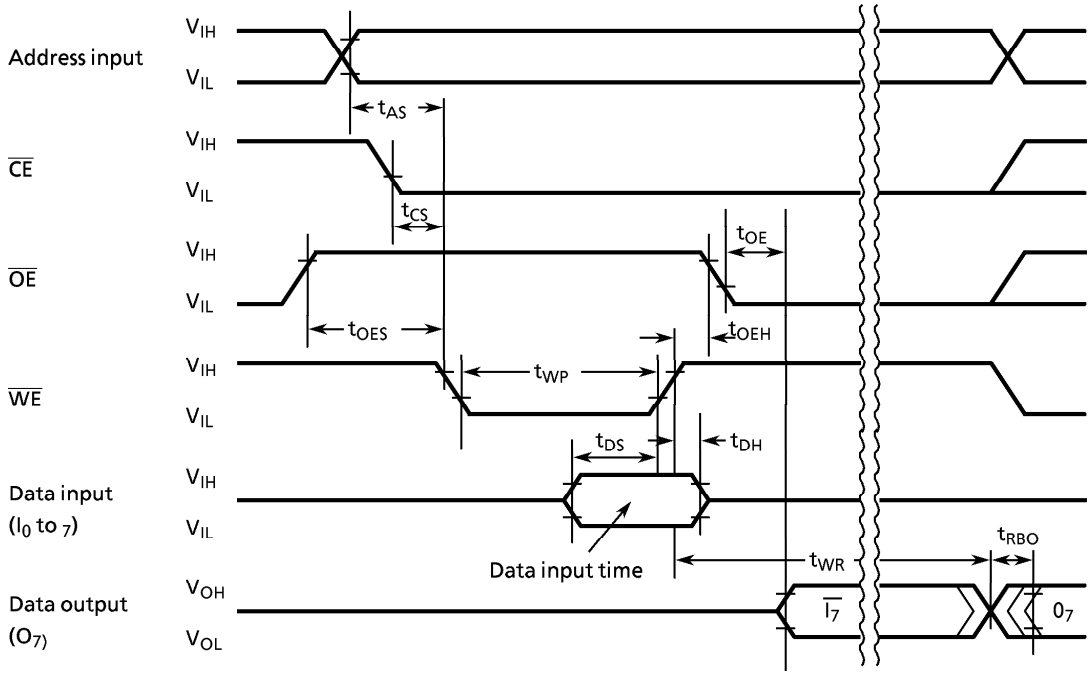
* At data polling

2. Write cycle No.2 ($\overline{CE}$ control)



* At data polling

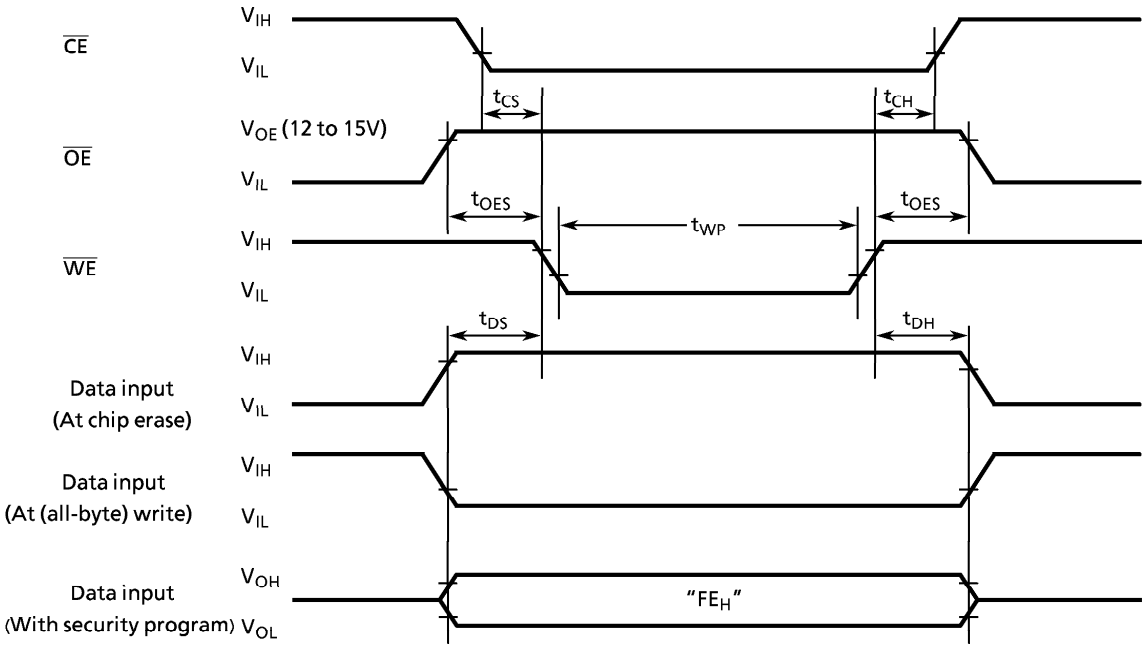
3. Data Polling



(3) Chip erase/write (all-byte)/ security program cycle

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT
Write set-up time	t_{CS}	150	–	–	ns
$\overline{OE}$ set-up time	t_{OES}	150	–	–	
Data set-up time	t_{DS}	150	–	–	
Data hold time	t_{DH}	100	–	–	
Write pulse width	t_{WP}	5	–	20	ms
Write hold time	t_{CH}	100	–	–	ns
$\overline{OE}$ hold time	t_{OEH}	100	–	–	

(Timing Chart)



CAUTIONS

TMP47E885F and TMP47P885F are covered by a patent agreement between Toshiba Corporation and Bull CP8. These products cannot be used with IC cards and other portable devices (as defined below).

"PORTABLE DEVICE"

(I) A portable piece of equipment with a length or breadth ±10 mm, and a thickness ±3 mm of the dimensions defined under ISO standard 7816, or

(II) A portable device conforming to the electrical connection layout and shape specified under ISO standard 7816, part 2, or

(III) A portable and pocket-size device for the identification of the carrier of the device or of the device itself, and for the accumulation of information relating to the carrier of the device or the device itself.