

DESCRIPTION

The HYM539400 is a 4M x 39-bit Fast page mode CMOS DRAM module consisting of ten HY5116400 in 24/28 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM. The HYM539400MG/ LMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- Low power dissipation

Max. battery back-up 33.0mW (L-part)

Max. CMOS standby 22.0mW (L-part)

55.0mW

Max. TTL standby 110.0mW

Max. operating

Speed	Power
60	4.95W
70	4.40W
80	3.85W

- Single power supply of 5V $\pm$ 10%

- TTL compatible inputs and outputs

- Fast access time

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	18ns	45ns
80	80ns	20ns	50ns

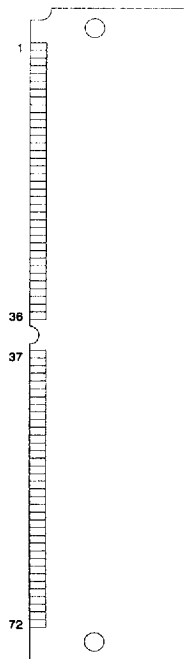
- Fast page mode operation

- CAS-before-RAS, RAS-only, Hidden refresh

- 4096 refresh cycles / 256ms (L-part)

4096 refresh cycles / 64ms

PIN CONNECTION



PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Out Enable
A0-A11*	Address Input
DQ0-DQ38	Data Input/Output
PD1-PD4	Presence Detect
VCC	Power (+ 5V)
VSS	Ground

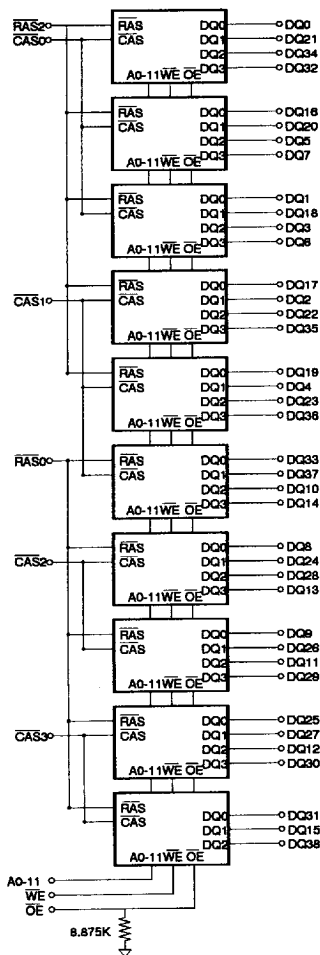
*A10 and A11 are applied to row address input only.

NOT AVAILABLE

PIN NAME

#	NAME	#	NAME
1	VSS	37	DQ33
2	DQ0	38	DQ35
3	DQ16	39	VSS
4	DQ1	40	CAS0
5	DQ17	41	CAS2
6	DQ2	42	CAS3
7	DQ18	43	CAS1
8	DQ3	44	RAS0
9	DQ19	45	NC
10	VCC	46	DQ37
11	A10	47	WE
12	A0	48	VSS
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	OE	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	VCC
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	DQ36	65	DQ15
30	VCC	66	DQ38
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	RAS2	70	PD4
35	DQ34	71	A11
36	DQ32	72	VSS

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-70
PD1	NC
PD2	NC
PD3	VSS
PD4	VSS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	7.0	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC + 1.0, All other pins not under test = VSS		-100	100	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trC = trC (min.)	60 70 80	- - -	900 800 700	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	20	mA	
ICC3	VCC Supply Current, RAS-only refresh	trC = trC (min.)	60 70 80	- - -	900 800 700	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tPC = tPC (min.)	60 70 80	- - -	700 600 500	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V	L-part	- -	10 4	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	trC = trC (min.)	60 70 80	- - -	900 800 700	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	trC = 62.5μs, CAS = CBR cycling or 0.2V OE & WE = VCC - 0.2V A0-A11 = VCC - 0.2V or 0.2V DQ0-DQ39 = VCC - 0.2V, 0.2V, or open	trAS ≤ 300ns trAS ≤ 1μs	- -	3.5 6.0	mA	1,4,5
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = VIL and CAS = VIH.
4. Only trAS(max.) = 1μs is applied to refresh of battery backup but trAS(max.) = 10μs is applied to normal functional operation.
5. ICC5(max.) = 4.0mA and ICC7 are applied to L-part only (HYM539400LMG).

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM539400MG/LMG						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	180	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	85	-	95	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	18	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRAS _P	RAS Pulse Width (Fast Page Mode)	60	400K	70	400K	80	400K	ns	
15	tRSH	RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	15	10K	18	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	52	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	45	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (4096 cycles)	-	64	-	64	-	64	ms	
		L-part	-	256	-	256	-	256		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

Continued

#	SYMBOL	PARAMETER	HYM539400MG/LMG						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	40	-	45	-	45	-	ns	8
42	tRWD	RAS to WE Delay Time	85	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	55	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	15	-	15	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	15	-	15	-	ns	
49	tOEA	OE Access Time	0	15	0	18	0	20	ns	
50	tOED	OE to Data Delay	15	-	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	15	ns	
52	tOEH	OE Command Hold Time	15	-	15	-	15	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	60	-	65	-	70	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	35	-	40	-	45	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition time is measured between VIH and VIL and assumed to be 5ns for all inputs.
3. Refer to the HY5116400 data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. tOFF(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. twCS is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twCS $\geq$ twCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.) = 256ms is applied to L-part only (HYM539400LMG).

CAPACITANCE

(TA = 25°C, VCC = 5V $\pm$ 10%, VSS = 0V, f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A11)	-	70	pF
CIN2	Input Capacitance (WE, OE)	-	80	pF
CIN3	Input Capacitance (RAS)	-	40	pF
CIN4	Input Capacitance (CAS)	-	24	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ38)	-	17	pF

The timing diagram illustrates the relationship between several control and data signals over time. The signals shown are RAS, CAS, ADDR, WE, OE, and DQ. The diagram includes various timing parameters such as t_{RAS} , t_{RCD} , t_{RSH} , t_{ICRP} , t_{ICSH} , t_{ICAS} , t_{ICRP} , t_{IAR} , t_{IRAD} , t_{IRAH} , t_{IASC} , t_{ICAH} , t_{IRAL} , t_{IASR} , t_{ICWL} , t_{IRWL} , t_{IWP} , t_{IOEH} , t_{IOED} , t_{PD} , t_{DH} , and t_{CRP} . The signals are shown as digital waveforms, with some signals like ADDR, WE, and OE having shaded regions indicating specific states or delays.

[illegible]

The timing diagram illustrates the relationship between the 28C010A device and its memory array. The signals shown are:

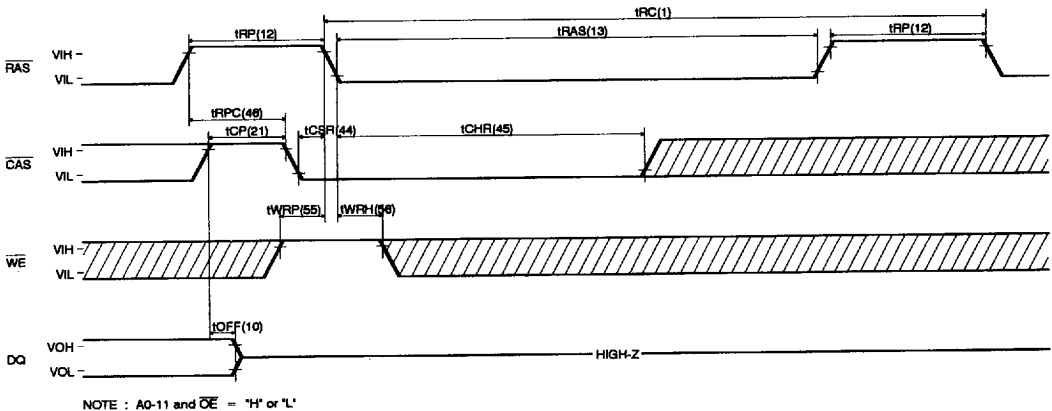
- RAS:** Row Address Strobe. Timing parameters include $t_{RASP}(14)$, $t_{ICPD}(20)$, $t_{ICSH}(18)$, $t_{ICPD}(21)$, $t_{ICPD}(21)$, $t_{ICPD}(20)$, and $t_{ICPD}(20)$.
- CAS:** Column Address Strobe. Timing parameters include $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, and $t_{ICPD}(20)$.
- ADDR:** Address. Timing parameters include $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, and $t_{ICPD}(20)$.
- WE:** Write Enable. Timing parameters include $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, and $t_{ICPD}(20)$.
- OE:** Output Enable. Timing parameters include $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, and $t_{ICPD}(20)$.
- DQ:** Data bus. Timing parameters include $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, $t_{ICPD}(20)$, and $t_{ICPD}(20)$.

The diagram shows the sequence of operations: RAS and CAS are active low pulses. ADDR is active low and contains ROW and COLUMN information. WE is active low and indicates write operations. OE is active low and indicates read operations. The data bus (DQ) shows the data being transferred between the device and the memory array.

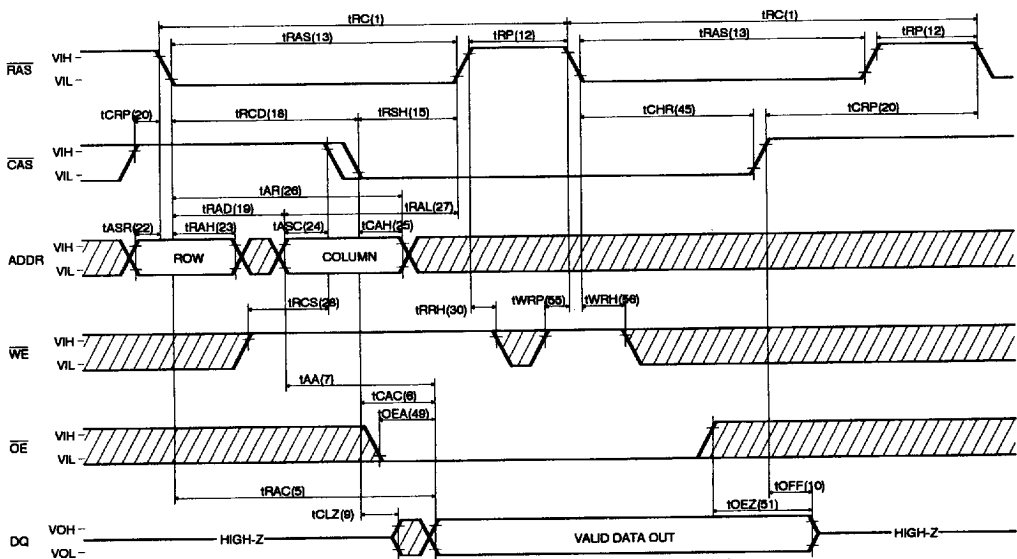
The timing diagram illustrates the relationship between RAS, CAS, and ADDR signals. RAS is active low, with parameters $t_{RC}(1)$, $t_{RAS}(13)$, and $t_{RP}(12)$. CAS is active low, with parameters $t_{CRP}(20)$ and $t_{RPC}(46)$. ADDR is active low, with parameters $t_{ASR}(22)$ and $t_{RAH}(23)$. The diagram shows the sequence of events for a memory access, including the period when RAS is high and CAS is low, and the period when both are high.

NOTE : $\overline{OE}$ and $\overline{WE}$ = 'H' or 'L'

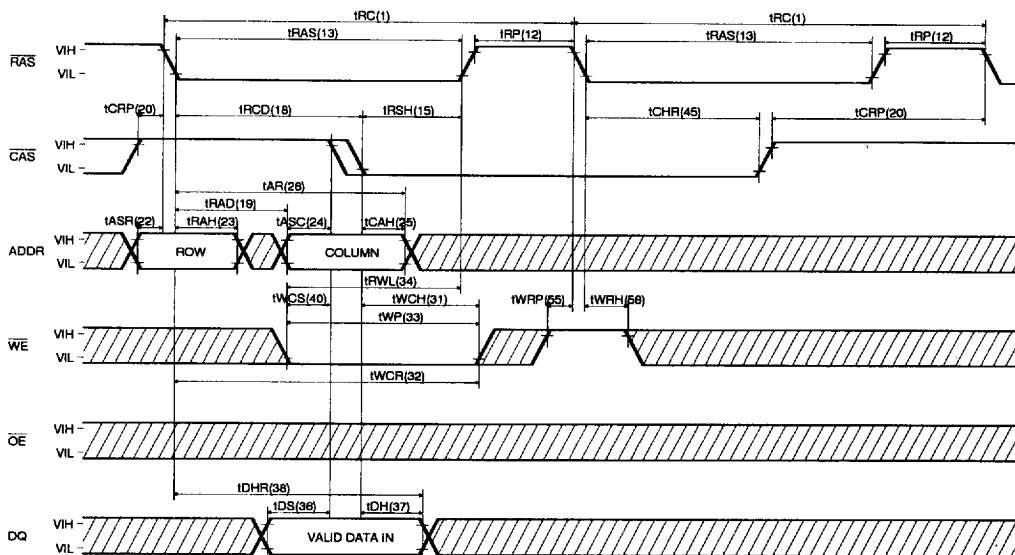
CAS-BEFORE-RAS REFRESH CYCLE



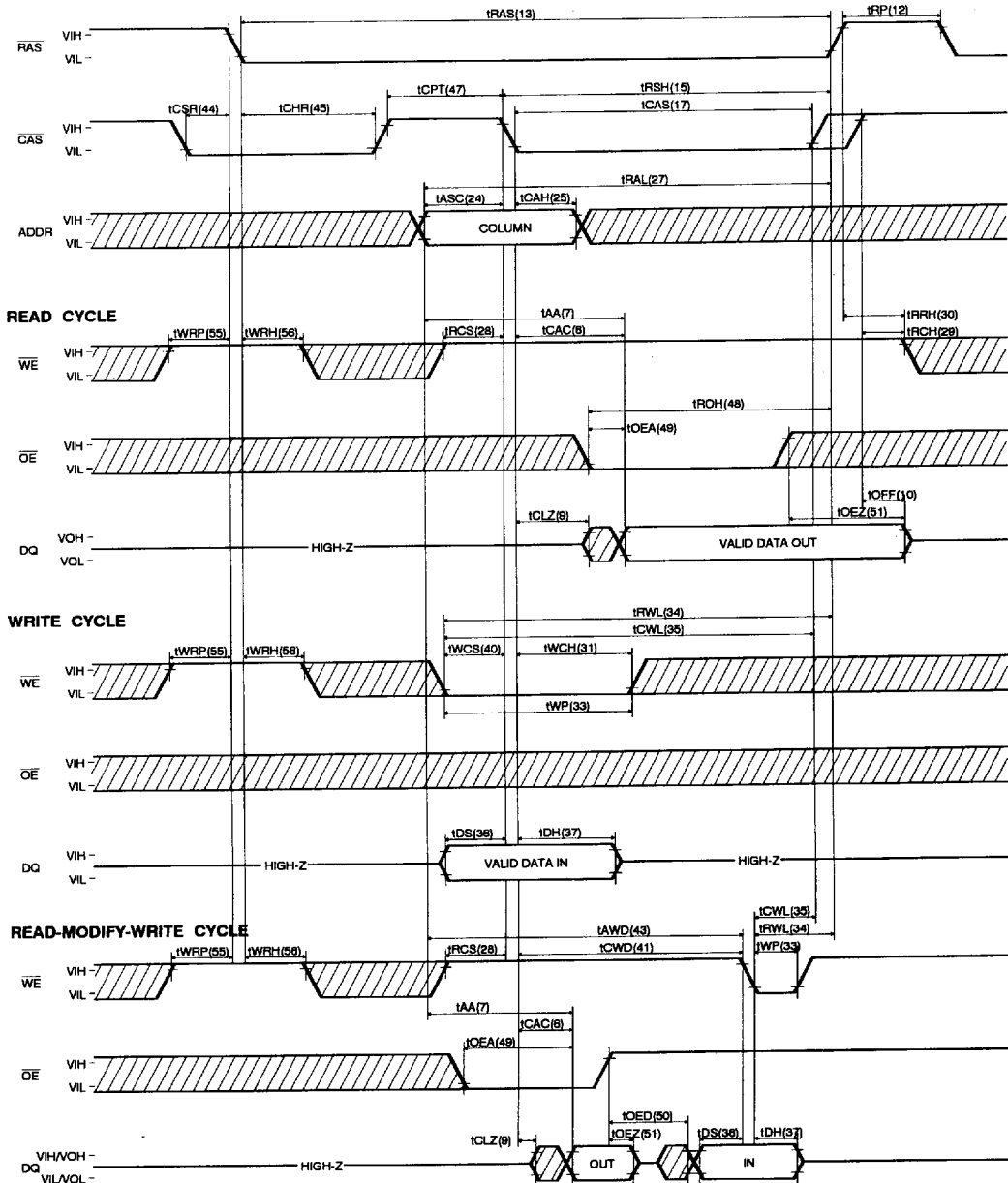
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

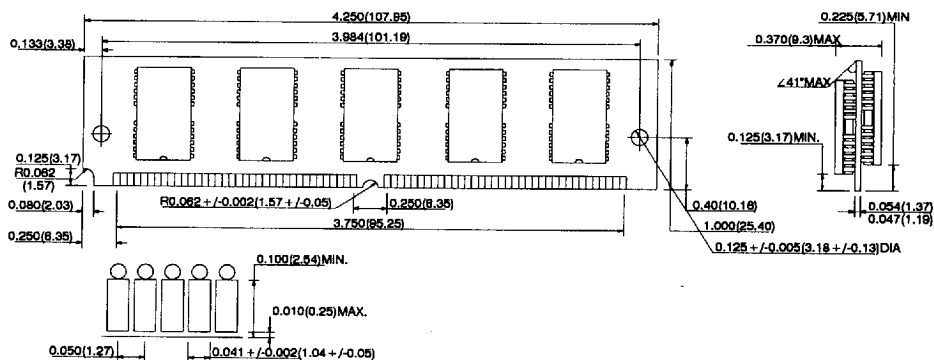


PACKAGE INFORMATION

72 pin Single In-line Memory Module (MG ; Gold plated)

HYM539400MG (SOJ mounted)

UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE	PLATING
HYM539400MG	6070/80		SIMM	Gold
HYM539400LMG	60/70/80	L-part	SIMM	Gold