REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
E	Change to military drawing format. Add two new device types. Add vendor CAGE 61394. Add vendor for device types 01 and 02 in DIP only.	1987 JUN 29	M.A. Frye
F	Add the Z package to device types 08 and 09. Add vendor CAGE 61394 to devices 01ZX, 02ZX, 08ZX and 09ZX. Deleted vendor similar part number AM27128-45/BUA from devices 01ZX and 02ZX in paragraph 6.4. Changes to table I and table II. Also changes to recommended operating conditions and figure 2. Editorial changes throughout.	1988 NOV 01	M.A. Frye

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	F	E																						
SHEET	22	23																						

REV STATUS OF SHEETS	REV	F	F	F	F	F	F	E	F	F	E	F	E	E	E	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY James E. Jamison

CHECKED BY Ray Monnin

APPROVED BY M.A. Frye

DRAWING APPROVAL DATE
11 OCTOVER 1983

REVISION LEVEL
F

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, 131, 072(16K X 8), UVE PROM

SIZE	CAGE CODE	
A	14933	82025

SHEET 1 OF 23

DESC FORM 193-1
SEP 87

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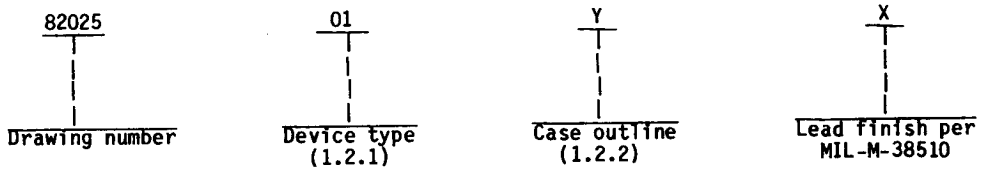
5962-E1036

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access	Program method
01	(see 6.4)	16,384 x 8 - Bit UV EPROM	450 ns	C
02	(see 6.4)	16,384 x 8 - Bit UV EPROM	250 ns	C
03	(see 6.4)	16,384 x 8 - Bit UV EPROM	200 ns	B
04	(see 6.4)	16,384 x 8 - Bit UV EPROM	300 ns	B
05	(see 6.4)	16,384 x 8 - Bit UV EPROM	250 ns	B
06	(see 6.4)	16,384 x 8 - Bit UV EPROM	150 ns	B
07	(see 6.4)	16,384 x 8 - Bit UV EPROM	110 ns	B
08	(see 6.4)	16,384 x 8 - Bit UV EPROM	200 ns	C
09	(see 6.4)	16,384 x 8 - Bit UV EPROM	300 ns	C

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline 1/
Y	D-10 (28-pin, 1.490" x .610" x .232"), dual-in-line package
Z	C-12 (32-terminal, .560" x 458" x .120"), rectangular chip carrier package

1.3 Absolute maximum ratings. 2/

Supply voltage (V_{CC}):	
Device types 01, 02, 08, 09	-0.3 V dc to +7.0 V dc
Device types 03 - 07	-0.6 V dc to +6.0 V dc ±.25 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation, (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J):	
Device types 01, 02, 08, 09	+175°C
Device types 03 - 07	+150°C
Thermal resistance, junction-to-case (O_{JC})	See MIL-M-38510, appendix C
All input or output voltages with respect to ground (device types 03 - 07)	-0.6 V dc to +6.25 V dc
Input voltage range:	
Device types 01, 02, 08, 09	-0.3 V dc to +7.0 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ All voltages referenced to V_{SS}.

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Input low voltage (V_{IL})	-0.1 V dc to 0.8 V dc
Input high voltage (V_{IH})	2.0 to V_{CC} +1
Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level program input voltage $V_{IN(PR)}$	21.0 V dc ±.5 V dc (program method A and C)
High level program input voltage $V_{IN(PR)}$	12.5 V dc ±.5 V dc (program method B)

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard, required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables.

3.2.2.1 Unprogrammed or erased devices. The truths table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$, unless otherwise specified		Group A subgroups	Device types	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_{OH} = -400 µA	V_{CC} = 4.5 V	1, 2, 3	01, 02, 08, 09	2.4		V
			V_{CC} = 5.25 V		03 - 07			
Low level output voltage	V_{OH}	I_{OL} = 2.1 mA	V_{CC} = 5.5 V	1, 2, 3	01, 02, 08, 09		0.4	V
			V_{CC} = 5.25 V		03 - 07		0.45	
Output leakage current (high)	I_{OH}	V_{CC} = 5.5 V 1/ V_{OUT} = 5.5 V		1, 2, 3	01, 02, 08, 09		10	µA
					03 - 07	-10	10	
Output leakage current (low)	I_{OL}	V_{CC} = 5.5 V 1/ V_{OUT} = 0.1 V		1, 2, 3	01, 02, 08, 09		10	µA
High level input current	I_{IH}	V_{IN} = 5.5 V	V_{CC} = 5.5 V	1, 2, 3	01, 02, 08, 09		1	µA
			Outputs deselected V_{CC} = 5.25 V 2/		03 - 07		10	
Low level input current	I_{IL}		V_{CC} = 5.5 V V_{IN} = 0.1 V	1, 2, 3	01, 02, 08, 09		1	µA
			Outputs deselected V_{CC} = 5.25 V V_{IN} = 0.4 V 2/		03 - 07		-10	
V_{pp} read voltage	V_{pp}			1, 2, 3	01, 02, 08, 09	V_{CC} -0.7	V_{CC} +1	V
Input voltage low	V_{IL}	V_{CC} = 5.5 V 3/		1, 2, 3	01, 02, 08, 09	-.1	0.8	V
Input voltage high	V_{IH}	V_{CC} = 4.5 V 3/		1, 2, 3	01, 02, 08, 09	2.0	6.5	V
V_{pp} supply current read/standby 4/	Ipp	V_{pp} = 5.5 V		1, 2, 3	All		5	mA
Supply current (standby)	I_{SB}	Outputs open $\overline{CE}$ = V_{IH}	V_{CC} = 5.5 V	1, 2, 3	01, 02, 08, 09		50	mA
			V_{CC} = 5.25 V		03 - 07			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$, unless otherwise specified		Group A subgroups	Device types	Limits Min	Limits Max	Unit
Supply current 2/	I_{CC}	Outputs open	V_{CC} = 5.5 V	1, 2, 3	01, 02, 08, 09		150	mA
		$\overline{OE}$ = $\overline{CE}$ = V_{IL}	V_{CC} = 5.25 V		03, 04, 05		140	
Input capacitance 2/ 5/	C_I	V_{IN} = 0 V, f = 1 MHz, T_C = +25°C		4	All		6	pF
Output capacitance 5/	C_O	V_{OUT} = 0 V, f = 1 MHz, T_C = +25°C		4	All		12	pF
Address access time	t_{AVQV}	2/ 6/ V_{CC} = 5.25 V, See figure 5	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	9, 10, 11	01		450	ns
					02,05		250	
					03,08		200	
					04,09		300	
					06		150	
					07		110	
Output enable to high Z	t_{DF} 7/		$\overline{CE}$ = V_{IL}	9, 10, 11	01		130	ns
					02,08, 09		90	
					03		65	
					04		80	
					05		65	
					06		55	
					07		45	
Output hold from address change	t_{OH} 7/		$\overline{CE}$ = $\overline{OE}$ = V_{IL}	9, 10, 11	All	0		ns
Chip enable access time	t_{ELQV}		$\overline{OE}$ = V_{IL}	9, 10, 11	01		450	ns
					02,05		250	
					03,08		200	
					04,09		300	
					06		150	
					07		125	
Output enable data on time	t_{OLQV}		$\overline{CE}$ = V_{IL}	9, 10, 11	01		150	ns
					02,05		100	
					03		85	
					04		110	
					06		65	
					07		55	

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OL} and I_{OH} with the output under test connected to V_{OUT}.
2/ Outputs shall be loaded in accordance with figure 4.
3/ Tests for all input and control pins.
4/ V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.
5/ All pins not being tested are to be grounded.

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6/ Equivalent ac test conditions (actual load condition vary by tester).
Output load: 1 TTL gate and C_L = 100 pF.
Input rise and fall times < 20 ns.
Input pulse levels: 0.4 V and 2.4 V.
Timing measurement reference levels:
Inputs = 1 V and 2 V.
Outputs = 0.8 V and 2 V.

7/ AC testing enable to three-state shall be tested initially and after any design changes.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.5.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and 4.6 and tables III, IV, and V.

3.5.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2).

(2) Bake, unbiased, for 12 hours at +200°C.

(3) Perform a margin test using $V_m = V_{CC}$ = 6.0 V at +25°C using loose timing.

(4) Erase device, then program 45 percent to 50 percent of the bits to a worst case speed pattern.

(5) Perform dynamic burn-in (see 4.2a).

(6) Perform a margin test using $V_m = V_{CC}$ = 6.0 V at +25°C.

(7) Perform 100 percent electrical testing at +125°C, +25°C, and -55°C.

(8) Erase device (see 3.5.1), except devices submitted for groups A, B, C, and D testing.

(9) Verify erasure (see 3.5.3).

Margin test method B

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.5.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = +6.0 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_m = 6.0 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.5.1), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.5.3).

Margin test method C

(1) Program, at +25°C, greater than 95 percent pattern (ex. diagonal "1's) (see 3.5.2).

(2) Bake, unbiased, for 8 hours at +200°C or 24 hours at +170°C or 72 hours at +150°C.

(3) Test at +95°C (see 3.5.3), including a margin test at V_m = +6 V and loose timing (i.e., t_{ACC} = 1 µs).

(4) Erase (see 3.5.1).

(5) Program at +25°C with a 50 percent pattern (ex. checkerboard bar) (see 3.5.2). (programmed with checkerboard at wafer sort).

(6) Test at +125°C (see 3.5.3).

(7) Burn-in (see 4.2a).

(8) Test at +125°C (see 3.5.3).

(9) Test at -55°C (see 3.5.3).

(10) Erase (see 3.5.1). Devices may be submitted for groups A, B, C, and D testing at this point.

(11) Verify erasure at +25°C (see 3.5.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity times exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the Model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch away from the lamp tubes. After erasure, all bits are in the high state.

4.5 Programming procedure for methods A and C. The programming characteristics in tables III and V and the following procedure shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 6, and programming characteristics of tables III and V shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

c. Programming occurs when Vpp is 21.0 V ±0.5 V, and chip enable and $\overline{PGM}$ are brought low.

4.6 Programming procedure for method B. The programming characteristics in table IV and the following procedure shall be used for programming the device.

a. Connect the device in the electrical configuration for programming the waveforms of figure 7, and programming characteristics of table IV shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4).

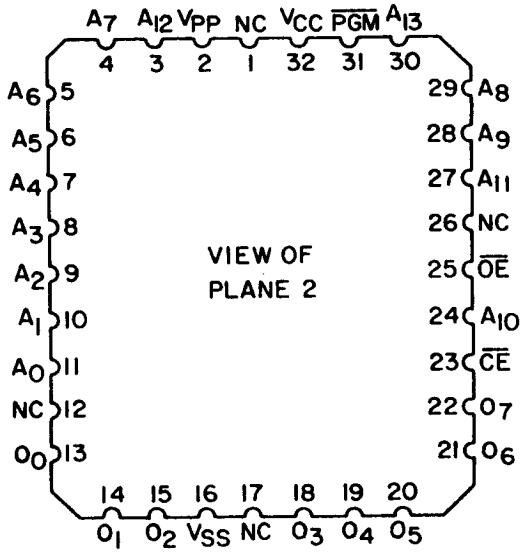
c. Programming occurs when Vpp is 12.5 V ±0.5 V, and chip enable and $\overline{PGM}$ are brought low.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(Hot), 10

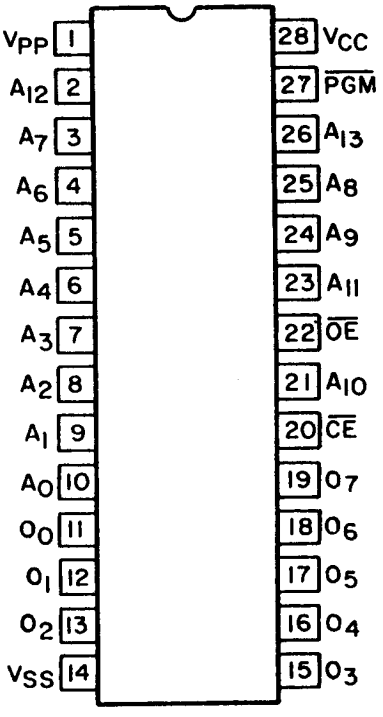
NOTES:
1. (*) indicates PDA applies to subgroup 1 (see 4.2).
2. Any or all subgroups may be combined when when using a high speed tester.
3. Subgroups 7 and 8 shall consist of verifying the pattern specified.
4. For all electrical tests, the device shall be programmed to the pattern specified.

CASE Z



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

CASE Y



Pin Names

A_0-A_{13}	Addresses
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
O_{0-7}	Outputs
$\overline{PGM}$	Program Pin

FIGURE 1. Terminal connections.

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Device types 03 through 07

Mode/pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_q	V_{PP}	V_{CC}	Outputs
Programming method	B	B	B	B	B	B	B
Outside disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program inhibit	V_{IL}	X	X	X	V_{PP}	V_{CC}	High Z
Program verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{OUT}
Intelligent identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code
Intelligent programming	V_{IL}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{IN}

NOTES:
1. It is recommended that verification for method B devices be performed after the completion of programming all bytes.
2. X means the input is a "don't care".
3. Using the intelligent programming algorithm (method B) allows the device to be programmed in a faster time.
4. V_H = 12 V ±0.5 V.

Device types 01, 02, 08, and 09

Mode/pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Outside disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon signature* (intelligent identifier)	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded data

NOTES:
1. X can be either V_{IL} or V_{IH}.
2. *For silicon signature (tm) (intelligent identifier) A0 is toggled. A9 = 12 ±0.5 V, and all other addresses are at TTL low (V_{IL}).

FIGURE 2. Truth tables for unprogrammed devices.

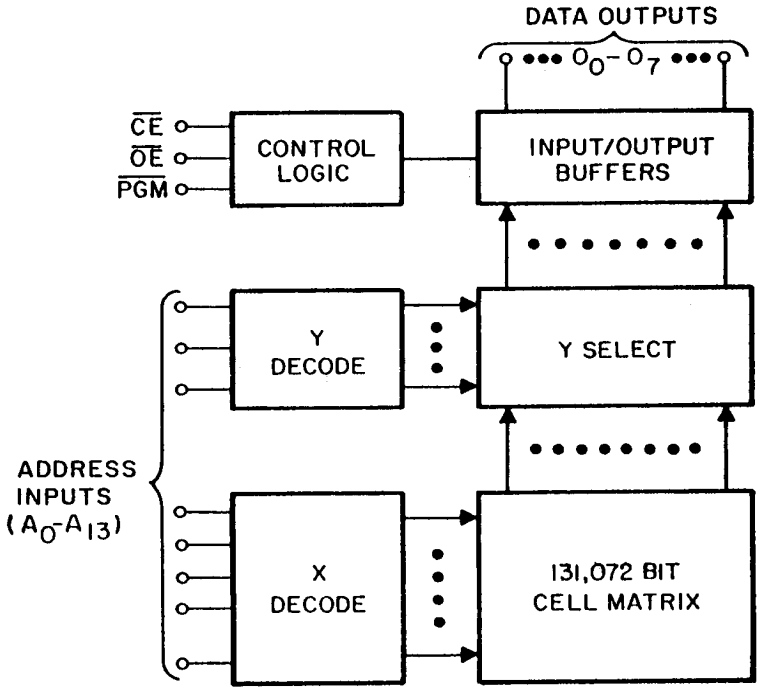


FIGURE 3. Logic diagram.

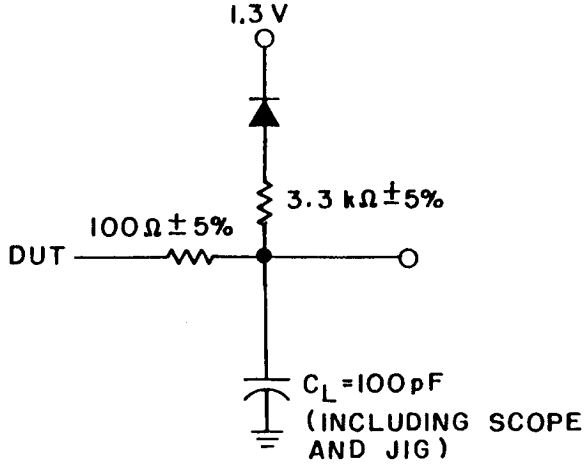
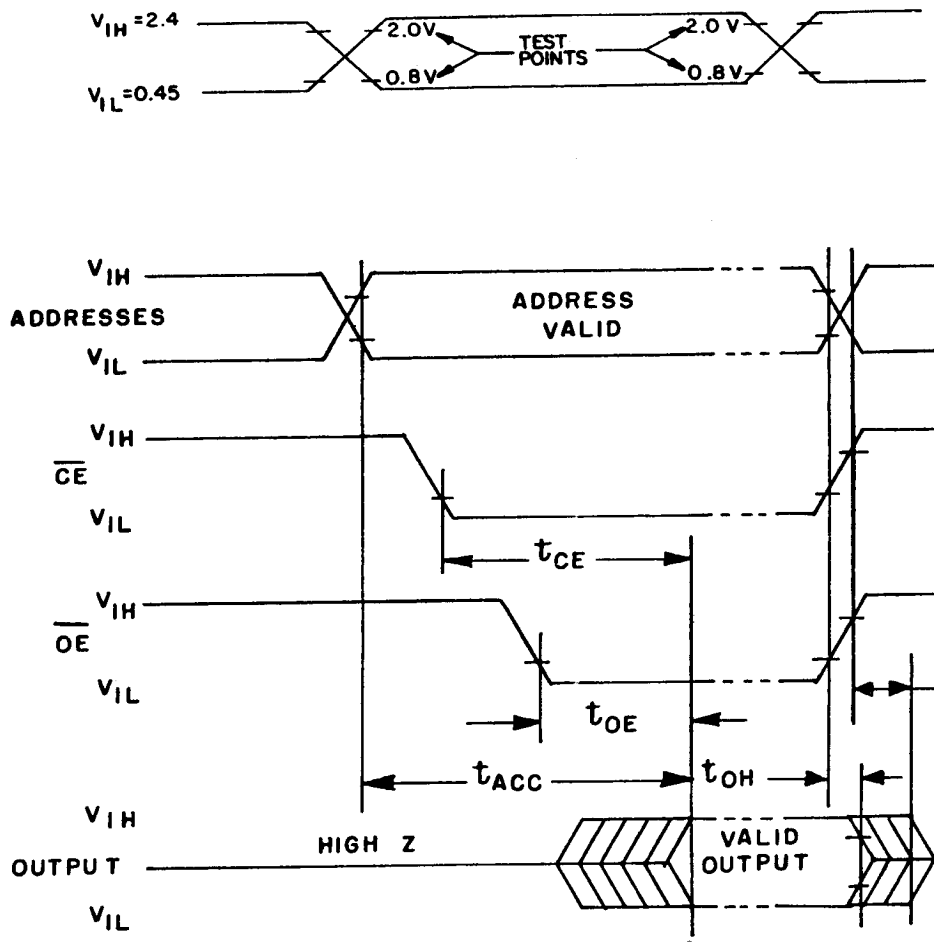


FIGURE 4. Output load (suggested).



NOTES:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

FIGURE 5. Timing diagram.

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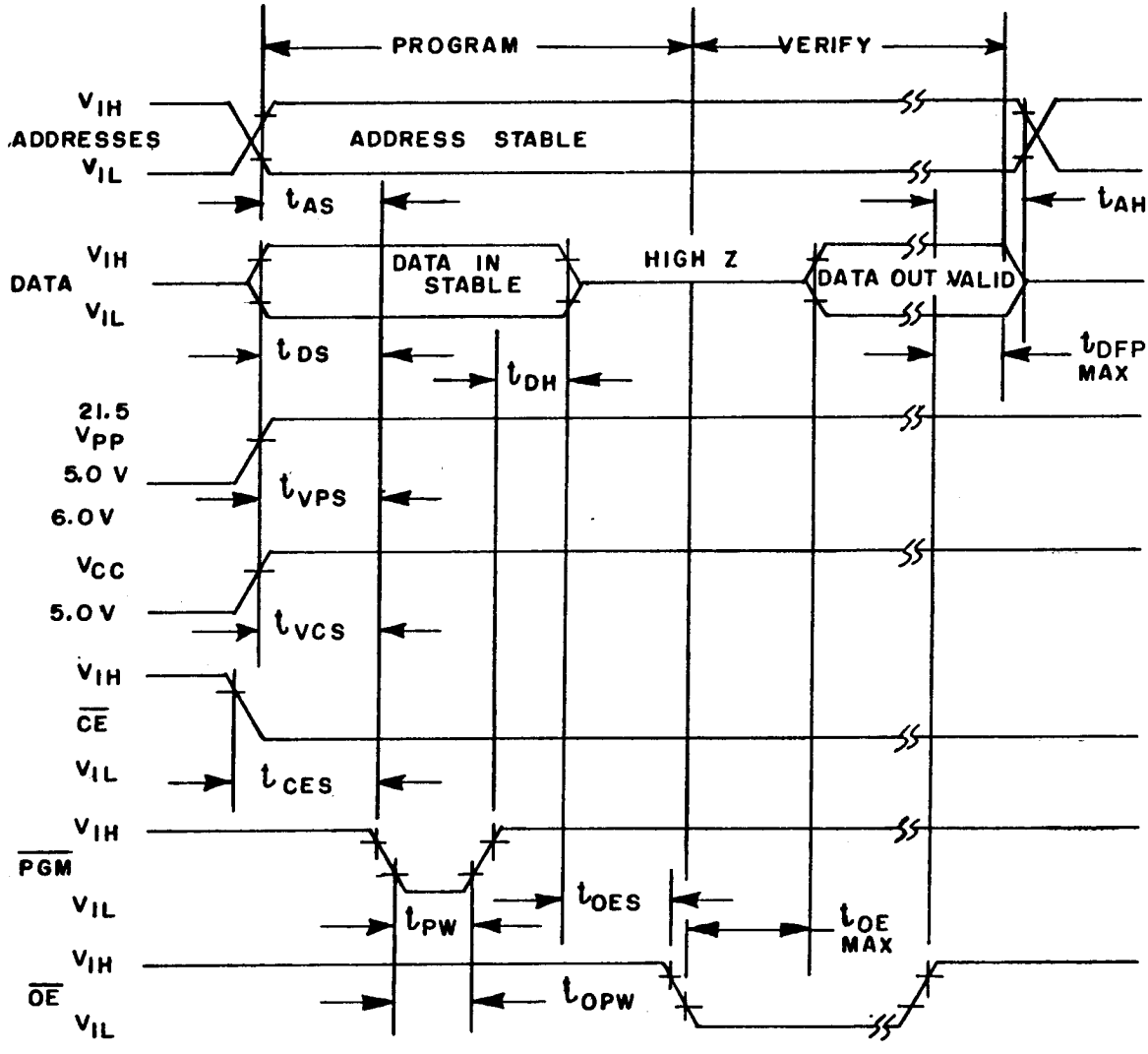
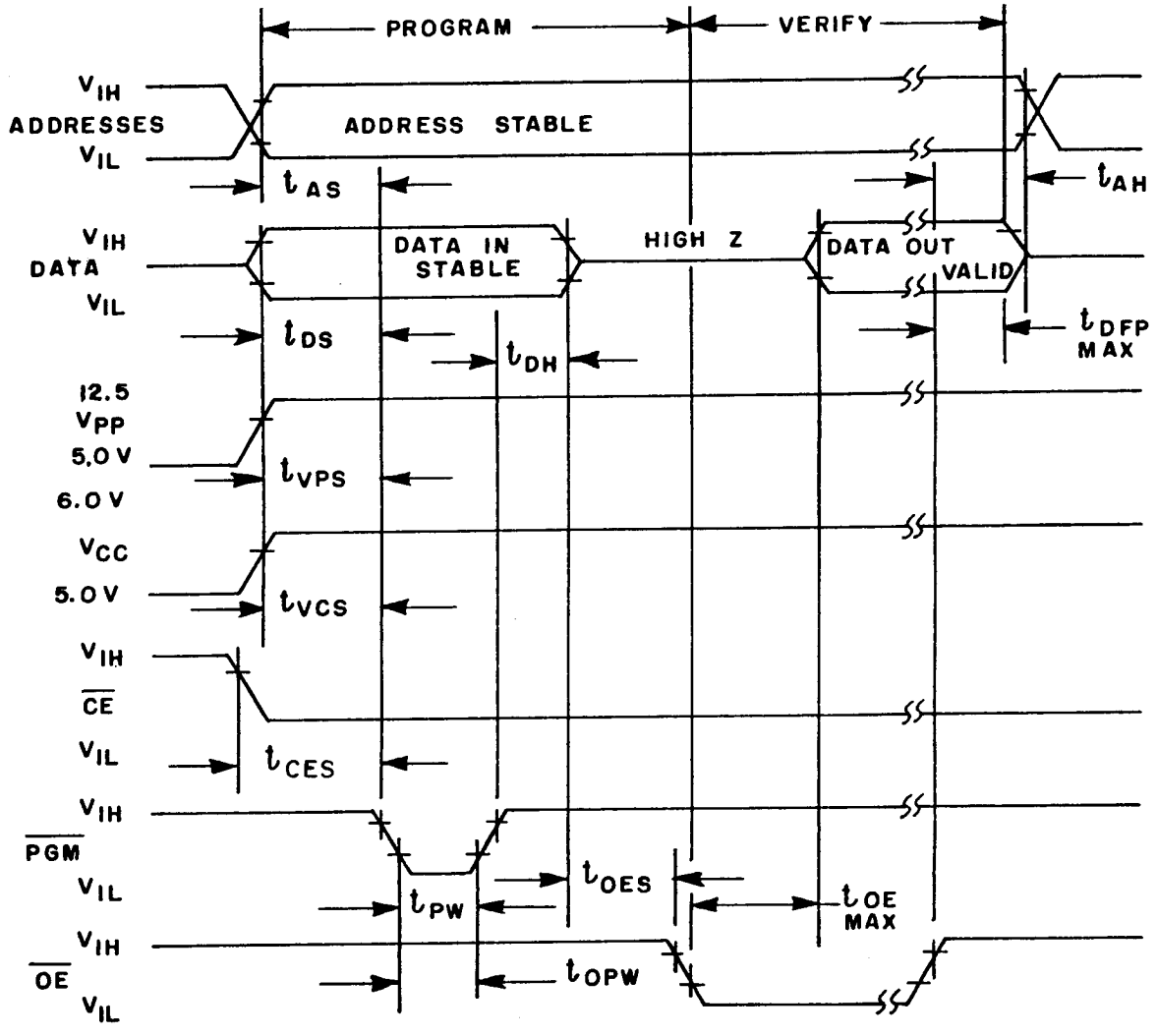


NOTES:
1. All times shown are minimum and in µs unless otherwise specified.
2. The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.
3. t_{OE} and t_{OFP} are characteristics of the device but must be accommodated by the programmer.
4. When programming the device, a 0.1 µF capacitor is required across V_{pp} and ground to suppress spurious voltage transients which can damage the device.

FIGURE 6. Programming timing diagram for methods A and C.



NOTES:
1. All times shown are minimum and in µs unless otherwise specified.
2. The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{III}.
3. t_{OE} and t_{OFP} are characteristics of the device but must be accommodated by the programmer.
4. When programming the device, a 0.1 µF capacitor is required across V_{pp} and ground to suppress spurious voltage transients which can damage the device.

FIGURE 7. Programming timing diagram for method B.

TABLE III. Programming characteristics for method A.

Parameter	Symbol	Conditions V_{CC} = 4.75 V to 5.25 V 1/ 2/ T_A = +25°C unless otherwise specified	Limits		Unit
			Min	Max	
Input low voltage	V_{IL}			0.8	V
Input high voltage	V_{IH}		2.2	V_{CC}+1	V
Input leakage current	I_{IL}	0.4 V $\leq V_{IN} \leq$ 5.25 V	-10	+10	µA
Programming voltage	V_{PP}		20.5	21.5	V
Programming supply current (program)	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$		30	mA
Programming supply current (program verify)	I_{PP3}			5	mA
Programming supply current (program inhibit)	I_{PP4}			5	mA
V_{CC} supply current (program inhibit)	I_{CC1}	$\overline{CE} = V_{IH}$		50	mA
V_{CC} supply current (program and verify)	I_{CC2}			150	mA
Address setup time	t_{AS}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Program pulse width	t_{PN}		45	55	ms
Vpp setup time	t_{PS}		2		µs
Output enable setup time	t_{OES}			150	ns

See footnotes at end of table.

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TABLE III. Programming characteristics for method A - Continued.

Parameter	Symbol	Conditions V_{CC} = 4.75 V to 5.25 V 1/ 2/ T_A = +25°C unless otherwise specified	Limits		Unit
			Min	Max	
Chip enable setup time	t_{CES}		2		µs
Chip enable to output delay	t_{DFP}		0	130	ns

1/ $t_f = t_r = 20$ ns; $V_{IL} = 0.45$ V; $V_{IH} = 2.4$ V; reference levels 0.8 V and 2.0 V.

2/ V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

TABLE IV. Programming characteristics for method B.

Test	Symbol	Conditions 1/ V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.5 V, T_A = +25°C unless otherwise specified	Limits Min	Limits Max	Unit
Input current (all inputs)	I_{IL}	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
Input low level (all inputs)	V_{IL}			0.8	V
Input high level	V_{IH}		2.0	V_{CC}+1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = -400 µA	2.4		V
V_{CC} supply current (program and verify)	I_{CC}			120	mA
Vpp supply current (program)	I_{PP}	$\overline{CE} = V_{IL}$		50	mA
A9 intelligent identifier voltage	V_{ID}		11.5	12.5	V
Address setup time	t_{AS}		2		µs
Output enable setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Output enable to output float delay	t_{DFP}	2/	0	130	ns
Vpp setup time	t_{PS}		2		µs
V_{CC} setup time	t_{CS}		2		µs

See footnotes at end of table.

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TABLE IV. Programming characteristics for method B - Continued.

Test	Symbol	Conditions 1/ V_{CC} = 6.0 V ±0.25 V, V_{PP} = 12.5 V ±0.5 V, T_A = +25°C unless otherwise specified	Limits Min	Limits Max	Unit
$\overline{PGM}$ initial program pulse width	t_{PW}	3/	0.95	1.05	ms
$\overline{PGM}$ overprogram pulse width	t_{OPW}	4/	1.9	78.75	ms
Data valid from $\overline{OE}$	t_{OE}			150	ns

1/ V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.

2/ This parameter is only sampled and is not 100 percent tested. Output float is defined as the point where data is no longer driven - see timing diagram on figure 7.

3/ Initial program pulse width tolerance is 1 ms ±5 percent.

4/ The length of the overprogram pulse may vary from 1.9 ms to 78.75 ms as a function of the iteration counter value X.

TABLE V. Programming characteristics for method C.

Test	Symbol	Conditions 1/ T_A = +25°C ±5°C, 5.75 V ≤ V_{CC} ≤ 6.25 V, 20.5 V ≤ V_{PP} ≤ 21.5 V unless otherwise specified	Limits		Unit
			Min	Max	
Input current (all inputs)	I_{IL}	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
Input low level (all inputs)	V_{IL}			0.8	V
Input high level	V_{IH}		2.0	VCC+1	V
Output low voltage during verify	V_{OL}	I_{OL} = 2.1 mA		0.45	V
Output high voltage during verify	V_{OH}	I_{OH} = 400 µA	2.4		V
V_{CC} supply current (program and verify)	I_{CC}			120	mA
Vpp supply current (program)	I_{PP}	$\overline{CE} = V_{IL}$		50	mA
A9 intelligent identifier voltage	V_{ID}		11.5	12.5	V
Address setup time	t_{AS}		2		µs
$\overline{OE}$ setup time	t_{OES}		2		µs
Data setup time	t_{DS}		2		µs
Address hold time	t_{AH}		0		µs
Data hold time	t_{DH}		2		µs
Output enable to output float delay	t_{DFP}	2/	0	130	ns
Vpp setup time	t_{PS}		2		µs
V_{CC} setup time	t_{CS}		2		µs

See footnotes at end of table.

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TABLE V. Programming characteristics for method C - Continued.

Test	Symbol	Conditions 1/ T_A = +25°C ±5°C, 5.75 V ≤ V_{CC} ≤ 6.25 V, 20.5 V ≤ V_{PP} ≤ 21.5 V	Limits		Unit
			Min	Max	
$\overline{PGM}$ initial program pulse width	t_{PW}		0.95	1.05	ms
$\overline{PGM}$ overprogram pulse width	t_{OPW}		2.85	78.75	ms
Data valid from $\overline{OE}$	t_{OE}			150	ns
$\overline{CE}$ setup time	t_{CES}		2		µs

1/ V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.

2/ Tested by inference only.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, OH 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.6) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Programming method	Margin test method
8202501YX	61394	DM27128-450	C	C
8202501ZX	61394	LM27128-450	C	C
8202502YX	61394	DM27128-250	C	C
8202502ZX	61394	LM27128-250	C	C
8202503YX	34649	MD27128A-20/B	B	B
8202503YX	34335	AM27128A-20/BXA	B	A
8202503ZX	34335	AM27128A-20/BUA	B	A
8202504YX	34649	MD27128A-30/B	B	B
8202504YX	34335	AM27128A-30/BXA	B	A
8202504ZX	34335	AM27128A-30/BUA	B	A
8202505YX	34649	MD27128A-25/B	B	B
8202505YX	34335	AM27128A-25/BXA	B	A
8202505ZX	34335	AM27128A-25/BUA	B	A
8202506YX	34649	MD27128A-15/B	B	B
8202507YX	34649	MD27128A-11/B	B	B
8202508YX	61394	DM27128-200	C	C
8202508ZX	61394	LM27128-200	C	C
8202509YX	61394	DM27128-300	C	C
8202509ZX	61394	LM27128-300	C	C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Intelligent identifier	
		Manufacturer	Device
34335	Advanced Micro Devices Incorporated 901 Thompson Place Sunnyvale, CA 94088	01	89
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051	89	89
61394	SEEQ Technology 1849 Fortune Drive San Jose, CA 95131	94	C1