

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X305 based system. Internal circuitry is provided for direct use in 8X305 applications. When used with the 8X305, the RAM address and data busses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-State outputs.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Ceramic DIP 400mil-wide	8X350/BWA

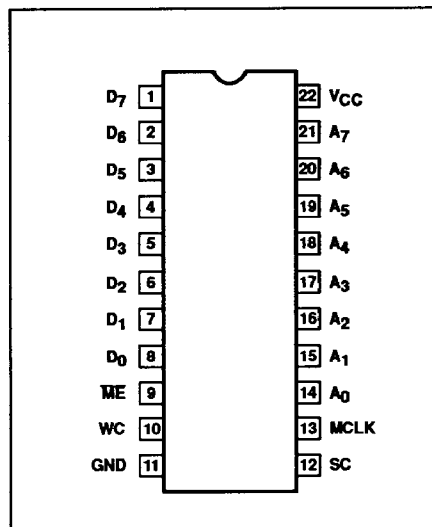
FEATURES

- On-chip address latches
- Schottky clamped
- One master enable input
- Directly interfaces with the 8X305 bipolar microprocessor with no external logic
- May be used on left or right bank
- Common I/O:
 - Inputs: PNP buffered
 - Outputs: 3-State

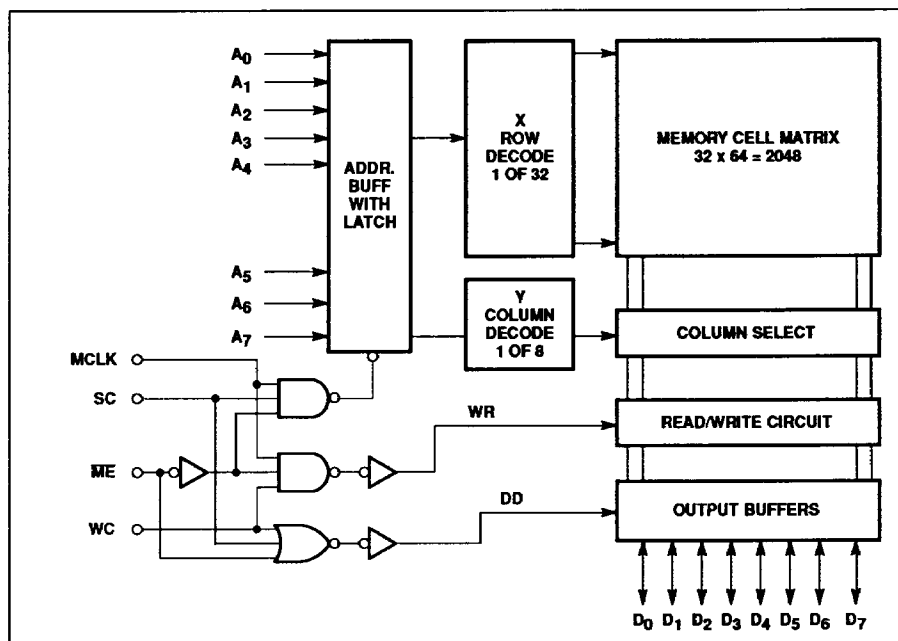
APPLICATIONS

- 8X305 working storage

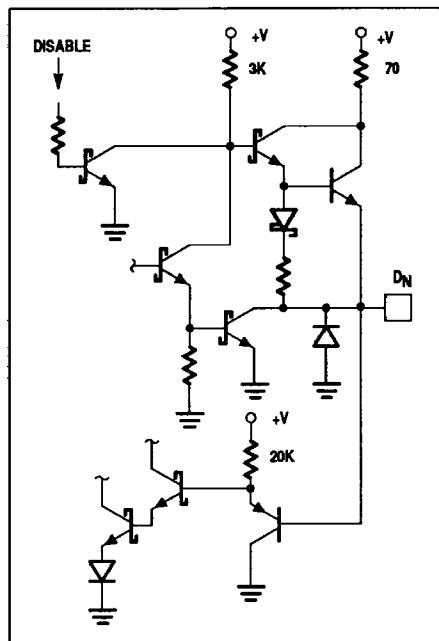
PIN CONFIGURATION



BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



2K-Bit TTL Bipolar RAM (256 × 8)**8X350****ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	+7	V _{DC}
V _I	Input voltage	+5.5	V _{DC}
V _O	Output voltage High	+5.5	V _{DC}
V _O	Output voltage Off-state	+5.5	V _{DC}
T _A	Operating temperature range	-55 to +125	°C
T _{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V²

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V _{IL} V _{IH} V _{IK}	Low High Clamp ³	V _{CC} = 4.75V, I _I = -18mA	2.0		0.8 -1.2	V V V
Output voltage						
V _{OL} V _{OH}	Low ⁴ High ⁵	V _{CC} = 4.75V I _{OL} = 9.6mA I _{OH} = -2mA	2.4		0.5	V V
Input current						
I _{IL} I _{IH}	Low High	V _{CC} = 5.25V V _I = 0.45V V _I = 5.5V			-150 50	μA μA
Output current						
I _{OZ} I _{OS}	Hi-Z state Short circuit ^{3, 6, 13}	V _{CC} = 5.25V ME = High, V _O = 5.5V ME = High, V _O = 0.5V SC = WC, ME = Low V _{CC} = 5.25V, V _O = 0V, High stored	 -15		60 -100 -85	μA μA mA
Supply current ⁷						
I _{CC}		V _{CC} = 5.25V			200	mA
Capacitance ¹³						
C _{IN} C _{OUT}	Input Output	ME = High, V _{CC} = 5.0V V _I = 2.0V V _O = 2.0V		5 8	10 13	pF pF

2K-Bit TTL Bipolar RAM (256 × 8)**8X350****TRUTH TABLE**

MODE	ME	SC	WC	MCLK	BUSSED DATA/ ADDRESS LINES
Hold address Disable data out	1	X	X	X	Hi-Z data out
Input new address	0	1	0	1	Address Hi-Z
Hold address Disable data out	0	1	0	0	Hi-Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	Hi-Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state ¹²	0	1	1	1	-
Hold address ¹² Disable data out	0	1	1	0	Hi-Z data out

X = Don't care

AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V²

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
t _{E1} t _{E2}	Output enable time Output enable time	Data out Data out	SC- ME-			40 40	ns ns
t _{D1} t _{D2}	Output disable time Output disable time	Data out Data out	SC+ ME+			40 40	ns ns
t _W	Master clock pulse width ⁸			50			ns
t _{SA} t _{HA}	Setup time Hold time	MCLK- Address	Address MCLK-	40 10			ns ns
t _{SD} t _{HD}	Setup time Hold time	MCLK- Data in	Data in MCLK-	45 10			ns ns
t _{S3} t _{H3}	Setup time Hold time	MCLK- ME+	ME- MCLK-	50 5			ns ns
t _{S1} t _{H2}	Setup time Hold time	MCLK- ME-	ME- MCLK-	40 5			ns ns
t _{S2} t _{H1} t _{H4}	Setup time Hold time Hold time	ME- SC- WC-	SC-, WC- MCLK- MCLK-	5 5 5			ns ns ns

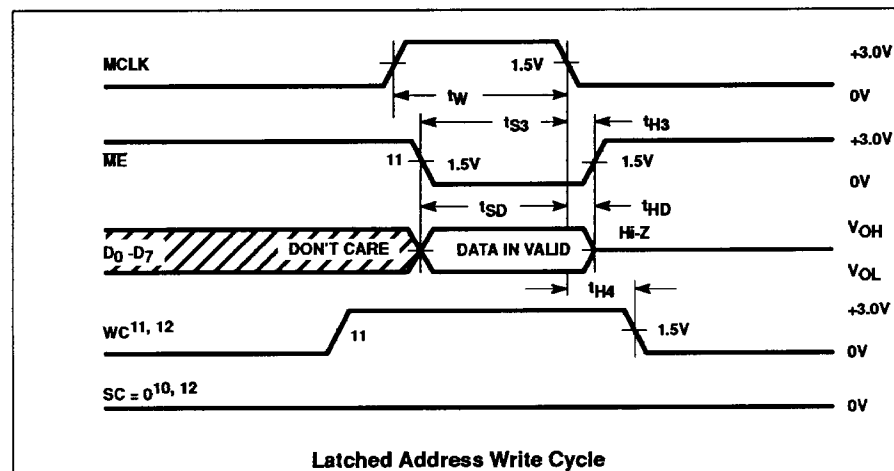
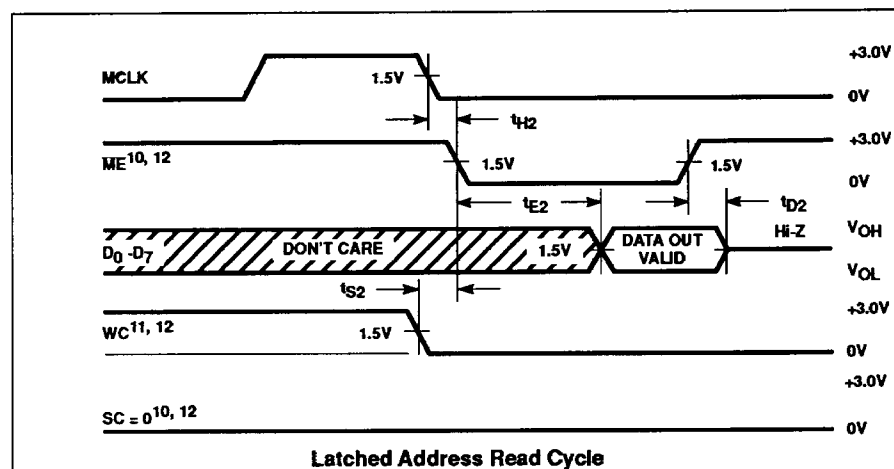
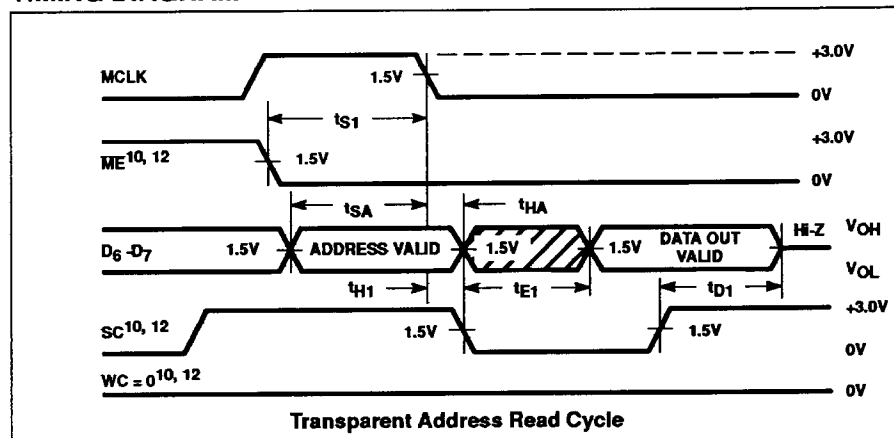
NOTES:

1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a one-minute warm-up. This testing will be guaranteed by testing at -40°C using instant on testing.
3. Test each pin one at a time.
4. Measured with a logic Low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with a logic High stored.
6. Duration of the short circuit should not exceed 1 second.
7. I_{CC} is measured with the Write enable and Memory enable inputs grounded, all other inputs ≥ 4.0V and the output open.
8. Minimum required to guarantee a Write into the slowest bit.
9. Applied to the 8X305 based system with the data and address pins tied to the IV Bus.
10. SC + ME = 1 to avoid bus conflict.
11. WC + ME = 1 to avoid bus conflict.
12. The SC and WC outputs from the 8X305 are never at 1 simultaneously.
13. Guaranteed, but not tested.

2K-Bit TTL Bipolar RAM (256 × 8)

8X350

TIMING DIAGRAM



MEMORY TIMING DEFINITIONS

t_{S1}	Required delay between beginning of Master Enable Low and falling edge of Master Clock.
t_{SA}	Required delay between beginning of valid address and falling edge of Master Clock.
t_{E1}	Delay between beginning of Select Command Low and beginning of valid data output on the IV Bus.
t_{E2}	Delay between when Master Enable becomes Low and beginning of valid data output on the IV Bus.
t_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
t_{D1}	Delay between when Select Command becomes High and end of valid data output on the IV Bus.
t_{D2}	Delay between when Master Enable becomes High and end of valid data output on the IV Bus.
t_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes Low.
t_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes Low.
t_{S2}	Required delay between when Select Command or Write Command becomes Low and when Master Enable becomes Low.
t_W	Minimum width of the Master Clock pulse.
t_{SD}	Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
t_{S3}	Required delay between when Master Enable becomes Low and falling edge of Master Clock.
t_{HD}	Required delay between beginning of valid data input on the IV Bus.
t_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes High.
t_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes Low.

8X350

The diagram illustrates the internal architecture and external connections of the 8X350 microcontroller. Key components and connections include:

- Central Processor:** 8X350 MICROCONTROLLER with pins for ADDRESS (A0-A12), DATA (I0-I15), and CONTROL (RESET, HALT, VCC, VR, VCR, ME).
- Memory:**
 - PROMs:** Two SIGNETICS 512 x 8 PROMs connected via address lines A4-A12 and data lines I0-I15.
 - RAM:** 8X350 256 x 8 RAM connected via address lines A4-A12 and data lines I0-I15.
- I/O Ports:** Four 8X37X I/O PORTs connected to the microcontroller's ME (Master Enable) pin and providing UD0-UD7 data and BIC/BIOC control signals.
- Control & Timing:**
 - RESET:** Connected to a 2N5320 transistor circuit with a 0.1µF capacitor.
 - HALT:** Connected to the VCR pin.
 - VCC, VR, VCR:** Power supply pins with associated decoupling capacitors.
 - ME:** Master Enable pin connected to the I/O ports.
- External Signals:** IVB0-IVB7, MCLK, SC, WC, LB, and RB signals are shown entering the microcontroller.

NOTE: $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 50pF$

The diagram illustrates the input pulse characteristics for a device. It shows two waveforms: a Negative Pulse and a Positive Pulse. Both pulses are defined by their voltage levels and timing parameters.

Negative Pulse: The pulse starts at 3.0V, transitions to 2.7V, then to V_M , and finally to 0.3V. The pulse width is t_W . The transition times are $t_{TLH}(tr)$ (from 0.3V to V_M) and $t_{THL}(tf)$ (from V_M to 0.3V).

Positive Pulse: The pulse starts at 0.3V, transitions to V_M , then to 2.7V, and finally to 3.0V. The pulse width is t_W . The transition times are $t_{TLH}(tr)$ (from 0.3V to V_M) and $t_{THL}(tf)$ (from V_M to 0.3V).

Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	$\leq 5ns$	$\leq 5ns$

2K-Bit TTL Bipolar RAM (256 × 8)**8X350****DEFINITIONS**

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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