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LH52253

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 15 */20/25/35 ns
- Standard 28-Pin, 300-mil DIP
- Space Saving 28-Pin, 300-mil SOJ
- JEDEC Standard Pinouts
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count

FUNCTIONAL DESCRIPTION

The LH52253 is a very high-speed 256K-bit static RAM organized as 64K × 4. This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is inactive (HIGH). The combination of $\overline{E}$ and $\overline{W}$ control the mode of operation of the LH52253.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static read of the memory location specified by the address lines will occur. Since the device is fully static in operation, new read cycles can be performed by simply changing the address. An Automatic Power Down feature reduces the current consumption when Read and Write cycles extend beyond their minimum cycle times.

The LH52253 offers an Output Enable ($\overline{G}$) for use in managing the Data Bus. Bus contention during Write cycles may be easily avoided by using the $\overline{G}$ input in the LH52253.

High-frequency design techniques should be employed to obtain the best performance from these devices. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

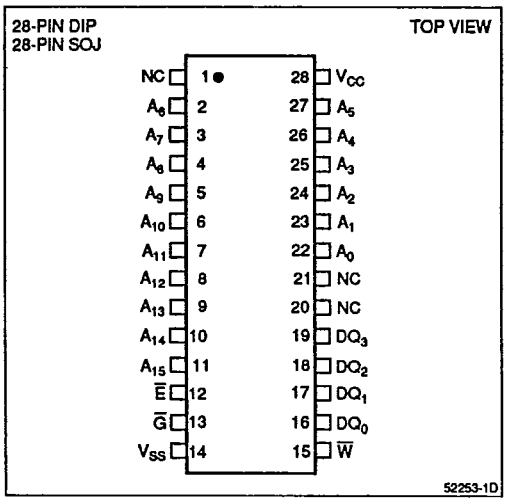

Figure 1. Pin Connections for DIP and SOJ

* Note: only the 15 ns access time part is Advance Information.

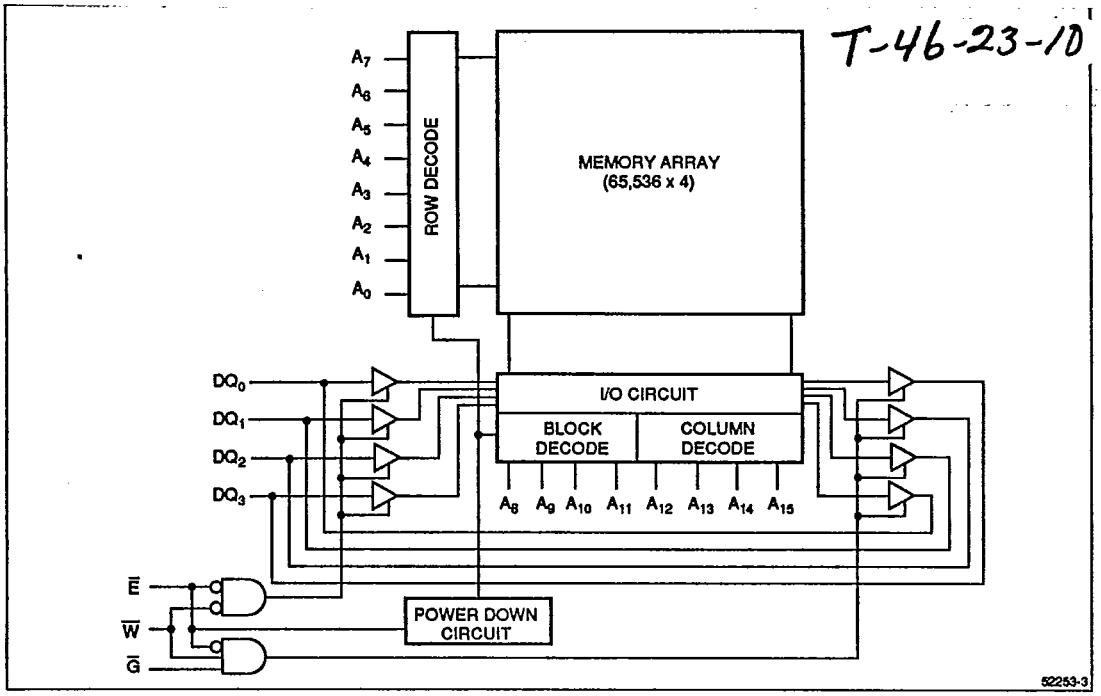

Figure 2. LH52253 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	MODE	DQ	Icc
H	X	X	Not Selected	High-Z	Standby
L	H	L	Read	Data Out	Active
L	H	H	Read	High-Z	Active
L	L	X	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
$\overline{G}$	Output Enable input
Vcc	Positive Power Supply
Vss	Ground

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ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Function operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 15 ns [2] $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}			165	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 20 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}			145	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{CYCLE} = 25 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}			135	mA
I_{CC1}	Operating Current [1]	Outputs open, t_{RC} = 35 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}			135	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V			1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ min			10	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTES:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.
2. Note: only the 15 ns access time part is Advance Information.

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AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

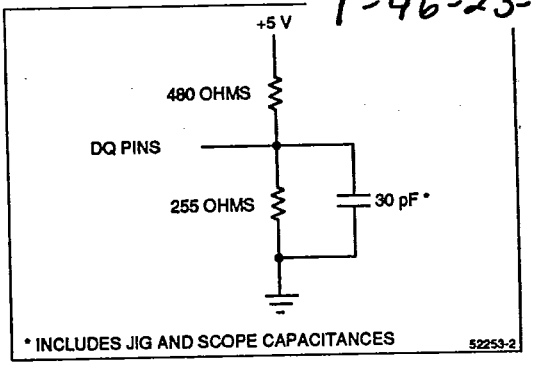

Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{DQ} (Input/Output Capacitance)	8 pF

NOTES:
1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-15 [4]		-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE									
t_{RC}	Read Cycle Timing	15		20		25		35		ns
t_{AA}	Address Access Time		15		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		15		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		8		10		10		12	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		12		15	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	7	0	9	0	10	0	12	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		30		35	ns
	WRITE CYCLE									
t_{WC}	Write Cycle Time	15		20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	12		15		20		25		ns
t_{AW}	Address Valid to End of Write	12		15		20		25		ns
t_{AS}	Address Setup	0		0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	0		0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	10		12		15		20		ns
t_{DW}	Input Data Setup Time	8		10		10		12		ns
t_{DH}	Input Data Hold Time	0		0		0		0		ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	4		4		4		4		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		6		7		8		10	ns

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
3. Guaranteed but not tested.
4. Note: only the 15 ns access time part is Advance Information.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in the Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid when $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Valid Data will be present following t_{GA} only if t_{EA} timing has been met.

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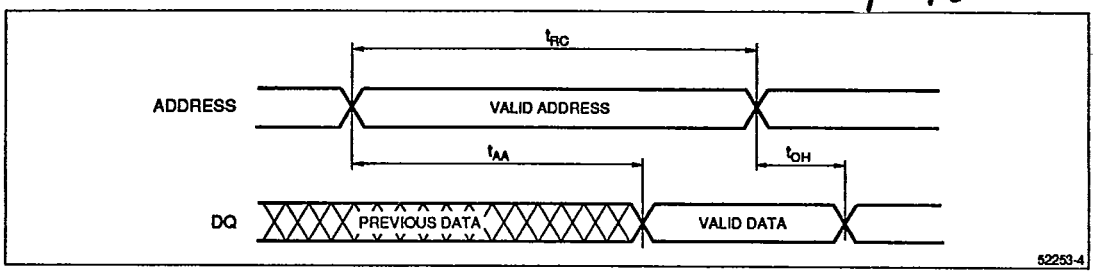

Figure 4. Read Cycle No. 1

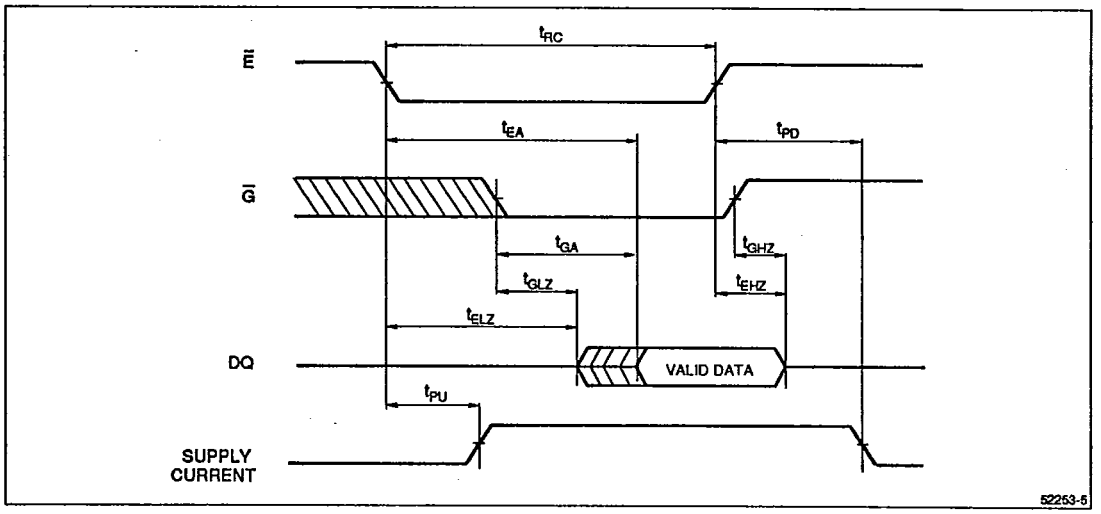

Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise. These timing diagrams assume $\overline{G}$ is LOW, but it should be kept HIGH during Write cycles to insure that the output drivers are disabled.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

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Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

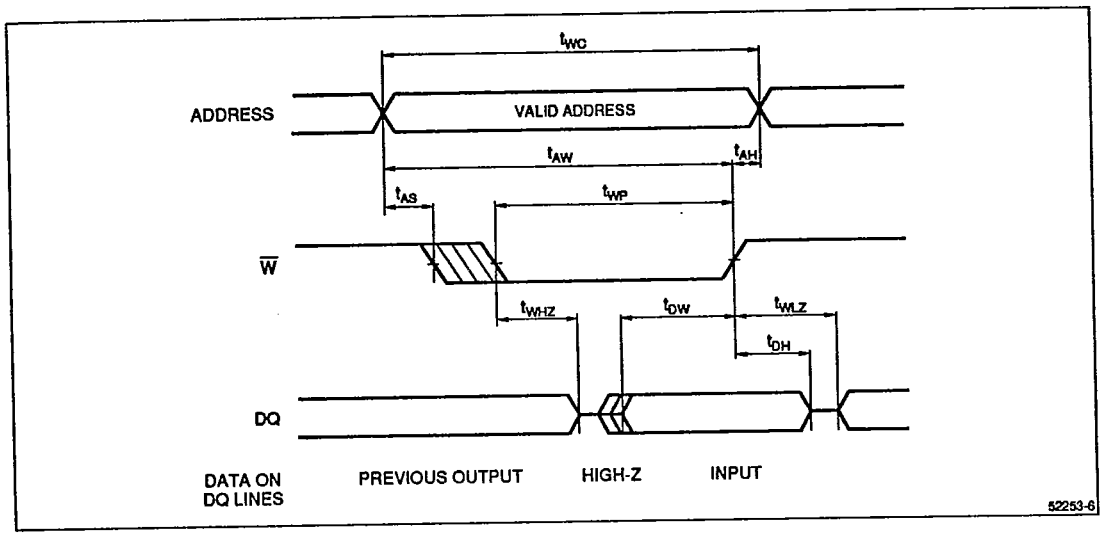


Figure 6. Write Cycle No. 1

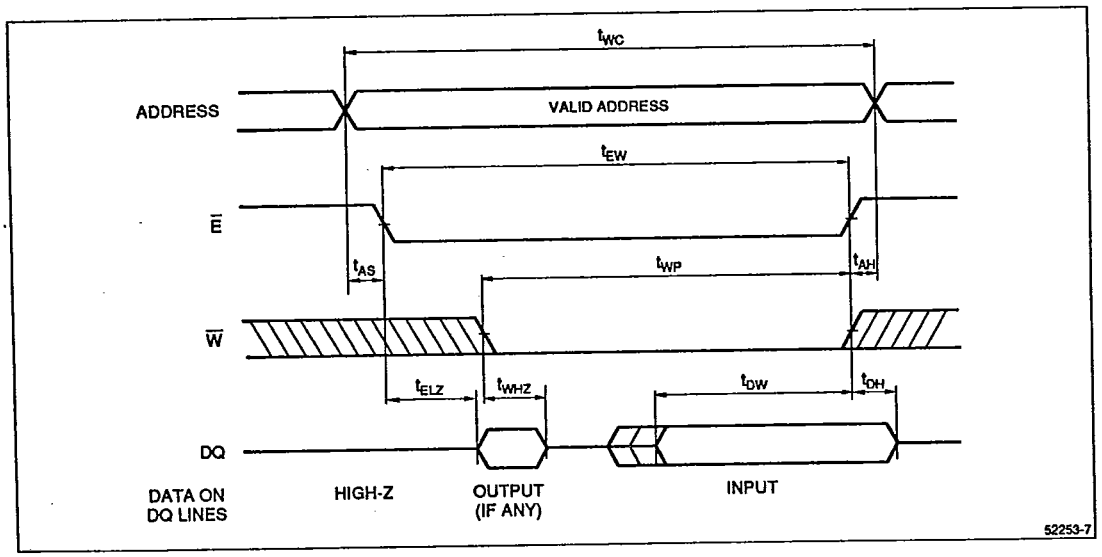
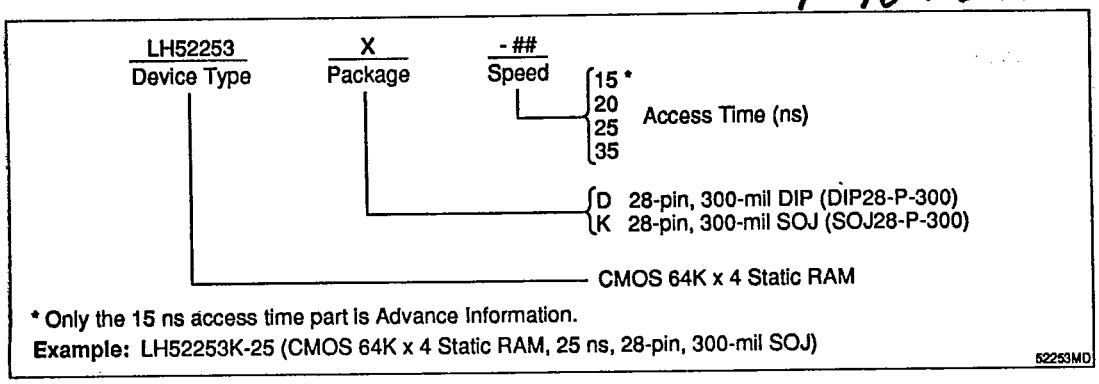


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



* Only the 15 ns access time part is Advance Information.

Example: LH52253K-25 (CMOS 64K x 4 Static RAM, 25 ns, 28-pin, 300-mil SOJ)

52253MD