Two-Channel Distributed System Interface (DSI) Physical Interface Device

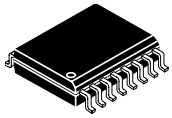
33790

DISTRIBUTED SYSTEM INTERFACE (DSI)

The 33790 is a dual channel physical layer interface IC for the Distributed System Interface (DSI) bus. It is designed to meet automotive requirements. It can also be used in non automotive applications. It supports bidirectional communication between slave and master ICs. Some slave devices derive a regulated 5.0 V from the bus, which can be used to power sensors, thereby eliminating the need for additional circuitry and wiring.

Features

- Two Independent DSI Compatible Buses
- Pinout Matched to MC68HC55 (SPI to DSI Logic)
- Wave-Shaped Bus Output Voltage
- Independent Thermal Shutdown and Current Limit
- Return Signalling Current Detection
- Internal Logic Input Pull ups and Pull downs
- On-Board Charge Pump
- 2.0 kV ESD Capability
- Communications Rate Up to 150 kbps
- Pb-Free Packaging Designated by Suffix Code EG



DW SUFFIX
EG SUFFIX (PB-FREE)
98ASB42567B
16-PIN SOICW

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33790DW/R2	-40°C to 85°C	16 SOICW
MCZ33790EG/R2		

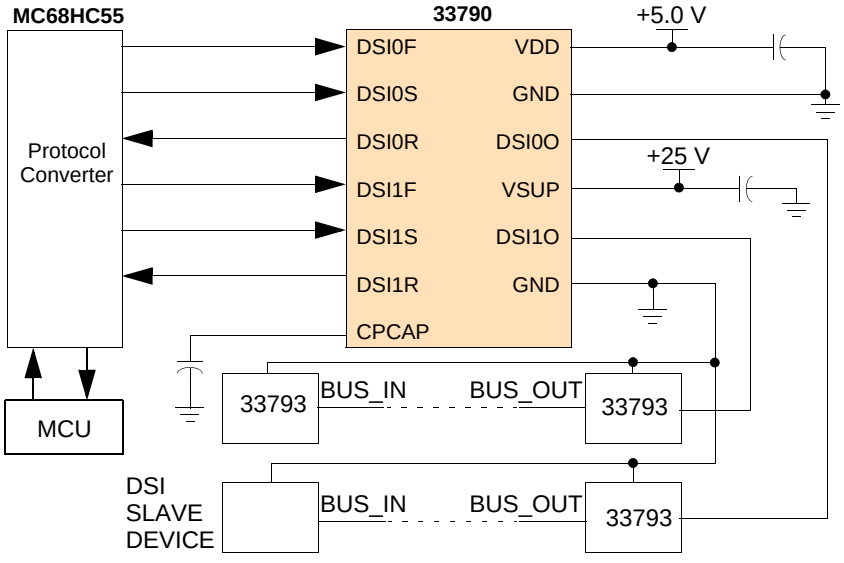


Figure 1. 33790 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

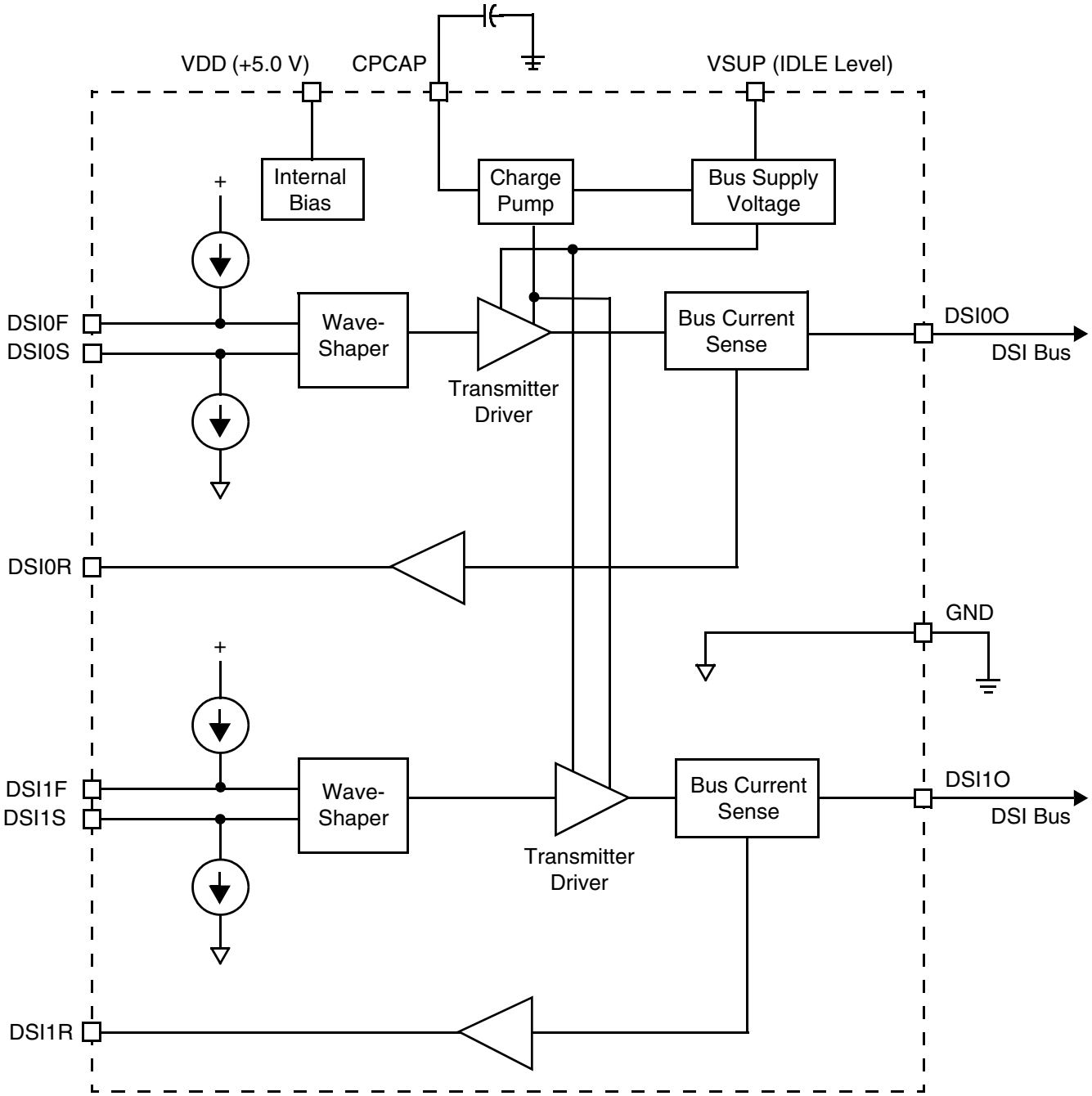


Figure 2. 33790 Simplified Internal Block Diagram

PIN CONNECTIONS

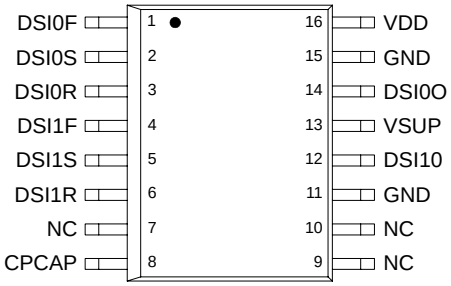


Figure 3. 33790 Pin Connections

Table 1. 33790 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 8.

Pin Number	Pin Name	Definition
1	DSI0F	This logic input controls the frame output for DSI channel 0 in accordance with Table 5, page 8.
2	DSI0S	This logic input controls the signalling output for DSI channel 0 in accordance with Table 5, page 8.
3	DSI0R	This logic output provides the return data for DSI channel 0 in accordance with Table 5, page 8.
4	DSI1F	This logic input controls the frame output for DSI channel 1 in accordance with Table 5, page 8.
5	DSI1S	This logic input controls the signalling output for DSI channel 1 in accordance with Table 5, page 8.
6	DSI1R	This logic output provides the return data for DSI channel 1 in accordance with Table 5, page 8.
7	NC	Unused.
8	CPCAP	Used to store and filter charge pump output.
9	NC	Unused.
10	NC	Unused.
11	GND	Circuit and bus ground return.
12	DSI1O	DSI bus 1 input/output.
13	VSUP	Idle level supply input. The voltage supplied to this pin sets the idle level on the DSI bus.
14	DSI0O	DSI bus 0 input/output.
15	GND	Circuit and bus ground return.
16	VDD	5.0 V logic supply input.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Continuous Load Dump - t < 300 ms	 V_{SUP} $V_{SUP(t)}$	 -0.5 to 25 40	V
Maximum Voltage on Input/Output Pins	V_{DD} DSIxS, DSIxF (1) DSIxO (1)	-0.3 to 5.5 -0.3 to V_{DD}+0.3 -0.3 to V_{SUP}+0.3	V
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Ambient Temperature	T_A	-40 to 85	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Peak Package Reflow Temperature During Reflow (2), (3)	T_{PPRT}	Note 3	°C
Continuous Current per Pin	V_{DD} DSIxR V_{SUP}	0 to 10 -2.5 to 5.0 500	mA
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	45	°C/W
Thermal Shutdown	T_{SD}	155 to 190	°C
ESD Voltage (All Pins) (4) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V

Notes

1. R = 0 Ω.
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
4. ESD1 performed in accordance with the Human Body Model (C_{ZAP}=100pF, R_{ZAP}=1500 Ω), ESD2 performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{SUP} ≤ 25.0 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY					
I_{SUP} Supply Current/Channel (Not Including I_{OUT}) DSIx0 = Idle Voltage, -100 mA ≤ I_{OUT} ≤ 0 mA DSIx0 = Output High Voltage, I_{OUT} = 12 mA	 I_{SUPI} I_{SUPH}	 – –	 1.35 5.0	 3.25 9.00	mA
I_{DD} Supply Current/Channel	I_{DD}	–	0.5	1.0	mA
BUS TRANSMITTER					
V_{SUP} to DSIxO ON Resistance (During Idle) I_{OUT} = -100 mA	$R_{DS(ON)}$	–	–	10	Ω
Output High Voltage DSIx0 (-15 mA ≤ I_{OUT} ≤ 1.0 mA)	$DSIV_{OH}$	4.175	4.5	4.825	V
Output Low Voltage DSIx0 (-15 mA ≤ I_{OUT} ≤ 1.0 mA)	$DSIV_{OL}$	1.325	1.5	1.675	V
Output High-Side Current Limit (5)	I_{CLH}	-100	–	-200	mA
Output Low-Side Current Limit (5)	I_{CLL}	110	–	220	mA
Input Leakage DSIxO When DSIxF Is High and DSIxS Is Low (0 V ≤ DSIxO ≤ Min (V_{SUP} = 16.5 V))	DSI_{IB}	-200	–	50	μA
BUS RECEIVER					
Return Current Threshold	I_{RH}	-5.0	-6.0	-7.0	mA
MICROCONTROLLER INTERFACE					
Logic Input Thresholds DSIxS, DSIxF	$V_{IN(TH)}$	1.10	–	2.20	V
Output High Voltage DSIxR Pin = -0.5 mA	V_{OH}	0.8 V_{DD}	–	V_{DD}	V
Output Low Voltage DSIxR Pin = 1.0 mA	V_{OL}	0.0	–	0.2 V_{DD}	V
Internal Pullup for DSIxF	I_{IL}	-100	–	-10	μA
Internal Pulldown for DSIxS	I_{IH}	10	–	100	μA

Notes

5. After 10 μs settling time (assured by design).

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{SUP} ≤ 25.0 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
MICROCONTROLLER INTERFACE					
Microcontroller Signal Cycle Time	t_{CYC}	6.6	–	1000	µs
Microcontroller Signal Low Time	t_{CYCL}	2.0	–	667	µs
Microcontroller Signal High Time	t_{CYCH}	2.0	–	667	µs
Microcontroller Signal Duty Cycle for Logic Zero	DC_{LO}	30	33	36	%
Microcontroller Signal Duty Cycle for Logic One	DC_{HI}	60.0	66.7	72.0	%
Microcontroller Signal Slew Time (6)	t_{SLEW}	–	–	500	ns
Frame Start to Signal Delay Time	t_{DLY1}	t_{cyc}-0.1	t_{cyc}	t_{cyc}+0.1	µs
Signal End to Frame End Delay Time	t_{DLY2}	1.0	–	–	µs
Rise Time (6)	t_{RISE}	0	–	100	ns
Fall Time (6)	t_{FALL}	0	–	100	ns
BUS TRANSMITTER					
Idle to Frame and Frame to Idle Slew Rate C ≤ 5.0 nF	$t_{SLEW(FRAME)}$	3.0	6.0	10.0	V/µs
Signal High to Low and Signal Low to High Slew Rate C ≤ 5.0 nF	$t_{SLEW(SIGNAL)}$	3.0	4.5	8.0	V/µs
Data Valid (V_{SUPx} = 25 V, C_L ≤ 5.0 nF)					µs
DSIxF, $V_{IN(TH)}$ to DSIxO = 5.3 V	t_{DVLD1}	2.44	–	6.56	
DSIxS, $V_{IN(TH)}$ to DSIxO = 2.6 V	t_{DVLD2}	0.25	–	1.3	
DSIxS, $V_{IN(TH)}$ to DSIxO = 3.4 V	t_{DVLD3}	0.25	–	1.3	
DSIxF, $V_{IN(TH)}$ to DSIxO = 7.0 V	t_{DVLD4}	0.25	–	1.3	
BUS RECEIVER					
Receiver Delay Time					ns
t_{DRH}: I = I_{RH} to DSIxR = 2.5 V	t_{DRH}	–	400	750	
t_{DRL}: I = I_{RH} to DSIxR = 2.5 V	t_{DRL}	–	400	750	

Notes

6. Slew times and rise and fall times between 10% and 90% of output high and low levels.

TIMING CHARACTERISTICS

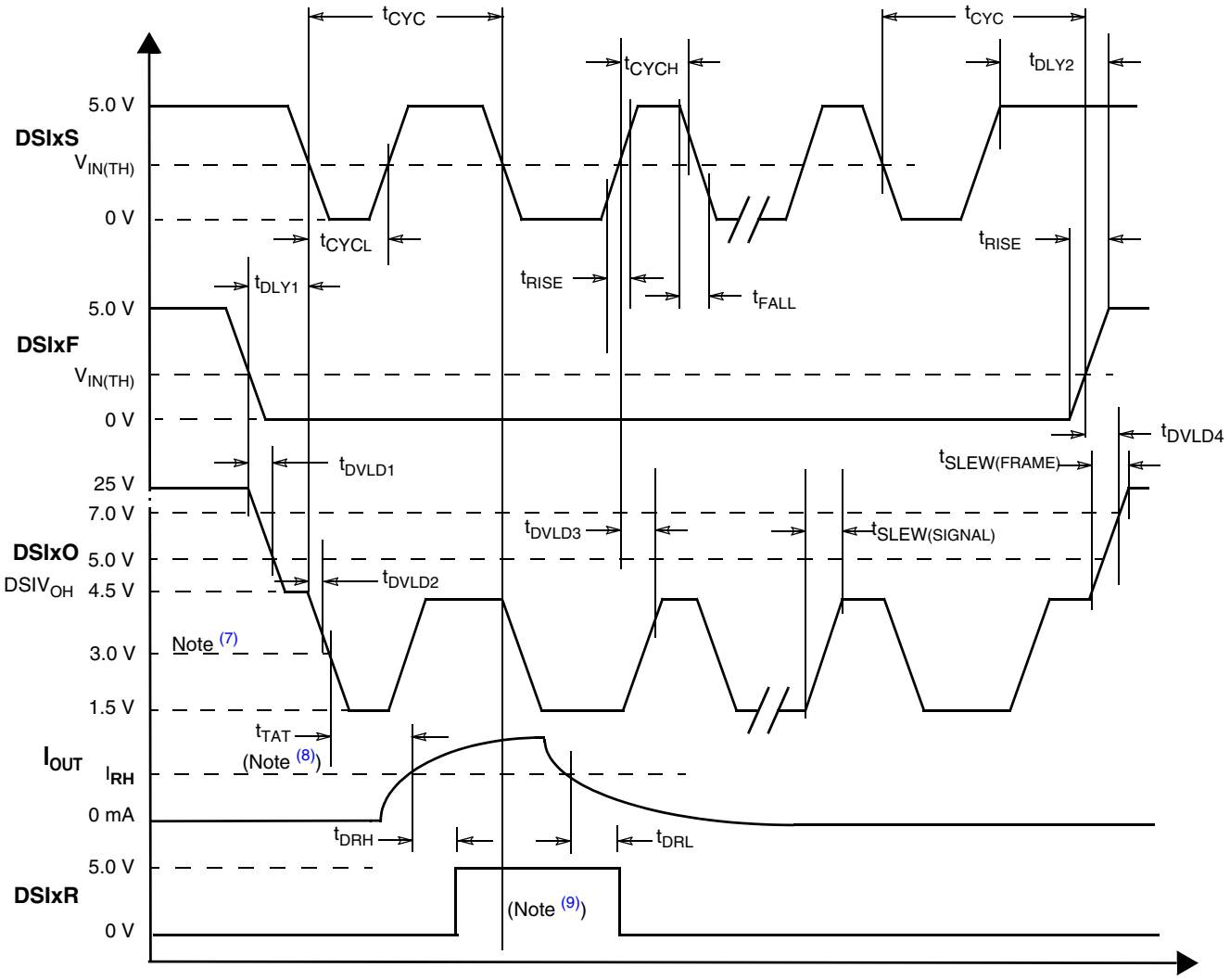


Figure 4. Timing Characteristics

Notes

7. Typical BUSIN/BUSOUT logic thresholds (V_{THL}) from MC33793 datasheet.
8. t_{TAT} (Turnaround Time) is dependent upon wire length, bus loads, and slave response characteristics.
9. DSIxR stable on falling edge of DSIxS or rising edge of DSIxF.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33790 is designed to provide the interface between logic and the DSI bus. It accepts signals with a typical 0 V to 5.0 V logic level to control the state of the bus output (Idle Level, Logic High Level, Logic Low Level, and High Impedance). It detects the current drawn from the bus output during signaling and outputs a 0 V to 5.0 V logic level corresponding to the bus current being above (Logic [1] out) the bus return logic [1] current or below (Logic [0] out). The 33790 contains current limiting of the bus outputs as required by the DSI Bus specification and thermal shutdown to protect itself from damage. Two independent DSI bus outputs are provided by the IC.

FUNCTIONAL TERMINAL DESCRIPTION

Bus Driver and Receiver

The Wave-Shaper converts the 0 V to 5.0 V logic inputs from DSIxF (frame) and DSIxS (signal) to a wave-shaped signal on the DSIxO output, as shown in the timing diagrams in Figure 2, page 2, and the truth table in Table 5. The Bus Current Sense detects the current being drawn by the device(s) on the bus during signalling (DSIxF=0). If the current is above a set level, DSIxR will be high; otherwise, it is low. Due to the variations in the turnaround time (t_{TAT}) from slave devices and bus delays, DSIxR should be sampled on the falling edge of DSIxS and on the rising edge of DSIxF (for the last return bit).

Table 5. DSI Bus Truth Table

DSIxF	DSIxS	Tx_{LIM}	DSIxR	DSIxO
0	0	0	Not Defined	Low (1.5 V)
0	1	0	Not Defined	High (4.5 V)
0	↓	0	Return Data	Unchanged
↑	X	0	Return Data	Unchanged
1	0	0	0	High Impedance
1	1	0	0	Idle≥V_{SUP}-0.5 V
X	X	1	1	High Impedance

The current for the idle state is from the supply connected to V_{SUP} and this supply should not be current limited below 250 mA per channel. During idle state, the voltage on the DSI bus will be very close to the V_{SUP} voltage.

Internal thermal shutdown circuitry and current limit individually protect the DSIxO outputs from shorts to battery and ground.

Typically, the thermal shutdown occurs between 160°C and 170°C. If the junction temperature rises above this temperature, the internal Tx_{LIM} bit is asserted, and the output drivers for DSIxO are disabled by the thermal shutdown circuitry. The output drivers remain off until the junction temperature decreases below approximately 155°C, at which time the thermal shutdown circuitry turns off and the outputs are re-enabled. Each DSIxO output has a unique thermal sense and shutdown circuit, so a short on one channel does not affect the other channel.

Charge Pump

The charge pump uses on-board capacitors to step the input voltage up to the voltage needed to drive the on-board transmitter FETs. A filter/storage capacitor is connected to CPCAP to hold the stepped-up voltage.

Input Pullups and Pulldowns

Internal current pullups are used on the DSIxF pins and pulldowns on the DSIxS pins. If these pins are left unconnected, their associated DSI bus will go to the unused (high impedance) state.

TYPICAL APPLICATIONS

The 33790 is intended for use in a DSI system. This device supplies the interface between standard logic levels and the voltage and current required for the DSI bus. Two independent DSI busses are supported by this part. The 33790 does not form the timing for the DSI bus. This is done by logic either embedded in a microcontroller or by the MC68HC55, which uses SPI commands and forms DSI protocol for communications over the DSI bus.

The pins from the MC68HC55 are made to line up with the pins connecting to the 33790. This includes all the DSIxF, DSIxS, and DSIxR pins.

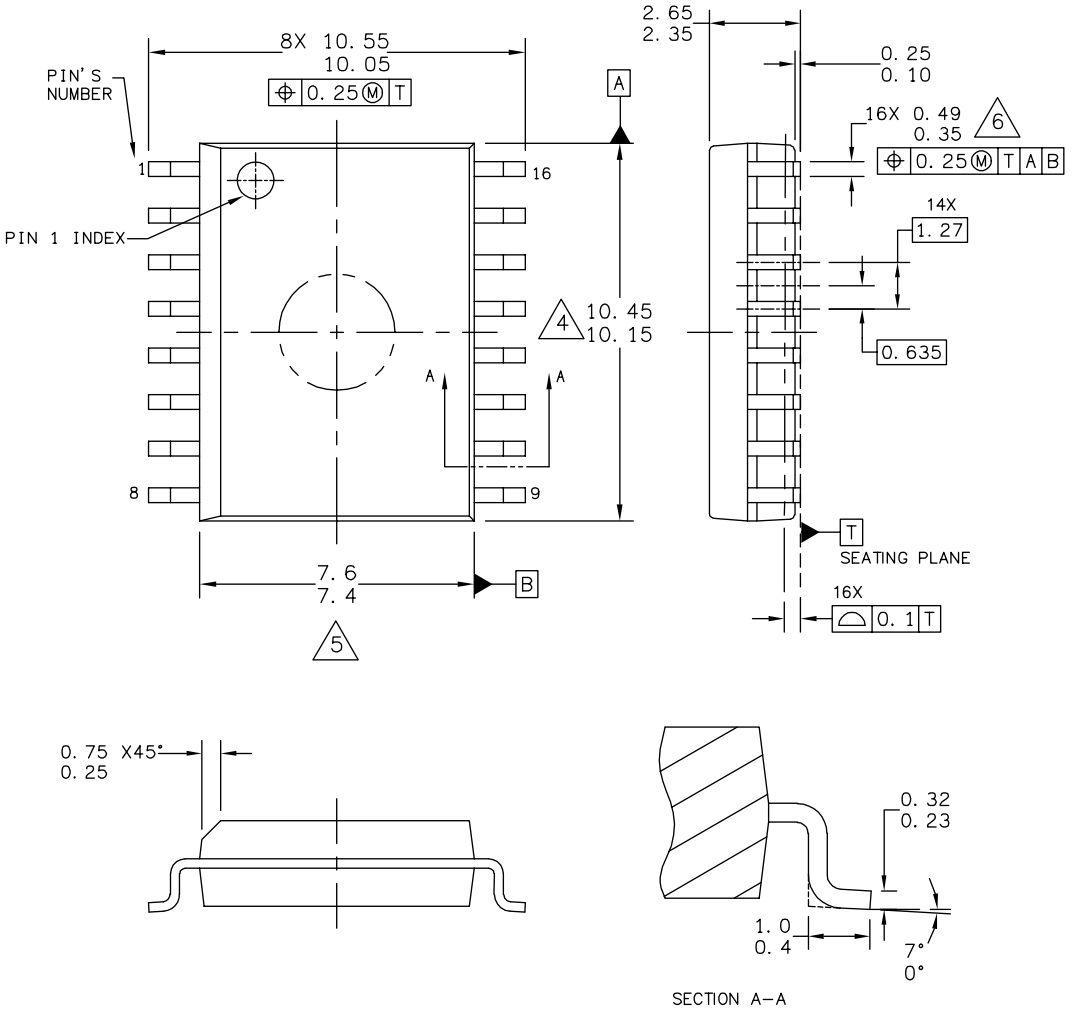
A capacitor attached to CPCAP serves as a charge reservoir for the gate drive charge pump. This circuit creates a voltage that is higher than the source of the N-channel output transistor. This allows turning on of the transistor enough to prevent any significant voltage drop across it. The rest of charge pump electronics are completely self-contained on the IC.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.

DW SUFFIX
EG SUFFIX (PB-FREE)
98ASB42567B
16-PIN SOICW



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TITLE: 16LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42567B	REV: F
	CASE NUMBER: 751G-04	02 JUN 2005
	STANDARD: JEDEC MS-013AA	

33790

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
7.0	5/2006	• Implemented Revision History page • Converted to Freescale format
8.0	11/2006	• Updated data sheet format • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 4. Added note with instructions to obtain this information from www.freescale.com.
9.0	11/2006	• Minor correction changes to Figure 1 and ordering information
10.0	12/2006	• Restated note Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics. on page 4

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