

## Features

- EE Programmable 65,536 x 1-, 131,072 x 1-, 262,144 x 1-, 524,288 x 1-, 1,048,576 x 1-, 2,097,152 x 1-, and 4,194,304 x 1-bit Serial Memories Designed to Store Configuration Programs for Altera FLEX<sup>®</sup> and APEX FPGAs (Device Selection Guide Included)
- Available as a 3.3V (-10%) to 5.0V (+10%) Version
- In-System Programmable (ISP) via 2-wire Bus
- Simple Interface to SRAM FPGAs
- Compatible with Atmel AT6000, AT40K and AT94K Devices, Altera FLEX<sup>®</sup>, APEX<sup>™</sup> Devices, Lucent ORCA<sup>®</sup> FPGAs, Xilinx XC3000<sup>™</sup>, XC4000<sup>™</sup>, XC5200<sup>™</sup>, Spartan<sup>®</sup>, Virtex<sup>®</sup> FPGAs, Motorola MPA1000 FPGAs
- Cascadable Read-back to Support Additional Configurations or Higher-density Arrays
- Very Low-power CMOS EEPROM Process
- Programmable Reset Polarity
- Available 8-lead PDIP, 20-lead PLCC and 32-lead TQFP Packages (Pin Compatible Across Product Family)
- Emulation of Atmel's AT24CXXX Serial EEPROMs
- Low-power Standby Mode

## Description

The AT17A series FPGA configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17A series device is packaged in the 8-lead PDIP<sup>(1)</sup>, 20-lead PLCC and 32-lead TQFP, see Table 1. The AT17A series configurator uses a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes. These devices also support a write-protection mechanism within its programming mode.

Note: 1. The 8-lead LAP and SOIC packages for the AT17LV65A/128A/256A do not have an A label. However, the 8-lead packages are pin compatible with the 8-lead package of Altera's EEPROMs, refer to the AT17LV65/128/256/512/010/002/040 datasheet available on the Atmel web site for more information.

The AT17A series configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

Table 1. AT17A Series Packages

| Package      | AT17LV65A/<br>AT17LV128A/<br>AT17LV256A | AT17LV512A | AT17LV010A | AT17LV002A | AT17LV040A |
|--------------|-----------------------------------------|------------|------------|------------|------------|
| 8-lead PDIP  | Yes                                     | Yes        | Yes        | —          | —          |
| 20-lead PLCC | Yes                                     | Yes        | Yes        | Yes        | —          |
| 32-lead TQFP | —                                       | —          | Yes        | Yes        | Yes        |



## FPGA Configuration EEPROM Memory

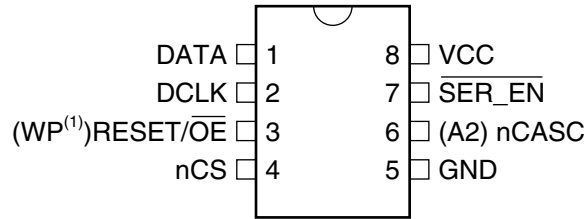
AT17LV65A  
AT17LV128A  
AT17LV256A  
AT17LV512A  
AT17LV010A  
AT17LV002A  
AT17LV040A

## 3.3V to 5V System Support

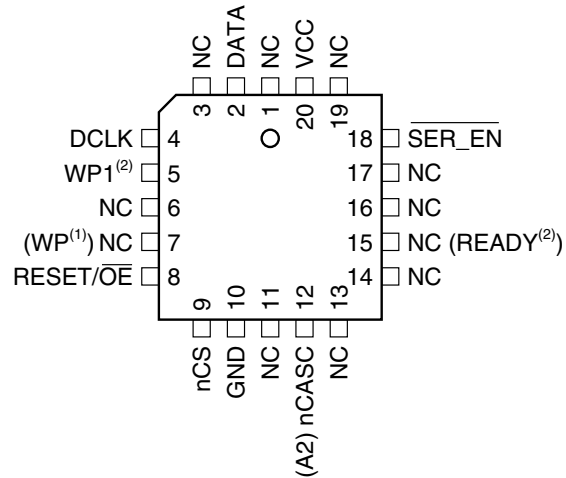


## Pin Configuration

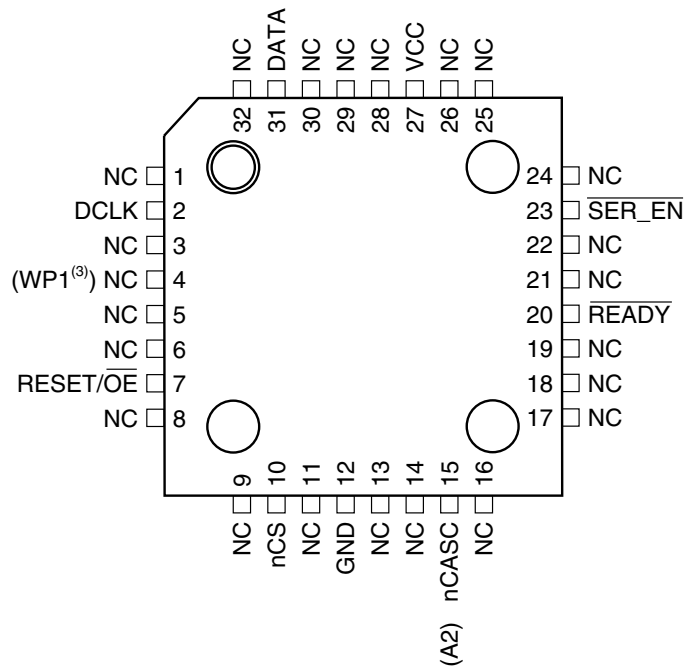
**8-lead PDIP**



**20-lead PLCC**

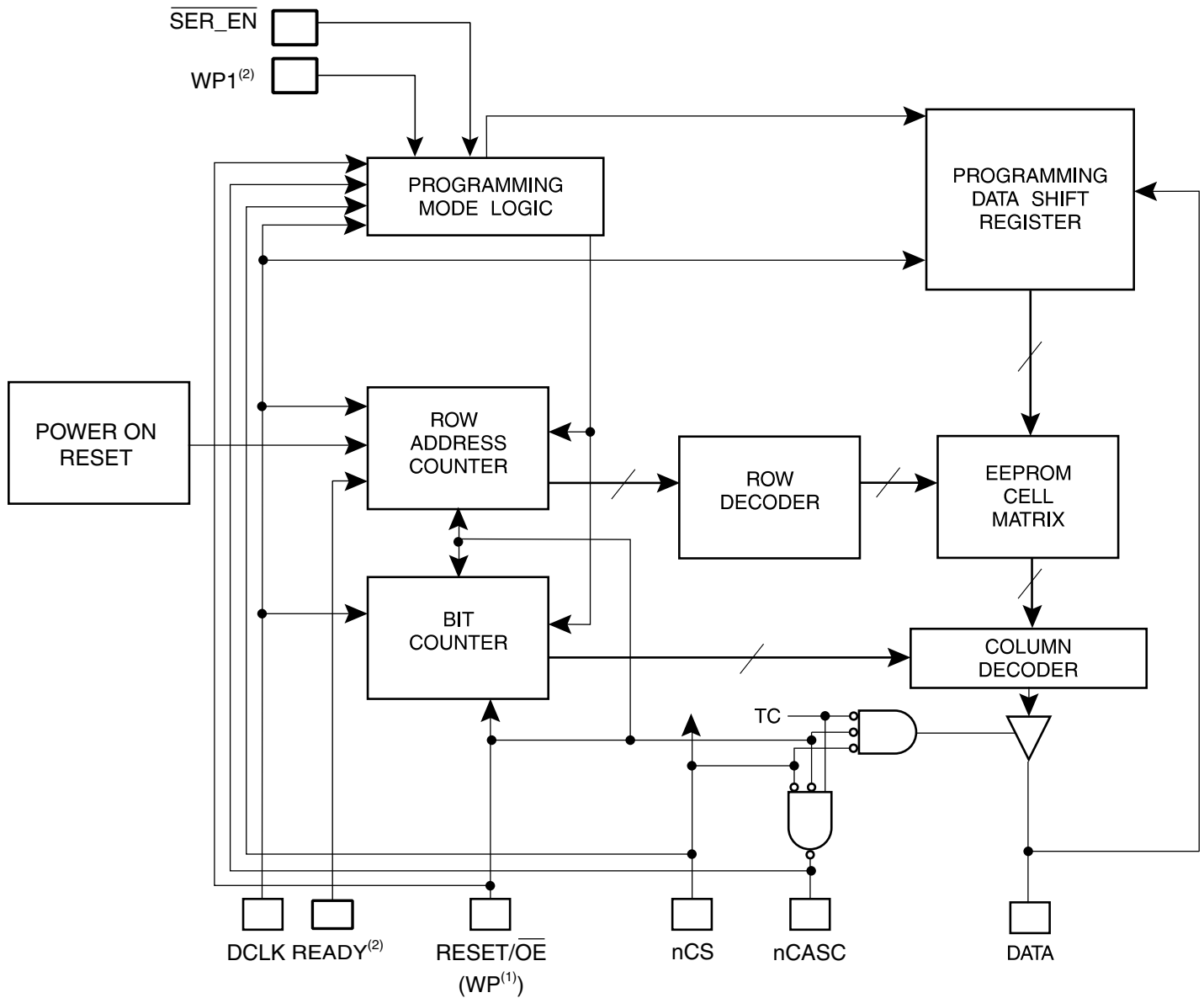


**32-lead TQFP**



- Notes:
1. This pin is only available on AT17LV65A/128A/256A devices.
  2. This pin is only available on AT17LV512A/010A/002A devices.
  3. This pin is only available on AT17LV010A/002A devices.

## Block Diagram



- Notes:
1. This pin is only available on AT17LV65A/128A/256A devices.
  2. This pin is only available on AT17LV512A/010A/002A/040A devices.



## Device Description

The control signals for the configuration EEPROM ( $\overline{\text{nCS}}$ ,  $\overline{\text{RESET/OE}}$  and  $\text{DCLK}$ ) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external controller.

The configuration EEPROM's  $\overline{\text{RESET/OE}}$  and  $\overline{\text{nCS}}$  pins control the tri-state buffer on the DATA output pin and enable the address counter and the oscillator. When  $\overline{\text{RESET/OE}}$  is driven Low, the configuration EEPROM resets its address counter and tri-states its DATA pin. The  $\overline{\text{nCS}}$  pin also controls the output of the AT17A series configurator. If  $\overline{\text{nCS}}$  is held High after the  $\overline{\text{RESET/OE}}$  pulse, the counter is disabled and the DATA output pin is tri-stated. When  $\overline{\text{nCS}}$  is driven subsequently Low, the counter and the DATA output pin are enabled. When  $\overline{\text{RESET/OE}}$  is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of the  $\overline{\text{nCS}}$ .

When the configurator has driven out all of its data and  $\overline{\text{nCASC}}$  is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This is the default setting for the device. Since almost all FPGAs use RESET Low and OE High, this document will describe  $\overline{\text{RESET/OE}}$ .

## Pin Description

| Name            | I/O | AT17LV65A/<br>AT17LV128A/<br>AT17LV256A | AT17LV512A/<br>AT17LV010A |            |            | AT17LV002A |            | AT17LV040A |
|-----------------|-----|-----------------------------------------|---------------------------|------------|------------|------------|------------|------------|
|                 |     | 20<br>PLCC                              | 8<br>PDIP                 | 20<br>PLCC | 32<br>TQFP | 20<br>PLCC | 32<br>TQFP | 32<br>PLCC |
| DATA            | I/O | 2                                       | 1                         | 2          | 31         | 2          | 31         | 31         |
| DCLK            | I   | 4                                       | 2                         | 4          | 2          | 4          | 2          | 2          |
| WP1             | I   | –                                       | –                         | 5          | 4          | 5          | 4          | –          |
| RESET/ŌE        | I   | 8                                       | 3                         | 8          | 7          | 8          | 7          | 7          |
| WP              | I   |                                         |                           | –          | –          | –          | –          | –          |
| nCS             | I   | 9                                       | 4                         | 9          | 10         | 9          | 10         | 10         |
| GND             |     | 10                                      | 5                         | 10         | 12         | 10         | 12         | 12         |
| nCASC           | O   | 12                                      | 6                         | 12         | 15         | 12         | 15         | 15         |
| A2              | I   |                                         |                           |            |            |            |            |            |
| READY           | O   | –                                       | –                         | 15         | 20         | 15         | 20         | 20         |
| SER_EN          | I   | 18                                      | 7                         | 18         | 23         | 18         | 23         | 23         |
| V <sub>CC</sub> |     | 20                                      | 8                         | 20         | 27         | 20         | 27         | 27         |

### DATA

Three-state DATA output for configuration. Open-collector bi-directional pin for programming.

### DCLK

Clock output or clock input. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the RESET/ $\overline{\text{OE}}$  input is held High, the nCS input is held Low, and all configuration data has not been transferred to the target device (otherwise, as the master device, the DCLK pin drives Low).

### WP1

WRITE PROTECT (1). This pin is used to protect portions of memory during programming, and it is disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations. This pin is only available on AT17LV512A/010A/002A devices.

### RESET/ $\overline{\text{OE}}$

Output Enable (active High) and RESET (active Low) when  $\overline{\text{SER\_EN}}$  is High. A Low logic level resets the address counter. A High logic level (with nCS Low) enables DATA and permits the address counter to count. In the mode, if this pin is Low (reset), the internal oscillator becomes inactive and DCLK drives Low. The logic polarity of this input is programmable and must be programmed active High (RESET active Low) by the user during programming for Altera applications.

### WP

Write protect (WP) input (when nCS is Low) during programming only ( $\overline{\text{SER\_EN}}$  Low). When WP is Low, the entire memory can be written. When WP is enabled (High), the lowest block of the memory cannot be written. This pin is only available on AT17LV65A/128A/256A devices.



|                                               |                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>nCS</b>                                    | Chip Select input (active Low). A Low input (with OE High) allows DCLK to increment the address counter and enables DATA to drive out. If the AT17A series is reset with nCS Low, the device initializes as the first (and master) device in a daisy-chain. If the AT17A series is reset with nCS High, the device initializes as a subsequent AT17A series device in the chain.    |
| <b>GND</b>                                    | Ground pin. A 0.2 $\mu$ F decoupling capacitor between $V_{CC}$ and GND is recommended.                                                                                                                                                                                                                                                                                             |
| <b>nCASC</b>                                  | Cascade Select Output (active Low). This output goes Low when the address counter has reached its maximum value. In a daisy-chain of AT17A series devices, the nCASC pin of one device is usually connected to the nCS input pin of the next device in the chain, which permits DCLK from the master configurator to clock data from a subsequent AT17A series device in the chain. |
| <b>A2</b>                                     | Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low). A2 has an internal pull-down resistor.                                                                                                                                                                                                |
| <b>READY</b>                                  | Open collector reset state indicator. Driven Low during power-on reset cycle, released when power-up is complete. (recommended 4.7 k $\Omega$ pull-up on this pin if used).                                                                                                                                                                                                         |
| <b><math>\overline{\text{SER\_EN}}</math></b> | Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the 2-wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER\_EN}}$ should be tied to $V_{CC}$ .                                                                                                                                             |
| <b><math>V_{CC}</math></b>                    | +3.3V (-10%) to 5.0V (+10%) power supply pin. AT17LV(A) devices with date codes of 0902 and later are tested to an extended voltage range. These parts can now be used in both 3.3V (-10%) to 5.0V (+10%) applications and replace the AT17C(A) 5V-only devices.                                                                                                                    |

## **FPGA Master Serial Mode Summary**

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17A Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

This document discusses the Altera FLEX FPGA device interfaces

## **Control of Configuration**

Most connections between the FPGA device and the AT17A Serial EEPROM are simple and self-explanatory.

- The DATA output of the AT17A series configurator drives DIN of the FPGA devices.
- The master FPGA DCLK output or external clock source drives the DCLK input of the AT17A series configurator.
- The nCASC output of any AT17A series configurator drives the nCS input of the next configurator in a cascaded chain of EEPROMs.
- $\overline{\text{SER\_EN}}$  must be connected to  $V_{CC}$  (except during ISP).

## **Cascading Serial Configuration EEPROMs**

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the next clock signal to the configurator asserts its nCASC output low and disables its DATA line driver. The second configurator recognizes the low level on its nCS input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the RESET/ $\overline{\text{OE}}$  on each configurator is driven to a Low level.

If the address counters are not to be reset upon completion, then the RESET/ $\overline{\text{OE}}$  input can be tied to a High level.

## **AT17A Series Reset Polarity**

The AT17A series configurator allows the user to program the polarity of the RESET/ $\overline{\text{OE}}$  pin as either RESET/ $\overline{\text{OE}}$  or RESET/OE. This feature is supported by industry-standard programmer algorithms.

## **Programming Mode**

The programming mode is entered by bringing  $\overline{\text{SER\_EN}}$  Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at  $V_{CC}$  supply only. Programming super voltages are generated inside the chip.

## **Standby Mode**

The AT17LV65A/128A/256A enters a low-power standby mode whenever nCS is asserted High. In this mode, the configurator consumes less than 50  $\mu\text{A}$  of current at 3.3V (100  $\mu\text{A}$  for the AT17LV512A/010A/002A/040A). The output remains in a high-impedance state regardless of the state of the RESET/ $\overline{\text{OE}}$  input.

## Absolute Maximum Ratings\*

|                                                    |                          |
|----------------------------------------------------|--------------------------|
| Operating Temperature.....                         | -55°C to +125°C          |
| Storage Temperature.....                           | -65°C to +150°C          |
| Voltage on Any Pin<br>with Respect to Ground ..... | -0.1V to $V_{CC} + 0.5V$ |
| Supply Voltage ( $V_{CC}$ ) .....                  | -0.5V to +7.0V           |
| Maximum Soldering Temp. (10 sec. @ 1/16 in.).....  | 260°C                    |
| ESD ( $R_{ZAP} = 1.5K$ , $C_{ZAP} = 100$ pF).....  | 2000V                    |

**\*NOTICE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Operating Conditions

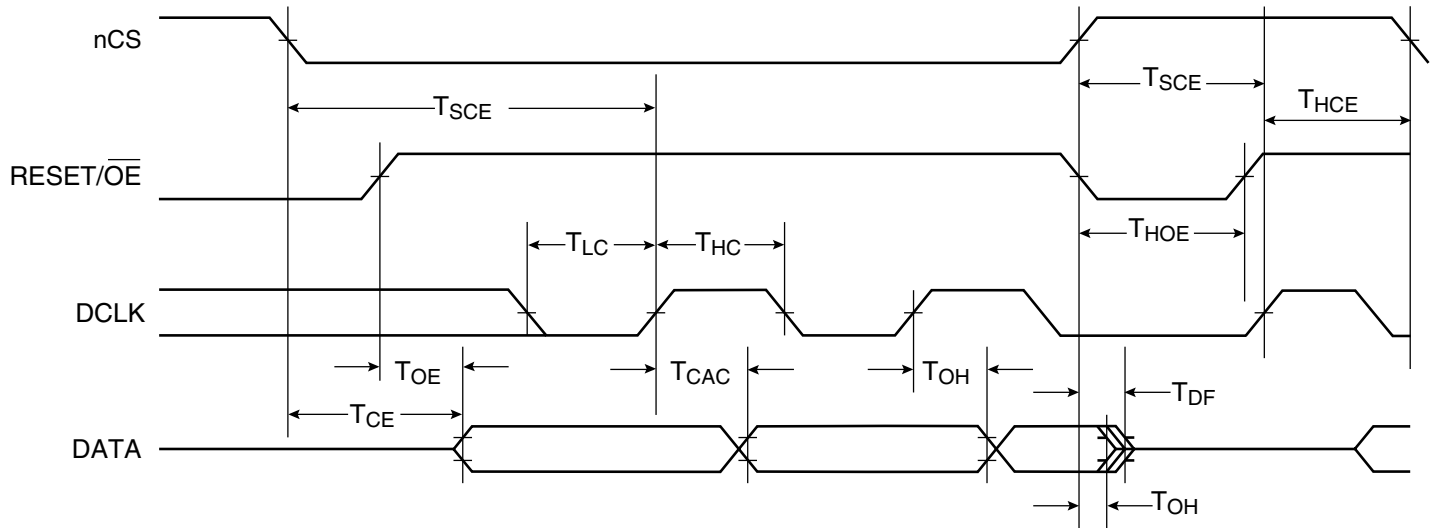
| Symbol   | Description |                                                   | AT17LV65A/<br>AT17LV128A/<br>AT17LV256A/<br>AT17LV512A/<br>AT17LV010A |     | AT17LV002A/<br>AT17LV040A |     | Units |
|----------|-------------|---------------------------------------------------|-----------------------------------------------------------------------|-----|---------------------------|-----|-------|
|          |             |                                                   | Min                                                                   | Max | Min                       | Max |       |
| $V_{CC}$ | Commercial  | Supply voltage relative to GND<br>-0°C to +70°C   | 3.0                                                                   | 5.5 | 3.15                      | 5.5 | V     |
|          | Industrial  | Supply voltage relative to GND<br>-40°C to +85°C  | 3.0                                                                   | 5.5 | 3.15                      | 5.5 | V     |
|          | Military    | Supply voltage relative to GND<br>-55°C to +125°C | 3.0                                                                   | 5.5 | 3.15                      | 5.5 | V     |

## DC Characteristics

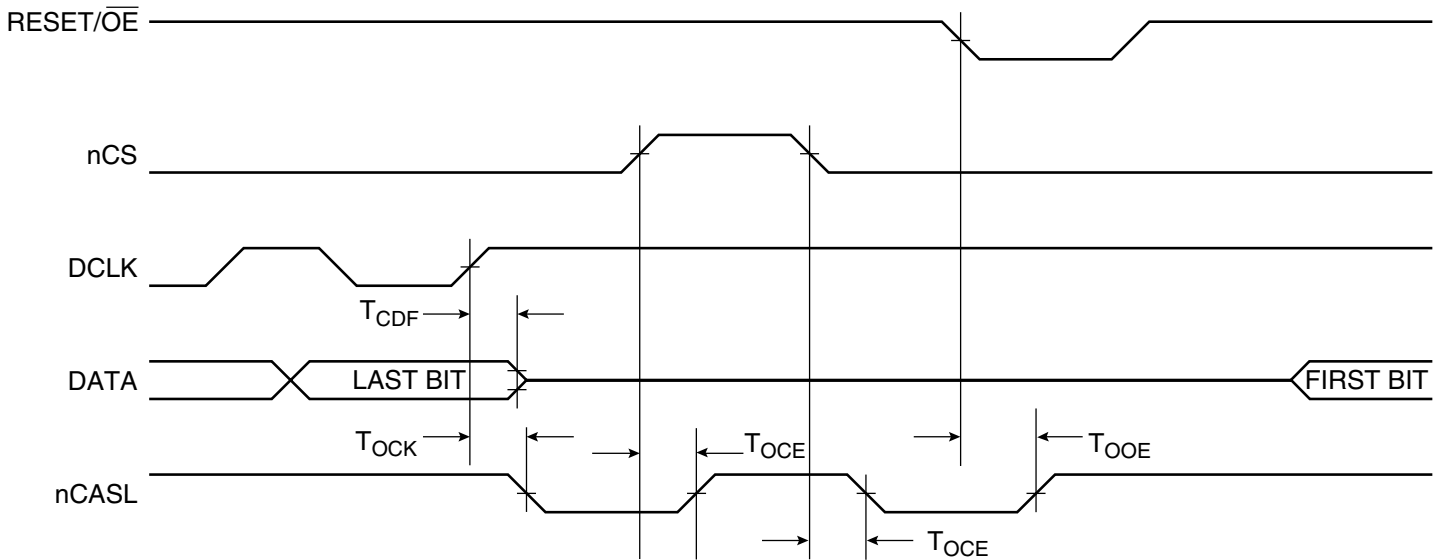
| Symbol           | Description                                                                |                         | AT17LV65A/<br>AT17LV128A/<br>AT17LV256A |                 | AT17LV512A/<br>AT17LV010A |                 | AT17LV002A/<br>AT17LV040A |                 | Units |
|------------------|----------------------------------------------------------------------------|-------------------------|-----------------------------------------|-----------------|---------------------------|-----------------|---------------------------|-----------------|-------|
|                  |                                                                            |                         | Min                                     | Max             | Min                       | Max             | Min                       | Max             |       |
| V <sub>IH</sub>  | High-level Input Voltage                                                   |                         | 2.0                                     | V <sub>CC</sub> | 2.0                       | V <sub>CC</sub> | 2.0                       | V <sub>CC</sub> | V     |
| V <sub>IL</sub>  | Low-level Input Voltage                                                    |                         | 0                                       | 0.8             | 0                         | 0.8             | 0                         | 0.8             | V     |
| V <sub>OH</sub>  | High-level Output Voltage (I <sub>OH</sub> = -2.5 mA)                      | Commercial              | 2.4                                     |                 | 2.4                       |                 | 2.4                       |                 | V     |
| V <sub>OL</sub>  | Low-level Output Voltage (I <sub>OL</sub> = +3 mA)                         |                         |                                         | 0.4             |                           | 0.4             |                           | 0.4             | V     |
| V <sub>OH</sub>  | High-level Output Voltage (I <sub>OH</sub> = -2 mA)                        | Industrial              | 2.4                                     |                 | 2.4                       |                 | 2.4                       |                 | V     |
| V <sub>OL</sub>  | Low-level Output Voltage (I <sub>OL</sub> = +3 mA)                         |                         |                                         | 0.4             |                           | 0.4             |                           | 0.4             | V     |
| V <sub>OH</sub>  | High-level Output Voltage (I <sub>OH</sub> = -2 mA)                        | Military                | 2.4                                     |                 | 2.4                       |                 | 2.4                       |                 | V     |
| V <sub>OL</sub>  | Low-level Output Voltage (I <sub>OL</sub> = +2.5 mA)                       |                         |                                         | 0.4             |                           | 0.4             |                           | 0.4             | V     |
| I <sub>CCA</sub> | Supply Current, Active Mode                                                |                         |                                         | 5               |                           | 5               |                           | 5               | mA    |
| I <sub>L</sub>   | Input or Output Leakage Current (V <sub>IN</sub> = V <sub>CC</sub> or GND) |                         | -10                                     | 10              | -10                       | 10              | -10                       | 10              | μA    |
| I <sub>CCS</sub> | Supply Current, Standby Mode                                               | Commercial              |                                         | 50              |                           | 100             |                           | 100             | μA    |
|                  |                                                                            | Industrial/<br>Military |                                         | 100             |                           | 100             |                           | 100             | μA    |



## AC Characteristics



## AC Characteristics when Cascading



## AC Characteristics

| Symbol          | Description                                               |                         | AT17LV65A/<br>AT17LV128A/<br>AT17LV256A |     | AT17LV512A/<br>AT17LV010A |     | AT17LV002A |     | AT17LV040A |     | Units |
|-----------------|-----------------------------------------------------------|-------------------------|-----------------------------------------|-----|---------------------------|-----|------------|-----|------------|-----|-------|
|                 |                                                           |                         | Min                                     | Max | Min                       | Max | Min        | Max | Min        | Max |       |
| $T_{OE}^{(2)}$  | RESET/ $\overline{OE}$ to Data Delay                      | Commercial              |                                         | 50  |                           | 50  |            | 50  |            | 50  | ns    |
|                 |                                                           | Military <sup>(1)</sup> |                                         | 55  |                           | 55  |            | 55  |            | 55  | ns    |
| $T_{CE}^{(2)}$  | nCS to Data Delay                                         | Commercial              |                                         | 60  |                           | 55  |            | 55  |            | 55  | ns    |
|                 |                                                           | Military <sup>(1)</sup> |                                         | 60  |                           | 60  |            | 60  |            | 60  | ns    |
| $T_{CAC}^{(2)}$ | DCLK to Data Delay                                        | Commercial              |                                         | 75  |                           | 60  |            | 60  |            | 60  | ns    |
|                 |                                                           | Military <sup>(1)</sup> |                                         | 80  |                           | 65  |            | 65  |            | 65  | ns    |
| $T_{OH}$        | Data Hold from nCS,<br>OE, or DCLK                        | Commercial              | 0                                       |     | 0                         |     | 0          |     | 0          |     | ns    |
|                 |                                                           | Military <sup>(1)</sup> | 0                                       |     | 0                         |     | 0          |     | 0          |     | ns    |
| $T_{DF}^{(3)}$  | nCS or OE to Data<br>Float Delay                          | Commercial              |                                         | 55  |                           | 50  |            | 50  |            | 50  | ns    |
|                 |                                                           | Military <sup>(1)</sup> |                                         | 55  |                           | 50  |            | 50  |            | 50  | ns    |
| $T_{LC}$        | DCLK Low Time                                             | Commercial              | 25                                      |     | 20                        |     | 20         |     | 20         |     | ns    |
|                 |                                                           | Military <sup>(1)</sup> | 25                                      |     | 20                        |     | 20         |     | 20         |     | ns    |
| $T_{HC}$        | DCLK High Time                                            | Commercial              | 25                                      |     | 20                        |     | 20         |     | 20         |     | ns    |
|                 |                                                           | Military <sup>(1)</sup> | 25                                      |     | 20                        |     | 20         |     | 20         |     | ns    |
| $T_{SCE}$       | nCS Setup Time to DCLK<br>(to guarantee proper counting)  | Commercial              | 35                                      |     | 20                        |     | 20         |     | 20         |     | ns    |
|                 |                                                           | Military <sup>(1)</sup> | 50                                      |     | 25                        |     | 25         |     | 25         |     | ns    |
| $T_{HCE}$       | nCS Hold Time from DCLK<br>(to guarantee proper counting) | Commercial              | 0                                       |     | 0                         |     | 0          |     | 0          |     | ns    |
|                 |                                                           | Military <sup>(1)</sup> | 0                                       |     | 0                         |     | 0          |     | 0          |     | ns    |
| $T_{HOE}$       | OE Low Time<br>(guarantees counter is reset)              | Commercial              | 25                                      |     | 20                        |     | 20         |     | 20         |     | ns    |
|                 |                                                           | Military <sup>(1)</sup> | 25                                      |     | 20                        |     | 20         |     | 20         |     | ns    |
| $F_{MAX}$       | Maximum Input<br>Clock Frequency                          | Commercial              | 10                                      |     | 15                        |     | 15         |     | 15         |     | MHz   |
|                 |                                                           | Military <sup>(1)</sup> | 10                                      |     | 10                        |     | 10         |     | 10         |     | MHz   |
| $T_{LC}$        | DCLK Low Time Master Mode                                 | Commercial              |                                         |     | 30                        | 300 | 30         | 300 |            |     | ns    |
|                 |                                                           | Military <sup>(1)</sup> |                                         |     | 30                        | 300 | 30         | 300 |            |     | ns    |
| $T_{HC}$        | DCLK High Time<br>Master Mode                             | Commercial              |                                         |     | 30                        | 300 | 30         | 300 |            |     | ns    |
|                 |                                                           | Military <sup>(1)</sup> |                                         |     | 30                        | 300 | 30         | 300 |            |     | ns    |
| $V_{RDY}$       | Ready Pin Open<br>Collector Voltage                       | Commercial              |                                         |     | 1.2                       | 2.4 | 1.2        | 2.4 |            |     | V     |
|                 |                                                           | Military <sup>(1)</sup> |                                         |     | 1.2                       | 2.4 | 1.2        | 2.4 |            |     | V     |

- Notes:
1. Preliminary specifications for military operating range only.
  2. AC test lead = 50 pF.
  3. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady-state active levels.

## AC Characteristics when Cascading

| Symbol          | Description                              |                                        | AT17LV65A/<br>AT17LV128A/<br>AT17LV256A |     | AT17LV512A/<br>AT17LV010A |     | AT17LV002A |     | AT17LV040A |     | Units |
|-----------------|------------------------------------------|----------------------------------------|-----------------------------------------|-----|---------------------------|-----|------------|-----|------------|-----|-------|
|                 |                                          |                                        | Min                                     | Max | Min                       | Max | Min        | Max | Min        | Max |       |
| $T_{CDF}^{(3)}$ | DCLK to Data Float Delay                 | Commercial                             |                                         | 60  |                           | 50  |            | 50  |            | 50  | ns    |
|                 |                                          | Industrial/<br>Military <sup>(1)</sup> |                                         | 60  |                           | 50  |            | 50  |            | 50  | ns    |
| $T_{OCK}^{(2)}$ | DCLK to nCASC Delay                      | Commercial                             |                                         | 55  |                           | 50  |            | 50  |            | 50  | ns    |
|                 |                                          | Industrial/<br>Military <sup>(1)</sup> |                                         | 60  |                           | 55  |            | 55  |            | 55  | ns    |
| $T_{OCE}^{(2)}$ | nCS to nCASC Delay                       | Commercial                             |                                         | 55  |                           | 35  |            | 35  |            | 35  | ns    |
|                 |                                          | Industrial/<br>Military <sup>(1)</sup> |                                         | 60  |                           | 40  |            | 40  |            | 40  | ns    |
| $T_{OOE}^{(2)}$ | RESET/ $\overline{OE}$ to<br>nCASC Delay | Commercial                             |                                         | 40  |                           | 35  |            | 35  |            | 35  | ns    |
|                 |                                          | Industrial/<br>Military <sup>(1)</sup> |                                         | 45  |                           | 35  |            | 35  |            | 35  | ns    |
| $F_{MAX}$       | Maximum Input<br>Clock Frequency         | Commercial                             | 8                                       |     | 12.5                      |     | 12         |     | 12         |     | ns    |
|                 |                                          | Industrial/<br>Military <sup>(1)</sup> | 8                                       |     | 10                        |     | 10         |     | 10         |     | ns    |

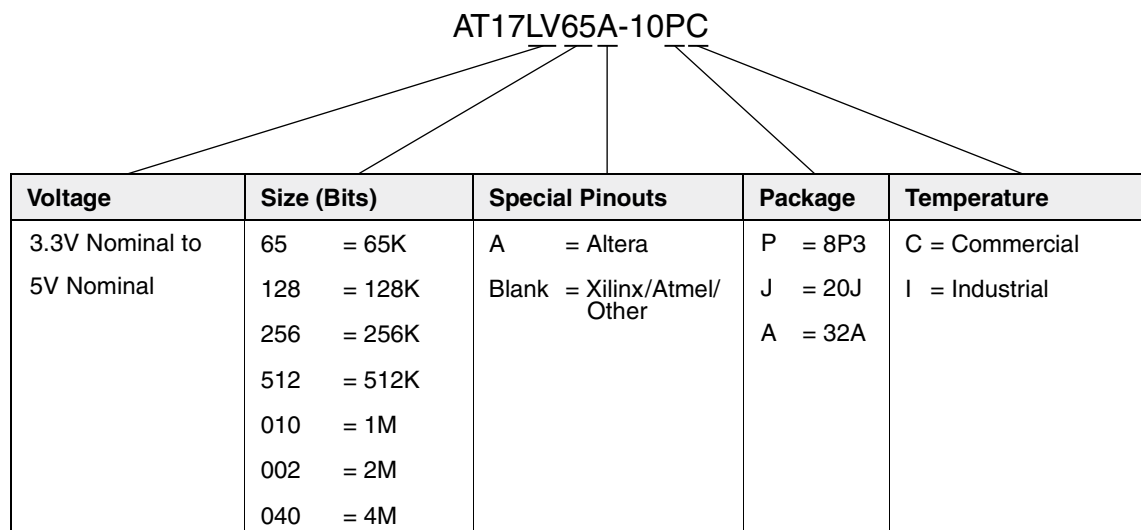
- Notes:
1. Preliminary specifications for military operating range only.
  2. AC test lead = 50 pF.
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## Thermal Resistance Coefficients<sup>(1)</sup>

| Package Type |                                       |                                     | AT17LV65A/<br>AT17LV128A/<br>AT17LV256A | AT17LV512A/<br>AT17LV010A | AT17LV002A | AT17LV040A |
|--------------|---------------------------------------|-------------------------------------|-----------------------------------------|---------------------------|------------|------------|
| 8P3          | Plastic Dual Inline Package (PDIP)    | $\theta_{JC}$ [°C/W]                |                                         | 37                        |            |            |
|              |                                       | $\theta_{JA}$ [°C/W] <sup>(2)</sup> |                                         | 107                       |            |            |
| 20J          | Plastic Leaded Chip Carrier (PLCC)    | $\theta_{JC}$ [°C/W]                | 35                                      | 35                        | 35         |            |
|              |                                       | $\theta_{JA}$ [°C/W] <sup>(2)</sup> | 90                                      | 90                        | 90         |            |
| 32A          | Thin Plastic Quad Flat Package (TQFP) | $\theta_{JC}$ [°C/W]                |                                         |                           |            |            |
|              |                                       | $\theta_{JA}$ [°C/W] <sup>(2)</sup> |                                         |                           |            |            |

Notes: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages”, available on the Atmel web site, at <http://www.atmel.com/atmel/acrobat/doc0636.pdf>.  
 2. Airflow = 0 ft/min.

**Figure 1.** Ordering Code<sup>(1)</sup>



Note: 1. The 8-lead LAP and SOIC packages for the AT17LV65A/128A/256A do not have an A label. However, the 8-lead packages are pin compatible with the 8-lead package of Altera's EEPROMs, refer to the AT17LV65/128/256/512/010/002/040 datasheet available on the Atmel web site for more information.

| Package Type |                                                                 |
|--------------|-----------------------------------------------------------------|
| <b>8P3</b>   | 8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)         |
| <b>20J</b>   | 20-lead, Plastic J-leaded Chip Carrier (PLCC)                   |
| <b>32A</b>   | 32-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP) |

## Ordering Information<sup>(1)</sup>

| Memory Size             | Ordering Code   | Package | Operation Range               |
|-------------------------|-----------------|---------|-------------------------------|
| 64-Kbit <sup>(2)</sup>  | AT17LV65A-10JC  | 20J     | Commercial<br>(0°C to 70°C)   |
|                         | AT17LV65A-10JI  | 20J     | Industrial<br>(-40°C to 85°C) |
| 128-Kbit                | AT17LV128A-10JC | 20J     | Commercial<br>(0°C to 70°C)   |
|                         | AT17LV128A-10JI | 20J     | Industrial<br>(-40°C to 85°C) |
| 256-Kbit <sup>(3)</sup> | AT17LV256A-10JC | 20J     | Commercial<br>(0°C to 70°C)   |
|                         | AT17LV256A-10JI | 20J     | Industrial<br>(-40°C to 85°C) |
| 512-Kbit <sup>(4)</sup> | AT17LV512A-10PC | 8P3     | Commercial<br>(0°C to 70°C)   |
|                         | AT17LV512A-10JC | 20J     |                               |
|                         | AT17LV512A-10PI | 8P3     | Industrial<br>(-40°C to 85°C) |
|                         | AT17LV512A-10JI | 20J     |                               |
| 1-Mbit <sup>(5)</sup>   | AT17LV010A-10PC | 8P3     | Commercial<br>(0°C to 70°C)   |
|                         | AT17LV010A-10JC | 20J     |                               |
|                         | AT17LV010A-10QC | 32A     |                               |
|                         | AT17LV010A-10PI | 8P3     | Industrial<br>(-40°C to 85°C) |
|                         | AT17LV010A-10JI | 20J     |                               |
|                         | AT17LV010A-10QI | 32A     |                               |
| 2-Mbit <sup>(6)</sup>   | AT17LV002A-10JC | 20J     | Commercial<br>(0°C to 70°C)   |
|                         | AT17LV002A-10QC | 32A     |                               |
|                         | AT17LV002A-10JI | 20J     | Industrial<br>(-40°C to 85°C) |
|                         | AT17LV002A-10QI | 32A     |                               |
| 4-Mbit <sup>(7)</sup>   | AT17LV040A-10QC | 32A     | Commercial<br>(0°C to 70°C)   |
|                         | AT17LV040A-10QI | 32A     | Industrial<br>(-40°C to 85°C) |

Notes: 1. Currently, there are two types of low-density configurators. The new version will be identified by a "B" after the datacode. The "B" version is fully backward-compatible with the original devices so existing customers will not be affected. The new parts no longer require a MUX for ISP. See programming specification for more details.

2. Use 64-Kbit density parts to replace Altera EPC1064.

3. Use 256-Kbit density parts to replace Altera EPC1213.

4. Use 512-Kbit density parts to replace Altera EPC1441.

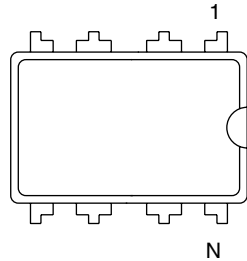
5. Use 1-Mbit density parts to replace Altera EPC1

6. Use 2-Mbit density parts to replace Altera EPC2. Atmel AT17LV002A devices do not support JTAG programming; Atmel AT17LV002A devices use a 2-wire serial interface for in-system programming.

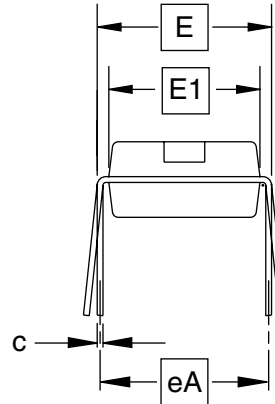
7. Use 4-Mbit density parts to replace Altera EPC4. Atmel AT17LV040A devices do not support JTAG programming; Atmel AT17LV040A devices use a 2-wire serial interface for in-system programming.

## Packaging Information

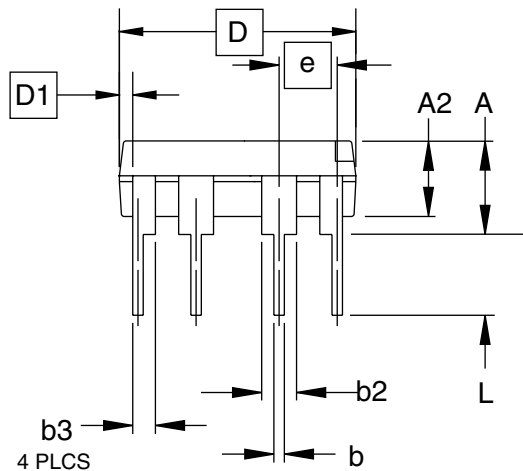
### 8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS  
(Unit of Measure = inches)

| SYMBOL | MIN       | NOM   | MAX   | NOTE |
|--------|-----------|-------|-------|------|
| A      |           |       | 0.210 | 2    |
| A2     | 0.115     | 0.130 | 0.195 |      |
| b      | 0.014     | 0.018 | 0.022 | 5    |
| b2     | 0.045     | 0.060 | 0.070 | 6    |
| b3     | 0.030     | 0.039 | 0.045 | 6    |
| c      | 0.008     | 0.010 | 0.014 |      |
| D      | 0.355     | 0.365 | 0.400 | 3    |
| D1     | 0.005     |       |       | 3    |
| E      | 0.300     | 0.310 | 0.325 | 4    |
| E1     | 0.240     | 0.250 | 0.280 | 3    |
| e      | 0.100 BSC |       |       |      |
| eA     | 0.300 BSC |       |       | 4    |
| L      | 0.115     | 0.130 | 0.150 | 2    |

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
  2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
  3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
  4. E and eA measured with the leads constrained to be perpendicular to datum.
  5. Pointed or rounded lead tips are preferred to ease insertion.
  6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual  
In-line Package (PDIP)

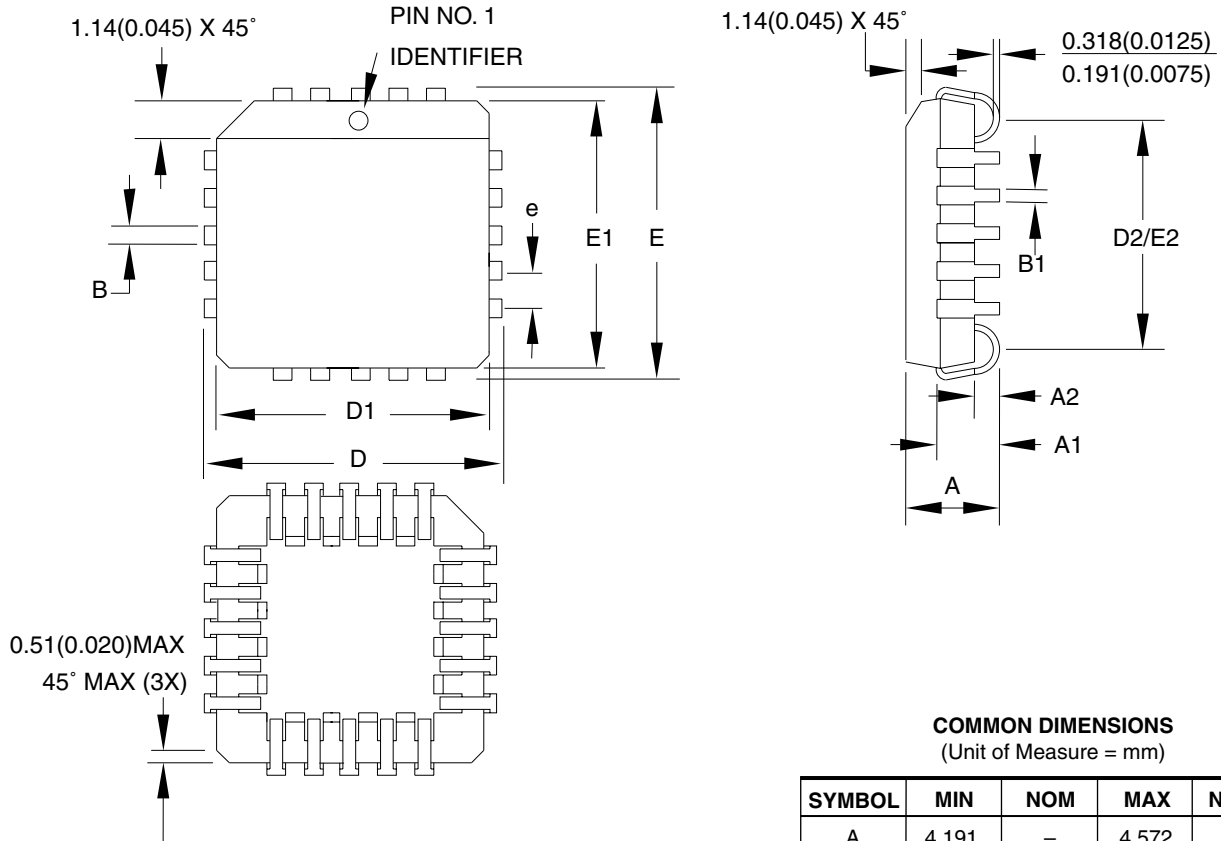
**DRAWING NO.**

8P3

**REV.**

B

## 20J – PLCC



- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN       | NOM | MAX    | NOTE   |
|--------|-----------|-----|--------|--------|
| A      | 4.191     | —   | 4.572  |        |
| A1     | 2.286     | —   | 3.048  |        |
| A2     | 0.508     | —   | —      |        |
| D      | 9.779     | —   | 10.033 |        |
| D1     | 8.890     | —   | 9.042  | Note 2 |
| E      | 9.779     | —   | 10.033 |        |
| E1     | 8.890     | —   | 9.042  | Note 2 |
| D2/E2  | 7.366     | —   | 8.382  |        |
| B      | 0.660     | —   | 0.813  |        |
| B1     | 0.330     | —   | 0.533  |        |
| e      | 1.270 TYP |     |        |        |

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

### TITLE

**20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)**

### DRAWING NO.

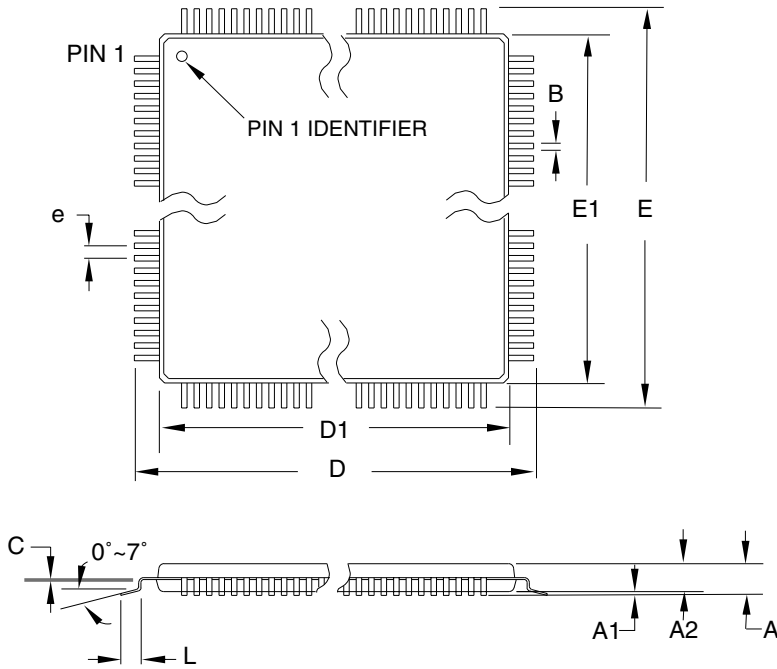
20J

### REV.

B



32A – TQFP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN      | NOM  | MAX  | NOTE   |
|--------|----------|------|------|--------|
| A      | –        | –    | 1.20 |        |
| A1     | 0.05     | –    | 0.15 |        |
| A2     | 0.95     | 1.00 | 1.05 |        |
| D      | 8.75     | 9.00 | 9.25 |        |
| D1     | 6.90     | 7.00 | 7.10 | Note 2 |
| E      | 8.75     | 9.00 | 9.25 |        |
| E1     | 6.90     | 7.00 | 7.10 | Note 2 |
| B      | 0.30     | –    | 0.45 |        |
| C      | 0.09     | –    | 0.20 |        |
| L      | 0.45     | –    | 0.75 |        |
| e      | 0.80 TYP |      |      |        |

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

|                                                                                                                                |                                                                                                                                                      |                           |                  |
|--------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------------------|
|  2325 Orchard Parkway<br>San Jose, CA 95131 | <b>TITLE</b><br><b>32A</b> , 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness,<br>0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | <b>DRAWING NO.</b><br>32A | <b>REV.</b><br>B |
|--------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------------------|



## **Atmel Headquarters**

### ***Corporate Headquarters***

2325 Orchard Parkway  
San Jose, CA 95131  
TEL 1(408) 441-0311  
FAX 1(408) 487-2600

### ***Europe***

Atmel Sarl  
Route des Arsenaux 41  
Case Postale 80  
CH-1705 Fribourg  
Switzerland  
TEL (41) 26-426-5555  
FAX (41) 26-426-5500

### ***Asia***

Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimhatsui  
East Kowloon  
Hong Kong  
TEL (852) 2721-9778  
FAX (852) 2722-1369

### ***Japan***

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
TEL (81) 3-3523-3551  
FAX (81) 3-3523-7581

## **Atmel Operations**

### ***Memory***

2325 Orchard Parkway  
San Jose, CA 95131  
TEL 1(408) 441-0311  
FAX 1(408) 436-4314

### ***Microcontrollers***

2325 Orchard Parkway  
San Jose, CA 95131  
TEL 1(408) 441-0311  
FAX 1(408) 436-4314

La Chantry  
BP 70602  
44306 Nantes Cedex 3, France  
TEL (33) 2-40-18-18-18  
FAX (33) 2-40-18-19-60

### ***ASIC/ASSP/Smart Cards***

Zone Industrielle  
13106 Rousset Cedex, France  
TEL (33) 4-42-53-60-00  
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906  
TEL 1(719) 576-3300  
FAX 1(719) 540-1759

Scottish Enterprise Technology Park  
Maxwell Building  
East Kilbride G75 0QR, Scotland  
TEL (44) 1355-803-000  
FAX (44) 1355-242-743

### ***RF/Automotive***

Theresienstrasse 2  
Postfach 3535  
74025 Heilbronn, Germany  
TEL (49) 71-31-67-0  
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906  
TEL 1(719) 576-3300  
FAX 1(719) 540-1759

### ***Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom***

Avenue de Rochepleine  
BP 123  
38521 Saint-Egreve Cedex, France  
TEL (33) 4-76-58-30-00  
FAX (33) 4-76-58-34-80

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***Atmel Programmable SLI Hotline***  
(408) 436-4119

***Atmel Programmable SLI e-mail***  
configurator@atmel.com

***FAQ***  
Available on web site

***e-mail***  
literature@atmel.com

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