This is an abbreviated datasheet.
Contact a Cypress representative
for complete specifications.

T-52-33-53

CY7C614

CYPRESS SEMICONDUCTOR

MBus Peripheral I/O Controller

Features

- Converts MBus cycles into cycles of 386SX protocol
- Allows MBus access to 8 on-board devices without requiring additional glue logic
- Performs MBus arbitration, supporting up to six masters
- Contains MBus watchdog timer

Introduction

The CY7C614 provides a means by which MBus slave accesses are transformed into accesses in 386SX protocol. That is, the MBus interface of the chip acts as an MBus slave, while the 386SX side acts as a master. Then, other logic can translate the 386 master cycles into bus cycles of a standard system bus, such as the AT.

Another function of the CY7C614 is to handle accesses to basic on-board devices, such as the boot PROM and serial ports. These do not proceed as 386SX cycles, but do use the 386 address and data buses. No additional "glue" logic is necessary to connect these to the CY7C614. The timing of the on-board cycles is programmable using internal registers. The CY7C614 is implemented in a standard 208-pin PQFP package.

The CY7C614 also contains two system-level functions. The first is the MBus arbitration logic, which supports up to six MBus masters. The second function is a watchdog timer for the MBus. If an MBus master gains control of the MBus and the bus is continuously busy for 204.8 microseconds without any acknowledgment appearing on the bus from the MBus slave, the watchdog timer will generate an MBus error acknowledgment.

Logic Block Diagram