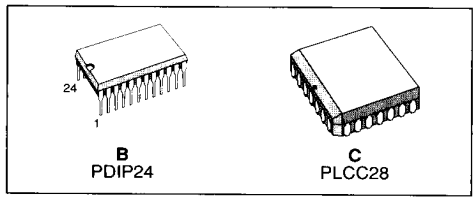
SGS-THOMSON MICROELECTRONICS

GAL20V8AS

E²PROM CMOS PROGRAMMABLE LOGIC DEVICE

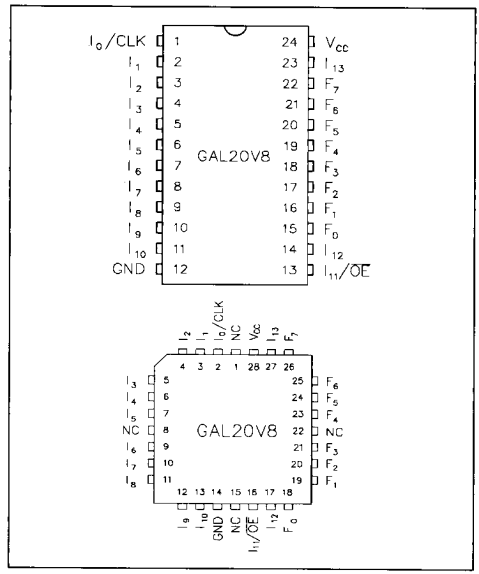
- HIGH PERFORMANCE SGS-THOMSON SINGLE-POLY E²PROM CMOS TECHNOLOGY
  - 10ns maximum propagation delay (GAL20V8AS-10*xxx*)
  - F_{max} = 62.5MHz
  - 7ns max. from clock input to data output
  - TTL compatible 24mA outputs
  - SGS-THOMSON proprietary Single-Poly F3-G™ technology
- GLITCH FREE DEVICE
  - Enhanced design minimises ground bounce
- VERY LOW POWER
  - 90mA typ. (115mA max.) I_{CC} Half power selection, 45mA typ. (55mA max.) I_{CC} Quarter power selection, 27mA typ. (30mA max.) I_{CC} Eighth power selection
- ELECTRICAL ERASABLE CELL TECHNOLOGY
  - Reconfigurable logic/reprogrammable cells
  - 100% tested: guaranteed 100% final programming yield
  - High speed electrical program & erase
- EIGHT OUTPUT MACROCELLS
  - Maximum flexibility for complex logic design
  - Programmable output polarity
  - Also emulates 21 types of 24 pin PAL® devices with full function/fuse map/parametric compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% functional testability
- ELECTRONIC SIGNATURE FOR USER'S IDENTIFICATION



B
PDIP24

C
PLCC28

Pin Connections



Pin Names

I_0–I_{13}	Input
CLK	Clock Input
F_0–F_7	I/O
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

DESCRIPTION

The GAL20V8AS, at 10ns maximum propagation delay time, combines a high performance CMOS process with Electrical Erasable Single-Poly F3-G™ technology — SGS-THOMSON proprietary — to provide one of the highest speed-power performance products available in PLD market.

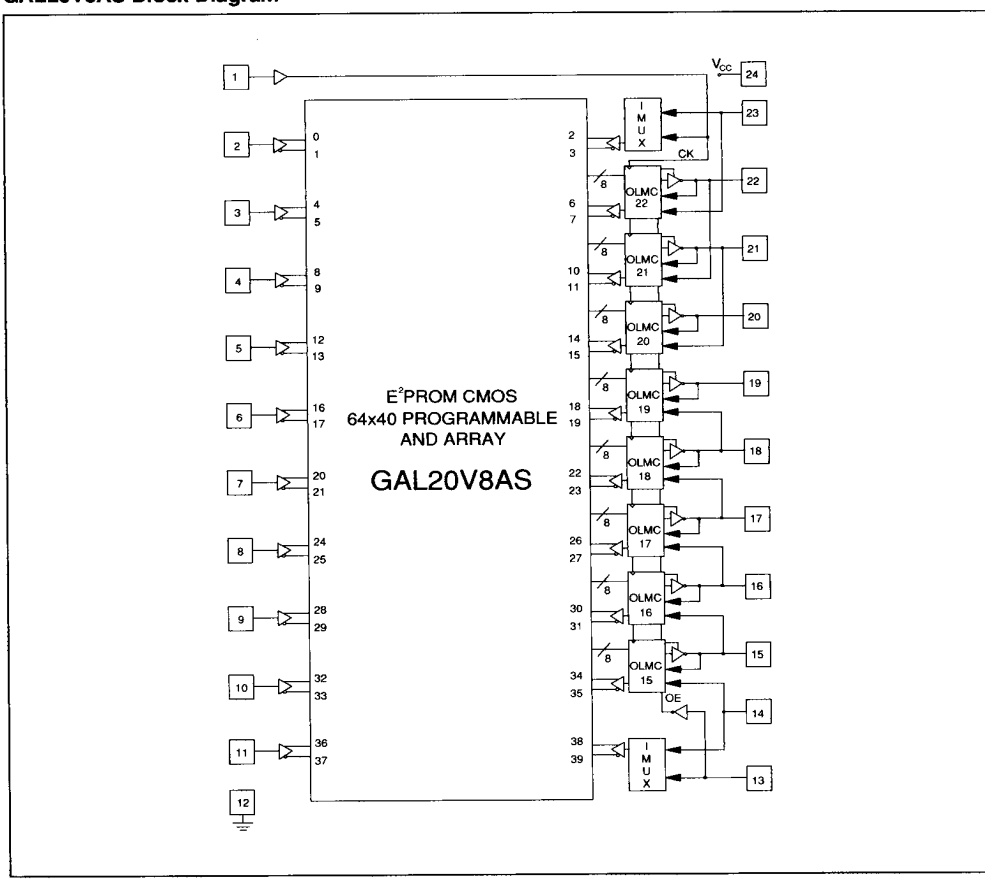
CMOS circuit allows GAL20V8AS to consume just 27mA (typ.) I_{CC} (Eighth power selection, 15ns) which represents a 75% saving in power when compared to its bipolar counterparts. Its E²PROM CMOS technology offers high speed (50ms) erase time providing the ability to reprogram or reconfigure the device quickly and efficiently.

GAL® is a registered trademark of Lattice Semiconductor Corp.; PAL® is a registered trademark of Monolithic Memories Inc.

GAL20V8AS features 8 programmable Output Logic Macro Cells (OLMCs) allowing each output to be configured by the user. Additionally, the GAL20V8AS is capable of emulating, in a functional/fuse map/parametric compatible mode, 21 types of 24 pin PAL® devices. Unique test circuits and reprogrammable cells allow complete AC, DC and functional testing during manufacture.

Therefore, SGS-THOMSON guarantees 100% field programmability and functionality of GAL® devices. SGS-THOMSON also guarantees 100 erase/write cycles and data retention exceeding 20 years.

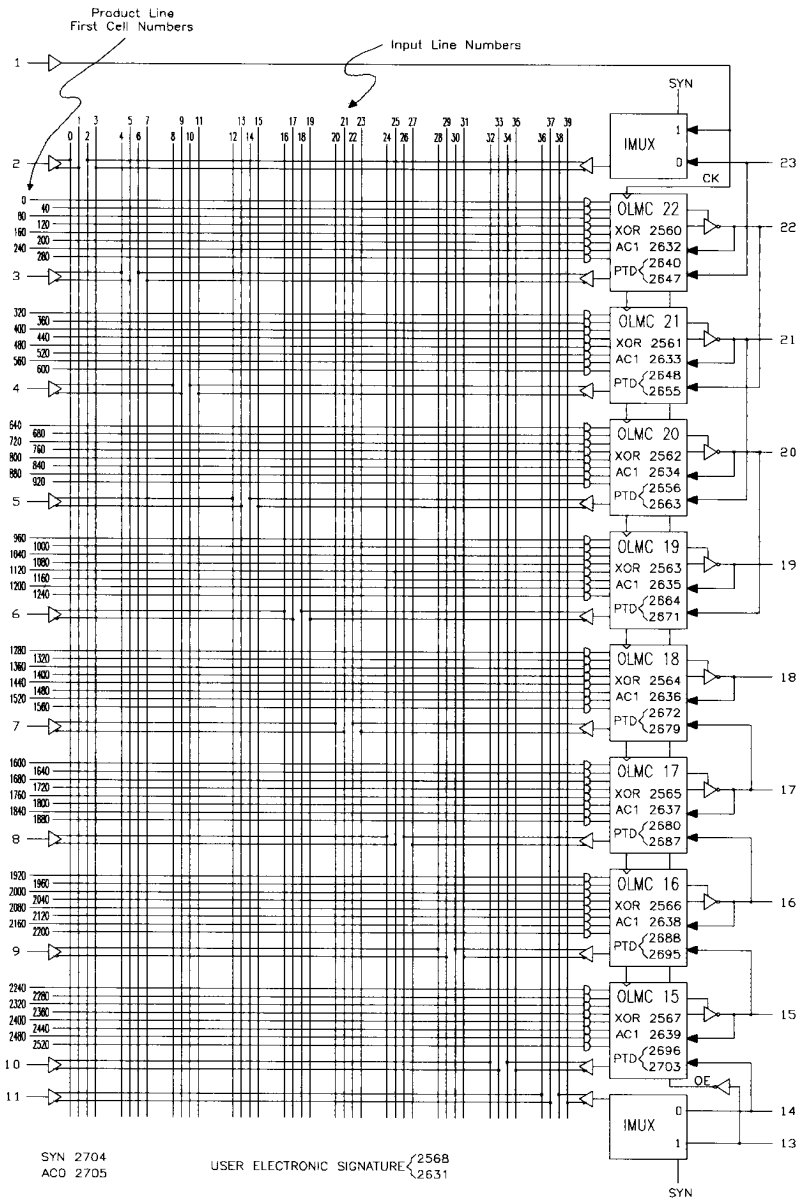
GAL20V8AS Block Diagram



GAL20V8AS PAL® Architecture Emulation

20L8	20R8	20RP6	20L2	18L4	16L6	14L8
20H8	20RP8	20R4	20H2	18H4	16H6	14H8
20P8	20R6	20RP4	20P2	18P4	16P6	14P8

GAL20V8AS Logic Diagram



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	Input Voltage Applied	-2.5 to V_{CC}+1	V
V_B	Off-State Output (Bidirectional) Voltage Applied	-2.5 to V_{CC}+1	V
T_{STG}	Storage Temperature	-65 to +125	°C
T_J	Junction Temperature (Operating)	-40 to +125	°C
T_L	Lead Temperature (Soldering)	260 (for 10s max.)	°C

Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

ESD Immunity

Test Method: Human Body Model (HBM)
ESD Tolerance ≥ 2000V
(See MIL-STD 883c).

Test Method: Charge Device Model (CDM)
ESD Tolerance ≥ 500V
Test Instrument: KeyTek ZapMaster

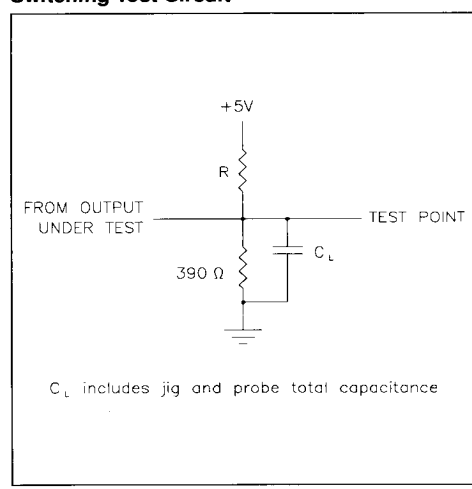
CDM is an additional test only for GAL®s not yet adopted as a company standard test.

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10%-90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure

3-state levels are measured 0.5V from steady-state active level.

Switching Test Circuit



Test Conditions

#	R [Ω]	C_L [pF]
1	200	50
2	Active High: ∞ Active Low: 200	50
3	Active High: ∞ Active Low: 200	5

Capacitance (T_A=25°C, f=1.0MHz, V_{CC}=5V)

Symbol	Parameter	Test Conditions	Maximum[+]	Units
C_I	Input Capacitance	V_I=2V	8	pF
C_B	Bidirectional Pin Capacitance	V_B=2V	10	pF

[+] Guarantied but not 100% tested.

DC Operating Conditions

Symbol	Parameter	Commercial Temperature Range		Industrial Temperature Range		Units
		Min.	Max.	Min.	Max.	
V_{CC}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_A	Ambient Temperature	0	70	-40	85	°C
V_{IL}	Input Low Voltage	V_{SS}*-0.5	0.8	V_{SS}*-0.5	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC}+1	2.0	V_{CC}+1	V
I_{OL}	Low Level Output Current	–	24	–	24	mA
I_{OH}	High Level Output Current	-3.2	–	-3.2	–	mA

* V_{SS} is the voltage applied to the GND pin.

Electrical Characteristics Over Operating Conditions (Commercial Temperature Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{IH}, I_{IL}	Input Leakage Current	$GND \le V_I \le V_{CC\ Max}$		–	±10	µA
I_{BH}, I_{BL}	Bidirectional Pin Leakage Current	$GND \le V_I \le V_{CC\ Max}$		–	±10	µA
I_{CC}	Operating Power Supply Current	f=15MHz (Q, E) f=25MHz (H) $V_{CC} = V_{CC\ Max}$ V_{IL}=0.5V V_{IH}=3.0V	Half Power	–	115	mA
			Quarter Power (only 15 and 20ns)	–	55	
			Eighth Power (only 15ns)	–	30	
I_{OS}*	Output Short Circuit Current	V_{CC}=5.0V, V_B=0.5V		-150	-30	mA
V_{OL}	Output Low Voltage	–		–	0.5	V
V_{OH}	Output High Voltage	–		2.4	–	V

Electrical Characteristics Over Operating Conditions (Industrial Temperature Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{IH}, I_{IL}	Input Leakage Current	$GND \le V_I \le V_{CC\ Max}$		–	±10	µA
I_{BH}, I_{BL}	Bidirectional Pin Leakage Current	$GND \le V_I \le V_{CC\ Max}$		–	±10	µA
I_{CC}	Operating Power Supply Current	f=15MHz (Q, E) f=25MHz (H) $V_{CC} = V_{CC\ Max}$ V_{IL}=0.5V V_{IH}=3.0V	Half Power	–	130	mA
			Quarter Power (only 15 and 20ns)	–	65	
			Eighth Power (only 15ns)	–	40	
I_{OS}*	Output Short Circuit Current	V_{CC}=5.0V, V_B=0.5V		-150	-30	mA
V_{OL}	Output Low Voltage	–		–	0.5	V
V_{OH}	Output High Voltage	–		2.4	–	V

* One output at a time for a maximum duration of one second.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	From	To	20V8AS 10 Max.☆	20V8AS 12 Max.☆	20V8AS 15 Max.	20V8AS 20 Max.	Units	Test Cond.*
t_{pd}	Combinational Propagation Delay	Input	Output	10	12	15	20	ns	1
t_{co}	Clock to Output Delay	Clock	Registered Output	7	10	10	15	ns	1
t_{en}	Product Term Output Enable to Output	Input	Output	10	12	15	20	ns	2
t_{enr}	Output Register Enable to Output	$\overline{OE}$	Registered Output	10	12	15	18	ns	2
t_{dis}	Product Term Output Disable to Output	Input	Output	10	12	15	20	ns	3
t_{disr}	Output Register Disable to Output	$\overline{OE}$	Registered Output	10	12	15	18	ns	3

AC Operating Conditions

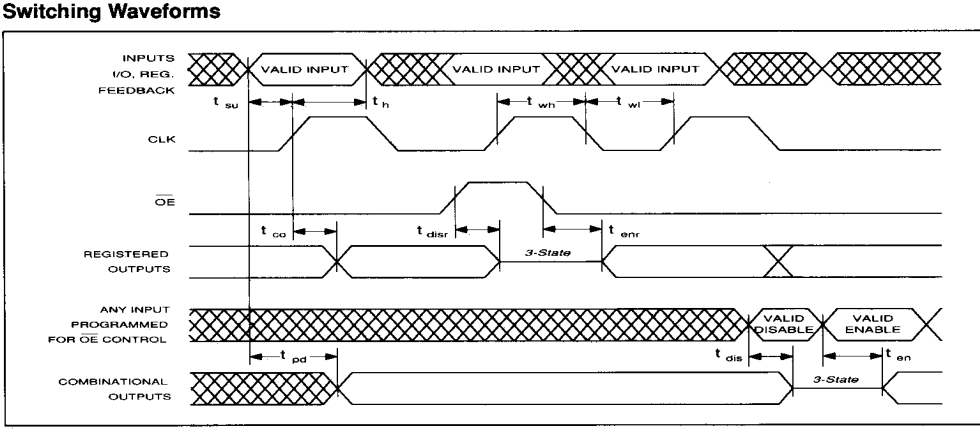
Symbol	Parameter	20V8AS 10☆ Min.	20V8AS 10☆ Max.	20V8AS 12☆ Min.	20V8AS 12☆ Max.	20V8AS 15 Min.	20V8AS 15 Max.	20V8AS 20 Min.	20V8AS 20 Max.	Units	Test Cond.*
t_{su}	Input or Feedback Setup Time (Before Clock Rise)	–	10	–	12	–	12	–	15	ns	–
t_h	Input or Feedback Hold Time (After Clock Rise)	–	0	–	0	–	0	–	0	ns	–
t_{wh}	Minimum Clock Width High	–	8	–	8	–	10	–	12	ns	–
t_{wl}	Minimum Clock Width Low	–	8	–	8	–	10	–	12	ns	–
f_{clk}✧	Clock Frequency Without Feedback	62.5	–	62.5	–	50	–	41.7	–	MHz	1
f_{clkf}✦	Clock Frequency With Feedback	58.8	–	48.5	–	41.6	–	33.3	–	MHz	1

☆ Commercial Temperature range only.

* Refer to "Switching Test Conditions".

✧ $f_{clk} = \frac{1}{t_{wh} + t_{wl}}$ ✦ $f_{clkf} = \frac{1}{t_{su} + t_{co}}$

Switching Waveforms



FUNCTIONAL DESCRIPTION

GAL20V8AS has a programmable AND array whose output terms feed a fixed (non programmable) OR array, as bipolar PAL®. The 2 × 10 input lines enter the AND array as true or complemented form. 64 product terms are available allowing standard Sum of Products Logic implementation. Each product term is obtained by appropriate connections between the input lines and the product term line. The connections can be made by programming the E^2PROM memory cell at each intersection of the AND matrix (2560 memory cells). The 64 product terms are divided into eight groups of 8 terms each. One product term for each group can be used to provide Output Enable control for combinational output, the others are connected with an OR gate into the corresponding OLMC (Output Logic Macrocell). The output buffer is in 3-state when the corresponding output enable signal is low.

OUTPUT LOGIC MACROCELL (OLMC)

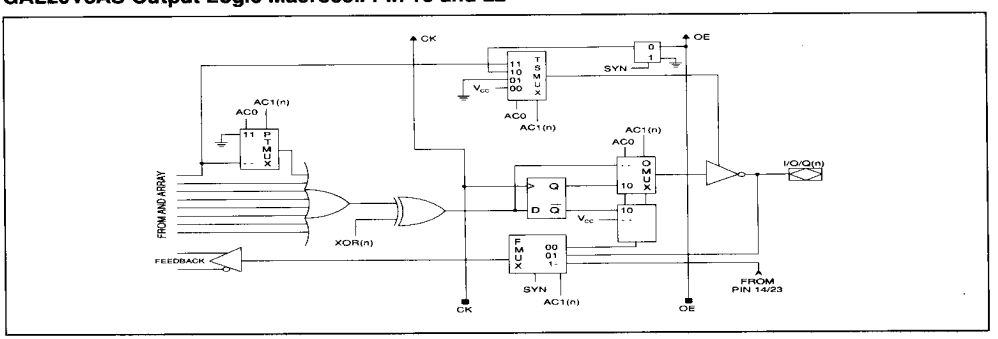
The following discussion pertains to configuring the output logic macrocells. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable is connected to all registered outputs; product terms can be used to provide individual output enable control for combinational outputs. All outputs have always programmable polarity.

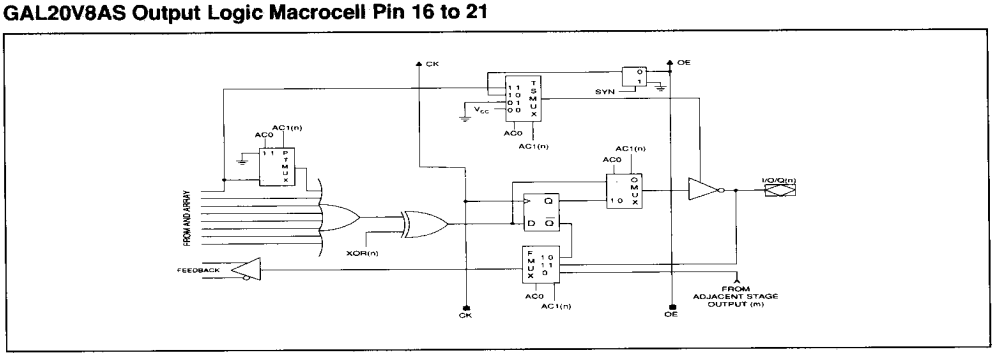
The output logic macrocell provides the designer with maximum output flexibility in matching signal requirements, thus providing more functions than existing 24 pin PAL® devices.

Three different configuration modes of the OLMCs are possible: registered, complex and simple. The output of an OLMC in registered mode can be either registered or combinational. Different modes cannot be mixed: i.e. all OLMCs of a device have to be configured in simple, complex or registered mode.

GAL20V8AS Output Logic Macrocell Pin 15 and 22



GAL20V8AS Output Logic Macrocell Pin 16 to 21

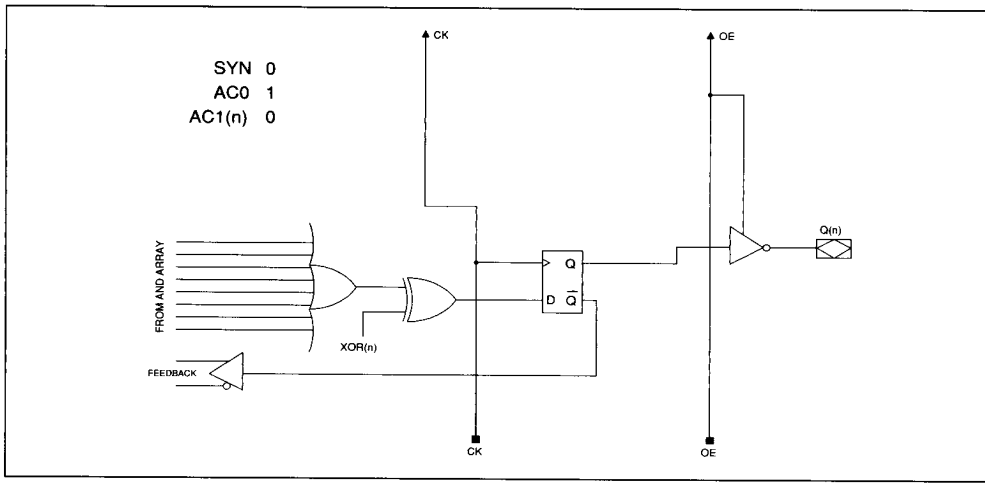


REGISTERED MODE

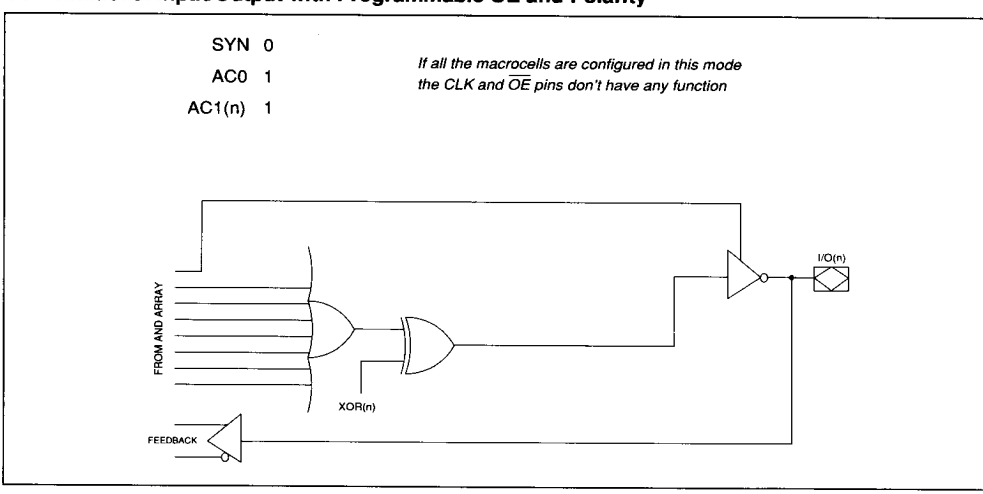
In registered mode macrocells are configured as registered outputs or combinational inputs/outputs. Any macrocell can be configured as registered output or combinational input/output. Up to 8 registered outputs or up to 8 inputs/outputs are possible in this mode.

All registered macrocells share common clock and output enable control. Registered outputs have 8 data product terms per output, while combinational inputs/outputs have only 7 data product terms per output: in the latter case the eighth product term serves as individual output enable control for each macrocell.

Registered Output with Programmable Polarity



Combinational Input/Output with Programmable OE and Polarity



COMPLEX MODE

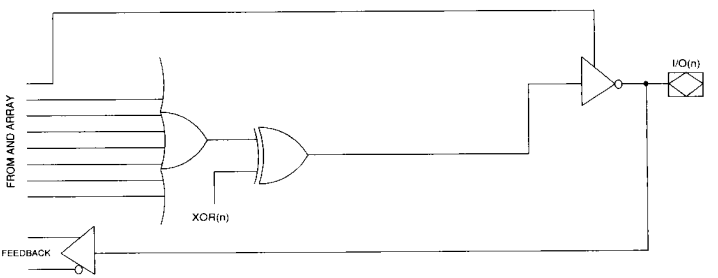
In complex mode macrocells are configured as combinational inputs/outputs or outputs only. The two outermost macrocells (15 and 22) do not have input capability: so only 6 inputs/outputs are possible in this mode. Applications requiring 8 inputs/outputs must be implemented in registered mode.

All macrocells have 7 data product terms per output; the eighth product term is used as individual output enable control for each macrocell. The clock and output enable pins (pins 1 and 13 respectively) are always available as inputs.

Combinational Input/Output with Programmable OE and Polarity

SYN 1
AC0 1
AC1(n) 1

The two outermost macrocells can't perform this function in Complex Mode

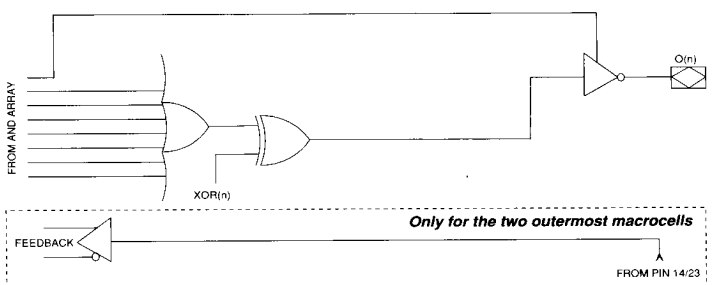


Combinational Output with Programmable OE and Polarity

SYN 1
AC0 1
AC1(n) 1

In Complex Mode the two outermost macrocells are permanently configured in this mode

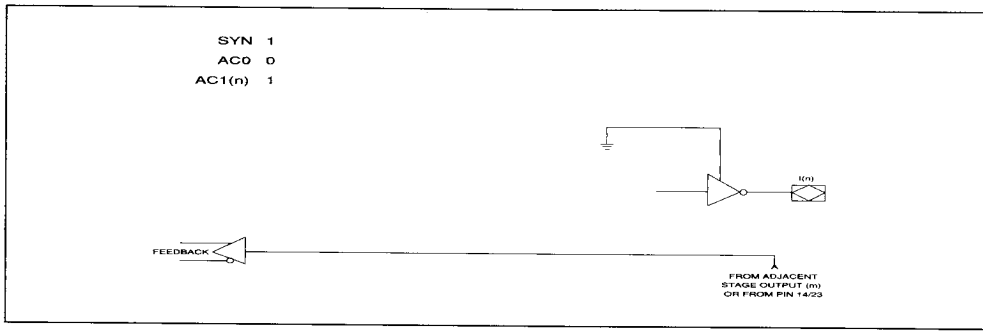
The other six macrocells can emulate this function by not using the feedback into the AND array



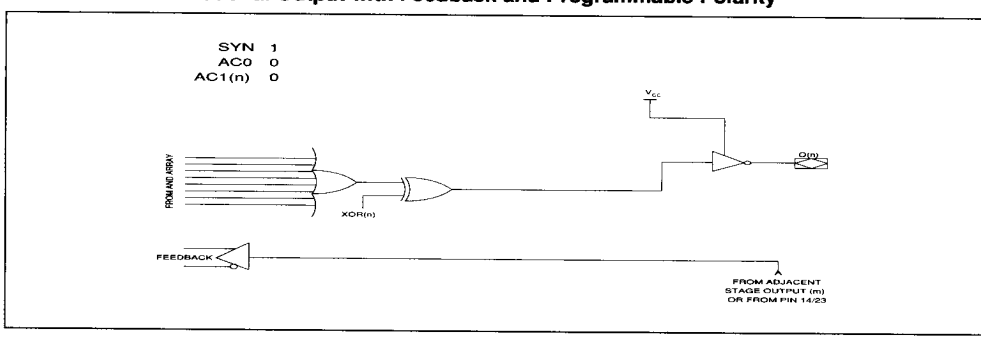
SIMPLE MODE

In simple mode macrocells are configured as dedicated inputs or as dedicated, always active, combinational outputs. Only the two outermost macrocells (15 and 22) can be configured as dedicated inputs. All macrocells have 8 data product terms per output. The clock and output enable pins (pins 1 and 13 respectively) are always available as inputs.

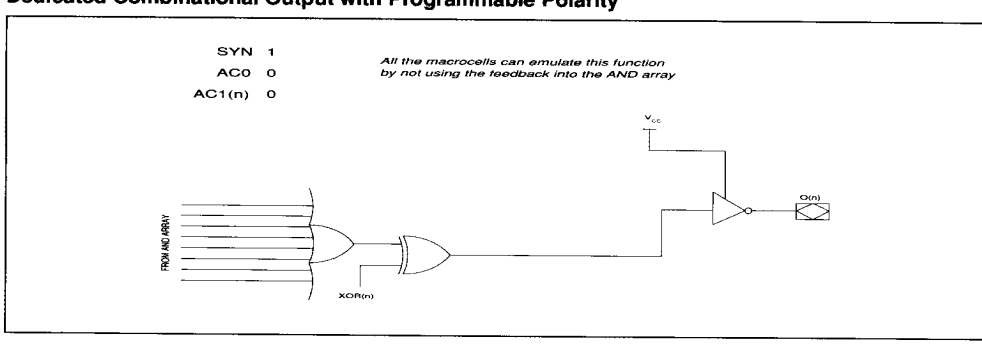
Dedicated Input Mode



Dedicated Combinational Output with Feedback and Programmable Polarity



Dedicated Combinational Output with Programmable Polarity

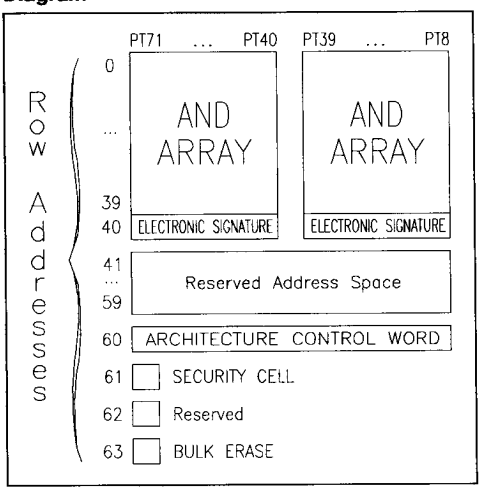


ROW ADDRESS MAP DESCRIPTION

There are a total of 44 unique row addresses available to the user when programming the GAL20V8AS device. Row addresses 0-39 each contain 64 bits of input term data. This is the AND array where the custom logic pattern is programmed. Row 40 is the Electronic Signature Word. It has 64 bits available for any user defined purpose. Row 41-59 are reserved by the manufacturer and are not available to users.

Row 60 contains the architecture and output polarity information. The 82 bits within this word are programmed to configure the device for a specific application. Row 61 contains a one bit security cell that when programmed prevents further pattern verification of the array. Row 63 is the row that is addressed to perform a bulk erase of the device, resetting it back to a virgin state. Each of these functions is described in the following sections.

GAL20V8AS Row Addresses Map Block Diagram



ELECTRONIC SIGNATURE WORD DESCRIPTION

An electronic signature word is provided with every GAL20V8AS device. It resides at row address 40 and contains 64 bits of reprogrammable memory that can contain user-defined data. Some uses include user ID codes, revision numbers, or inventory control. This signature data is always available to the user independent of the state of the security cell.

ARCHITECTURE CONTROL WORD

All the various output configurations of the GAL20V8AS devices are controlled by programming cells within the 82 bit Architecture Control Word that resides at row 60. The location of specific bits within the Architecture Control Word is shown in the control word diagram in figure below. The function of the SYN, AC0 and AC1(n) bits have been explained in the OUTPUT LOGIC MACROCELL description. The eight polarity bits determine each output's polarity individually. The numbers below the XOR(n) and AC1(n) bits in the architecture control word diagram shows the output device pin number that the polarity bits control.

SECURITY CELL

Row address 61 contains the Security Cell (one bit). The Security Cell is provided on all GAL20V8AS devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further verification of the array (rows 0-39). The cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

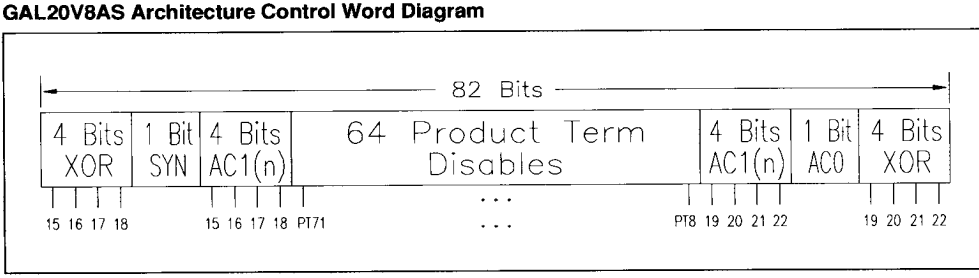
BULK ERASE MODE

By addressing row 63 during a programming cycle, a clear function performs a bulk erase of the array and the Architecture Control Word. In addition, the Electronic Signature Word and the Security Cell are erased. This mode resets a previously configured device back to its virgin state.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the

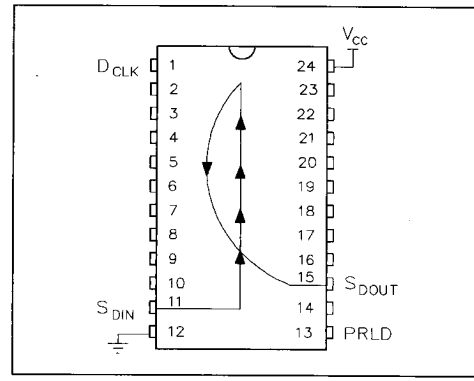
GAL20V8AS Architecture Control Word Diagram



design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper management of these conditions, a method must be provided to break the feedback paths, and force any desired (e.g. illegal) state into a register. Then the machine can be sequenced and the outputs tested for the correct next state condition. The GAL20V8AS device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors can perform output register preload automatically.

The figure on the right shows the pin functions necessary to preload the register. This test mode is entered by raising PRLD to V_{IES} (register preload input voltage, typically 15V), which enables the serial data in (S_{DIN}) buffer and the serial data out (S_{DOUT}) buffer. Data is then serially shifted into the registers on each rising edge of the clock, D_{CLK}. Only the macrocells with registered output configurations are loaded. If only 3 outputs have registers, then only 3 bits need be shifted in. The registers are loaded from the bottom up as shown in the figure on the right.

Output Register Preload Pinout



LATCH-UP PROTECTION

GAL® devices are designed with an on board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

POWER-UP RESET

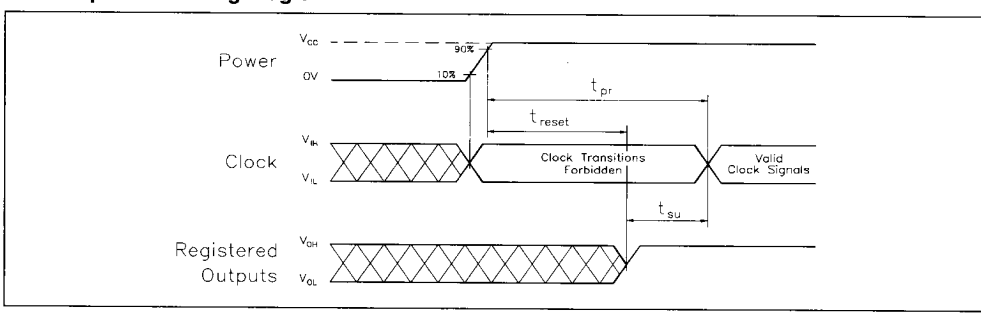
Circuitry within the GAL20V8AS provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{reset}=10µs). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This features can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, the V_{CC} rise must be monotonic to guarantee a valid power-up reset of the GAL20V8AS. The registers will reset within a maximum of t_{reset} time: before this time any clock transition from low to high is forbidden to avoid undesired commutations. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met (i.e. avoid clocking before the t_{pr}=t_{reset}+t_{su} time interval).

DEVICES PROGRAMMING

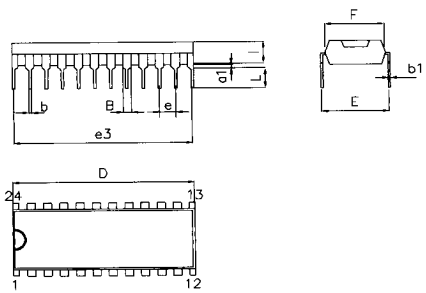
SGS-THOMSON strongly recommends the use of qualified programming hardware. Programming on unapproved equipment will invalidate all guarantees.

Power-Up Reset Timing Diagram



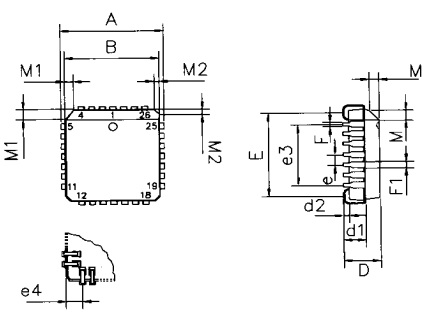
PACKAGE MECHANICAL DATA

PDIP 24 Pins



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
a1	0.38			0.015		
B	1.27		1.65	0.050		0.065
b		0.46			0.018	
b1		0.25			0.010	
D			31.88			1.255
E		7.62			0.300	
e		2.54			0.100	
e3		27.94			1.100	
F			6.86			0.27
I			4.32			0.170
L		3.30			0.130	

PLCC 28 Pins



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.20		4.57	0.165		0.180
d1	2.29		3.04	0.090		0.120
d2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
e4			1.99			0.078
F		0.46			0.018	
F1		0.71			0.028	
M		1.24			0.049	
M1		1.143			0.045	
M2			0.51			0.020

Seating Plane: 0.101 mm/0.004 inches

Ordering Informations*

SGS-THOMSON GAL®s are available in a variety of package and temperature ranges.
General ordering code is reported below.

GAL20V8AS - s w p t j

PLCC Pinout	**J**	Jedec Pinout
Temperature	**1**	0°C to +70°C
	3	-40°C to+85°C (only for 15 and 20ns Speed selection)
Package	**B**	24 Pins PDIP
	C	28 Pins PLCC
Power	**H**	Half Power
	Q	Quarter Power (only for 15 and 20ns Speed selection)
	E	Eighth Power (only for 15ns Speed selection)
Speed	**10**	10ns
	12	12ns
	15	15ns
	20	20ns

Example: ordering code for a GAL20V8AS, 12ns speed and Half Power in PLCC (Jedec pinout) is **GAL20V8AS-12HC1J**

* Please contact local Product Marketing for latest update on package / temperature range availability.