Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (64K x 1-BIT)

IDT7187S
IDT7187L

T-46-23-05

FEATURES:

- High speed (equal access and cycle time)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin plastic and ceramic DIP, 24-pin plastic SOIC, 22-pin and 28-pin leadless chip carrier and 24-pin CERPACK
- Produced with advanced CMOS high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

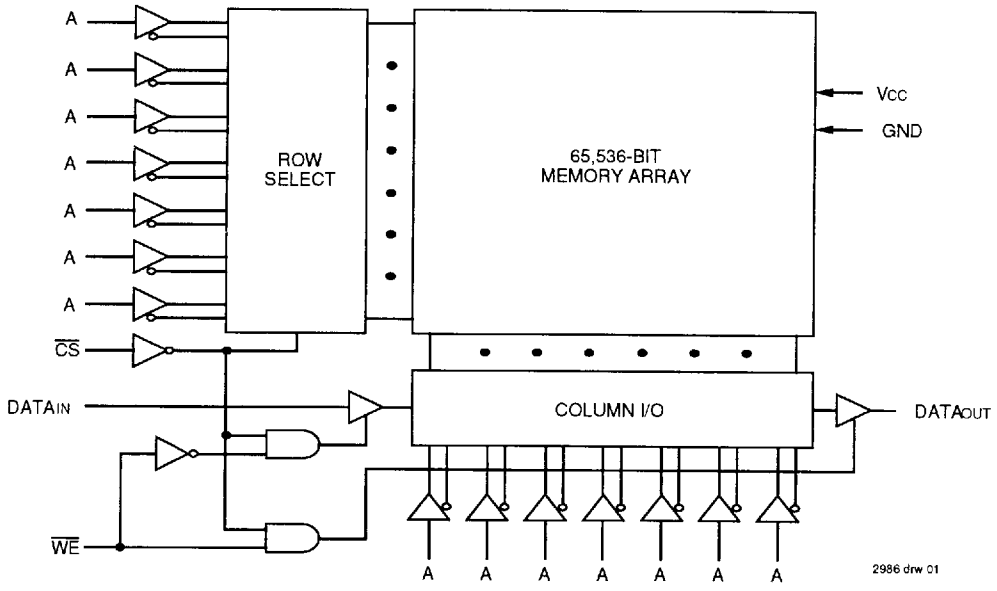
The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability CMOS technology. Access times as fast as 15ns are available.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—I_{SB} and I_{SB1}. I_{SB} provides low-power operation; I_{SB1} provides ultra-low-power operation. The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30μW.

Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil plastic or ceramic DIP, 24-pin plastic SOIC (Gull-Wing and J-Bend), 22- and 28-pin leadless chip carriers, or 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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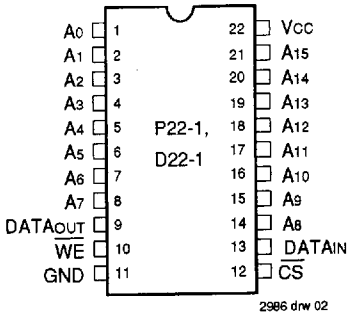
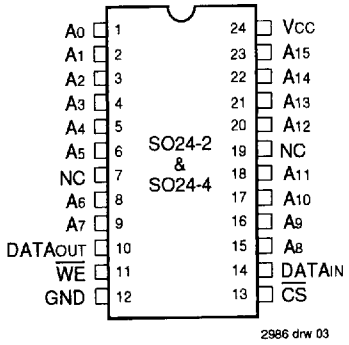
The IDT logo is a registered trademark of Integrated Device Technology, Inc.

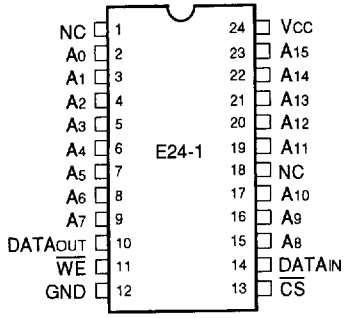
PIN CONFIGURATIONS



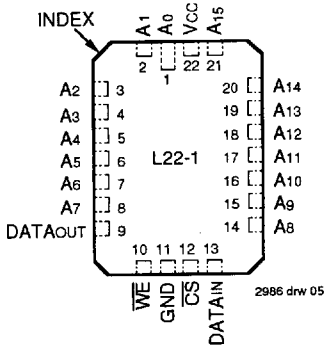
DIP
TOP VIEW



SOIC/SOJ
TOP VIEW



CERPACK
TOP VIEW

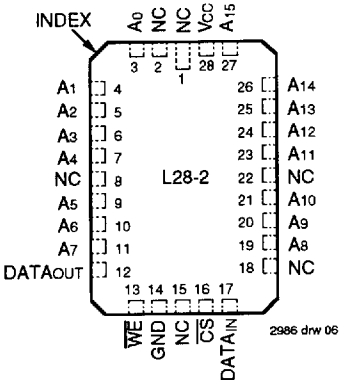


22-PIN LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A15	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
VCC	Power
DATAIN	Data Input
DATAOUT	Data Output
GND	Ground

2986 tbl 01



28-PIN LCC
TOP VIEW

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DOUT	Active
Write	L	L	High-Z	Active

2986 tbl 02

NOTES:
1. H = VIH, L = VIL, X = don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2986 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2986 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2986 tbl 05

1. VIL (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2986 tbl 06

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DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT7187S Min.	IDT7187S Max.	IDT7187L Min.	IDT7187L Max.	Unit
|ILI|	Input Leakage Current	VCC = Max., VIN = GND to VCC	MIL. COM'L.	— —	10 5	— —	5 2	µA
|ILO|	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	MIL. COM'L.	— —	10 5	— —	5 2	µA
VOL	Output Low Voltage	IOL = 10mA, VCC = Min.			0.5	—	0.5	V
		IOL = 8mA, VCC = Min.		—	0.4	—	0.4	
VOH	Output High Voltage	IOL = –4mA, VCC = Min.		2.4	—	2.4	—	V

2986 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7187S15(3)		7187S20 7187L20		7187S25 7187L25		7187S35 7187L35		7187S45 7187L45		7187S55/70 7187L55/70		7187S85 7187L85		Unit
			Com'l.	Mil.	Com'l.	Mil.(3)	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	100	—	90	105	90	105	90	105	—	105	—	105	—	105	mA
		L	—	—	70	85	70	85	70	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	140	—	130	140	120	130	110	120	—	120	—	120	—	120	mA
		L	—	—	110	120	100	110	90	100	—	95	—	90	—	90	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	60	—	55	65	50	55	45	50	—	50	—	50	—	50	mA
		L	—	—	40	60	35	50	30	40	—	35	—	30/28	—	28	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	20	—	15	20	15	20	15	20	—	20	—	20	—	20	mA
		L	—	—	0.3	1.5	0.3	1.5	0.3	1.5	—	1.5	—	1.5	—	1.5	

2986 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}, f = 0 means no input lines change.
3. These specs are preliminary.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

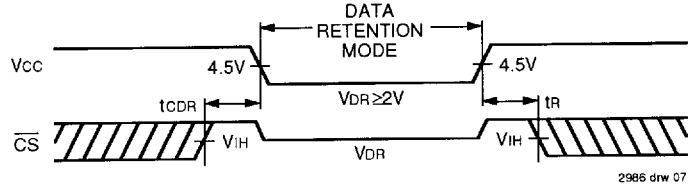
(L Version Only) V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0v	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

2986 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2986 drw 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2986 tbl 10

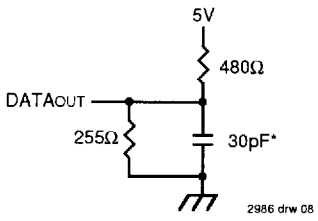


Figure 1. AC Test Load

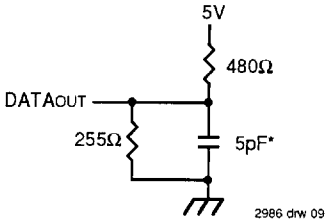


Figure 2. AC Test Load (for tHZ, tLZ, twz and tow)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

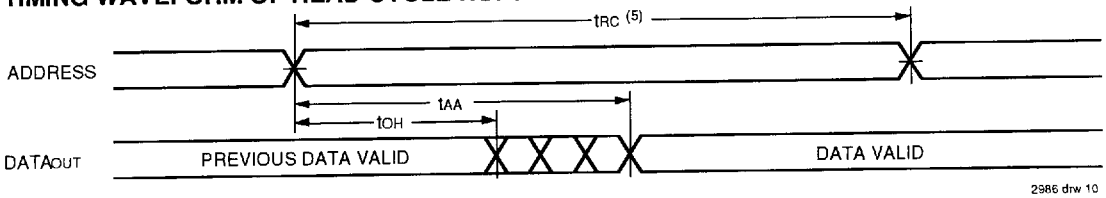
Symbol	Parameter	7187S15(1)/20 7187L20		7187S25 7187L25		7187S35/45(2) 7187L35/45(2)		7187S55(2) 7187L55(2)		7187S70(2) 7187L70(2)		7187S85(2) 7187L85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
tAA	Address Access Time	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tACS	Chip Select Access Time	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tLZ	Output Selection to Output in Low-Z(3)	5	—	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Chip Deselect to Output in High-Z(3)	—	6	—	12	—	17/20	—	30	—	30	—	40	ns
tPU	Chip Select to Power-Up Time(3)	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power-Down Time(3)	—	15/20	—	20	—	30/35	—	35	—	35	—	40	ns

2986 tbl 11

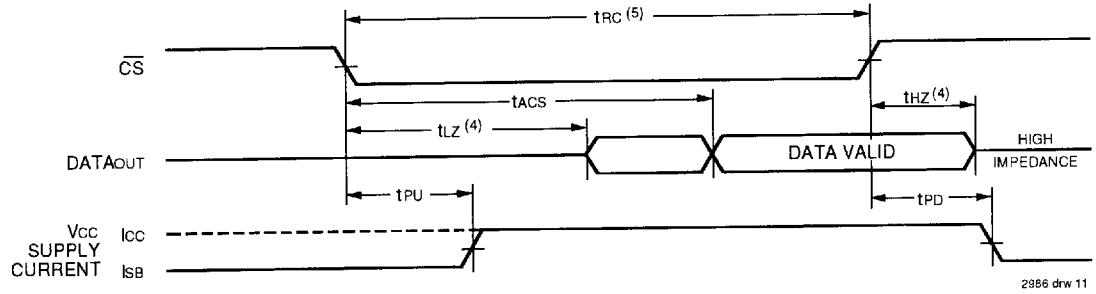
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

6

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)



NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. $\overline{CS}$ is LOW for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

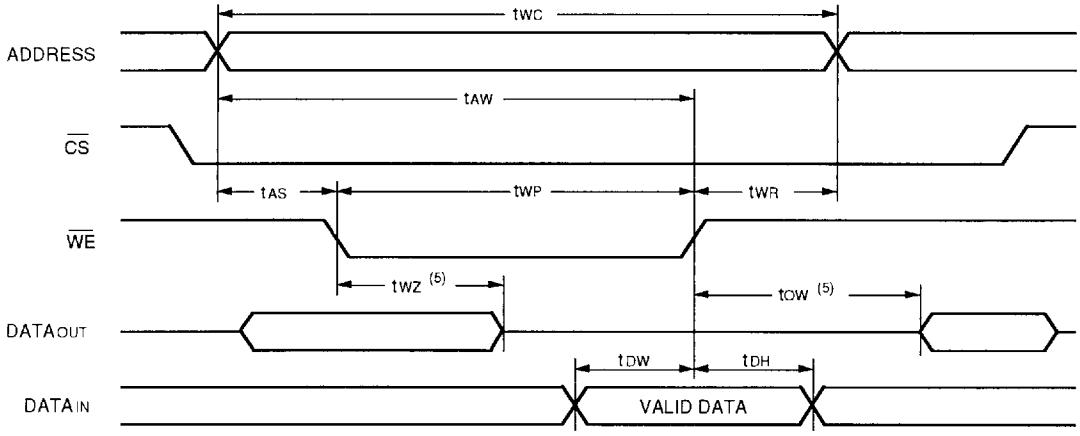
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7187S15[1]/20 7187L20		7187S25 7187L25		7187S35/45[2] 7187L35/45[2]		7187S55[2] 7187L55[2]		7187S70[2] 7187L70[2]		7187S85[2] 7187L85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	12/15	—	25	—	35/45	—	55	—	70	—	85	—	ns
tCW	Chip Select to End-of-Write	12/15	—	20	—	25/40	—	50	—	55	—	65	—	ns
tAW	Address Valid to End-of-Write	12/15	—	20	—	25/40	—	50	—	55	—	65	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12/15	—	20	—	20/25	—	35	—	40	—	45	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	8/10	—	15	—	15/25	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	5	—	5	—	5	—	5	—	5	—	ns
tWZ	Write Enable to Output in High-Z[3]	—	6/8	—	12	—	15/30	—	30	—	30	—	40	ns
tOW	Output Active from End-of-Write[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
2986 tbl 12

1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1,2,3,4]

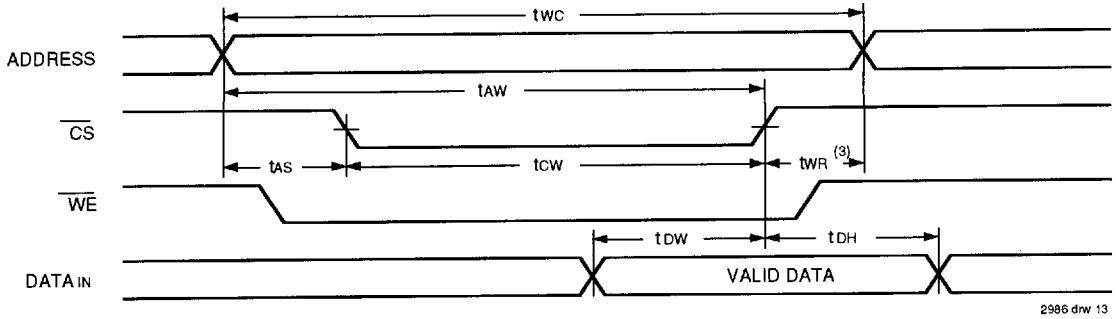


2986 drw 12

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION