Integrated Device Technology, Inc.

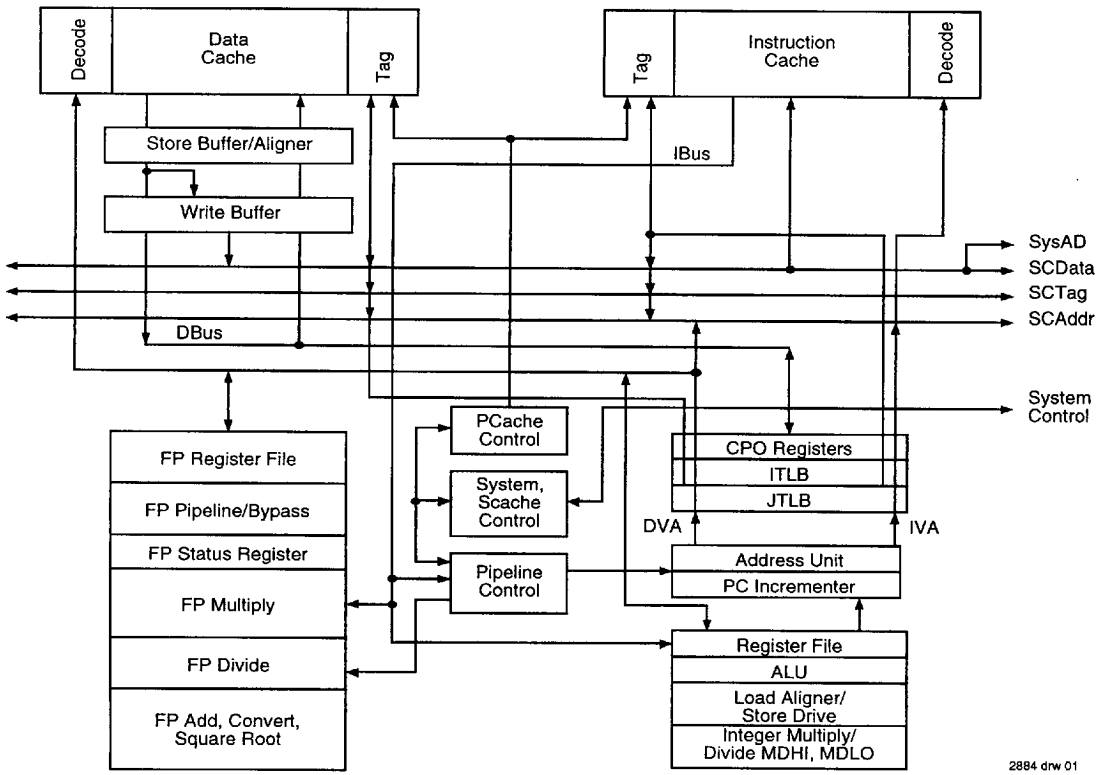
THIRD GENERATION 64-BIT SUPER-PIPELINED RISC MICROPROCESSOR

IDT79R4400™
IDT79RV4400

FEATURES:

- True 64-bit microprocessor
  - — 64-bit integer operations
  - — 64-bit floating-point operations
  - — 64-bit registers
  - — 64-bit virtual address space
- High-performance microprocessor
  - — Super-pipelined architecture supports 200MIPS at 100MHz
  - — No issue restrictions for dual instruction issue
- High level of integration
  - — 64-bit integer CPU
  - — 64-bit floating-point accelerator
  - — 16KB instruction; 16KB data cache
  - — Flexible MMU with large TLB
- Standard operating system support includes:
  - — Microsoft Windows™ NT
  - — UNISOFT UNIX™ System V.4
- Fully software compatible with R3000A 32-bit RISC Processor Family
- 50, 67, 75, 88 and 100MHz clock frequencies
- 64GB physical address space
- Processor family for a wide variety of applications
  - — Desktop workstations
  - — Deskside or departmental servers
  - — High-performance embedded applications
  - — Tightly coupled multi-processing systems
  - — Fault tolerant systems
- R4400 for 5V operation and RV4400 for 3.3V operation

BLOCK DIAGRAM



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DESCRIPTION:

The IDT79R4400 family supports a wide variety of processor-based applications, from 32-bit ARC compliant desktop systems through high-performance, 64-bit OLTP systems manipulating large data bases in a multi-processor-based system. The IDT79R4400 products offer a broad range of price-performance options for high-performance systems, allowing the system architect unprecedented degrees of freedom in making price-performance tradeoffs.

The IDT R4400 products provide complete upward application-software compatibility with the IDT79R3000 family of microprocessors, including the IDT79R3000A and the IDT RISController™ family (IDT79R3051™ family). Microsoft Windows NT and UNISOFT UNIX V.4 operating systems insure the availability of thousands of applications programs, geared to provide a complete solution to a large number of processing needs. An array of development tools facilitates the rapid development of R4400-based systems, enabling a wide variety of customers to take advantage of the MIPS Open Architecture philosophy.

The R4400 family achieves a unique balance between high-integer and high-floating-point performance. The key to this balance is the super-pipelined architecture of the processor, which brings performance gains to both integer and floating-point intensive programs without requiring recompilation to take advantage of the architectural advancement. The execution engine is assured of a rapid and continual supply of instructions and data through the use of large on-chip caches, and a high-performance on-chip TLB.

The R4400 family also provides a compatible, timely, and necessary evolution path from 32-bit to true, 64-bit computing. The original design objectives of the R4400 clearly mandated this evolution path; the result is a true 64-bit processor fully compatible with 32-bit operating systems and applications.

The 64-bit computing and addressing capability of the R4400 enables a wide variety of capabilities previously limited by a smaller address space. For example, the large address space allows operating systems with extensive file mapping; direct access to large files can occur without explicit I/O calls. Applications such as large CAD databases, multi-media, and high-quality image storage and retrieval all directly benefit from the enlarged address space.

This data sheet provides an overview of the features and architecture of the IDT79R4400 CPU family. A more detailed description of the processor is available in the *"R4400 Hardware User's Manual"*. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

IDT79R4400 FAMILY MEMBERS

The IDT79R4400 processor is available in three different configurations: the IDT79R4400MC and IDT79R4400SC, which include a 128-bit wide secondary cache bus; and the IDT79R4400PC, with no secondary cache interface. All references to R4400 apply to R4400 (5V) and RV4400 (3.3V) operation.

PC CONFIGURATION

The IDT79R4400PC is available in a 179-pin Pin Grid Array (PGA). This configuration does not support secondary cache or cache coherency, and is ideal for applications such as high-performance embedded control and low-cost desktop systems, where the on-chip caches provide enough performance and where cost, power, and board space must be kept to a minimum. By eliminating a secondary cache, a system can be designed with fewer parts and lower power consumption.

SC CONFIGURATION

The 79R4400SC is available in a 447-pin Pin Grid Array (PGA). This processor supports a secondary cache interface and is ideal in systems where high performance is desired. This component supports a 128kB to 4mB secondary cache made from standard SRAMs. This flexibility allows system designers to make price/performance tradeoffs in cache subsystem designs.

MC CONFIGURATION

The IDT79R4400MC is also available in the 447-pin Pin Grid Array (PGA). This processor supports a secondary cache and configurable multiprocessor cache coherency protocols. Like the "SC" configuration, this processor also supports a 128kB to 4mB secondary cache made from standard SRAMs. The IDT79R4400MC is well suited for a range of designs from high performance desktop systems to fault tolerant multiprocessor servers.

5

HARDWARE OVERVIEW

The IDT R4400 processor brings a high-level of integration designed for high-performance computing. The key elements of the IDT R4400 are briefly described below. A more detailed description of each of these subsystems is available in other literature.

Superpipelined Implementation

In order to achieve the high-performance desired for today's applications and user's interfaces, the R4400 exploits instruction level parallelism using a superpipelined microarchitecture.

The R4400 uses an 8-stage superpipeline which places no issue restrictions on instruction issue. Thus, any two instructions can be issued each master clock cycle under normal circumstances, leading to 200MIPS performance at 100MHz. One key advantage of this architecture is that all existing applications can gain from the architectural advancement represented by the R4400, without requiring recompilation to reorder the software.

In order to support dual instruction issue, the internal pipeline of the R4400 operates at twice the external clock frequency. Instruction execution stages such as cache accesses are pipelined (thus the chip itself is super-pipelined) to eliminate bottlenecks associated with long-latency functional units. Other stages, such as the ALU stage, completely process one operation per pipeline clock cycle, allowing the results of one operation to be immediately used by the instruction which follows, with no pipeline interlocks.

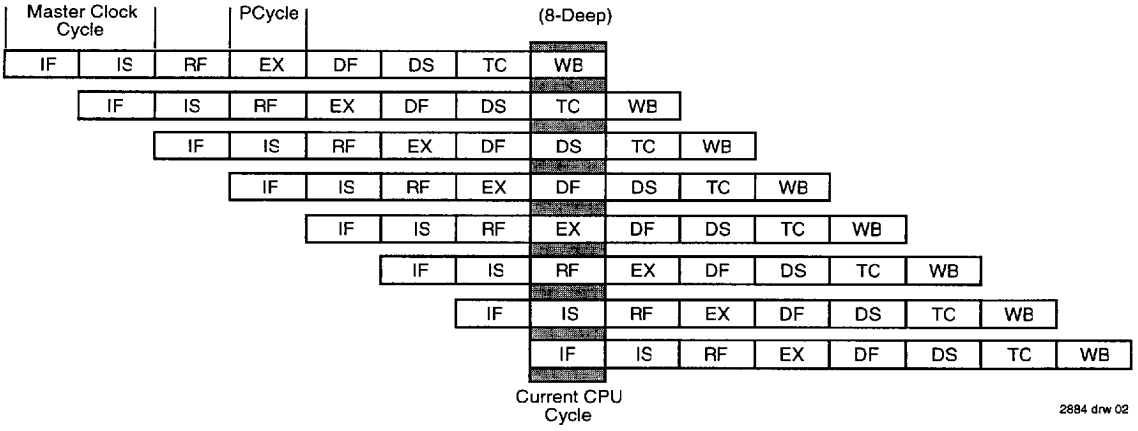
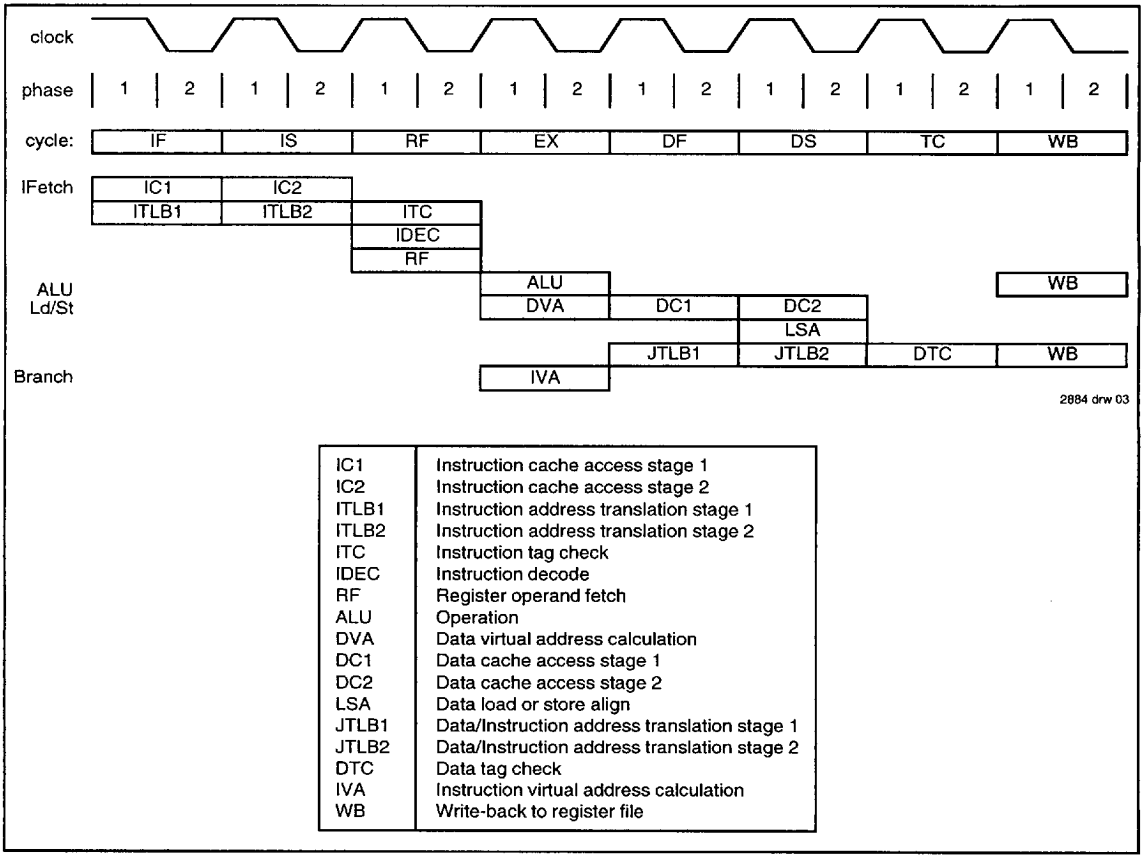


Figure 1. R4400 8-Stage Super-Pipeline



IC1	Instruction cache access stage 1
IC2	Instruction cache access stage 2
ITLB1	Instruction address translation stage 1
ITLB2	Instruction address translation stage 2
ITC	Instruction tag check
IDEC	Instruction decode
RF	Register operand fetch
ALU	Operation
DVA	Data virtual address calculation
DC1	Data cache access stage 1
DC2	Data cache access stage 2
LSA	Data load or store align
JTLB1	Data/Instruction address translation stage 1
JTLB2	Data/Instruction address translation stage 2
DTC	Data tag check
IVA	Instruction virtual address calculation
WB	Write-back to register file

Figure 2. Pipeline Activities

High clock frequency results from careful construction of the various resources of the processor: pipelining cache accesses, shortening register access times, implementing virtually indexed primary caches, and allowing the latency of functional units to span multiple pipeline stages.

After extensive simulation of many methods of exploiting instruction level parallelism, superpipelining was chosen because it improves integer performance commensurate with floating-point performance. Thus, the R4400 provides performance benefits both to technical computing applications, and also to a wide variety of commercial applications as well. In today's technology, superpipelining results in less complex logic, faster cycle times, quicker design cycles, and lower cost. The pipeline of the IDT79R4400 is illustrated in Figure 1.

THE R4400 PIPELINE

The R4400 processor has an eight-stage execution pipeline. That is, each instruction takes eight Pclock (Pipeline clocks, at twice the frequency of the input clock) cycles to execute, but a new instruction is started on each Pclock cycle. Another way of viewing the process is that, at any point in time, eight separate instructions are being executed at once. Figure 1 shows the R4400 pipeline in both views: a horizontal slice shows the execution process of individual instructions, and a vertical slice shows the processing of eight instructions at once.

Each box shown in Figure 1 corresponds to a part of the execution process.

Figure 2 illustrates the activities occuring within each pipestage as a function of the instruction type. First, in the IF stage, an instruction address is selected by the program counter logic and the first half of both the instruction cache fetch (IC1) and the instruction virtual to physical address translation (ITLB1) is performed. The instruction address translation is done through a two entry subset of the main or *joint* translation lookaside buffer (JTLB) called the ITLB. In the IS stage, the second half of both the instruction cache fetch (IC2) and instruction translation (ITLB2) are done.

During the RF stage, three activities occur in parallel. The instruction decoder (IDEC) decodes the instruction and checks for interlock conditions. Meanwhile, the instruction tag check (ITC) is performed between the instruction cache tag and the page frame number (PFN) from the ITLB's translation. In parallel with both of the above, the operands are fetched from the register file (RF).

In the EX stage, if the instruction is a register-to-register operation, the arithmetic or logical operation is performed (ALU). If the instruction is a load/store, a data virtual address is calculated (DVA). If the instruction is a branch, a virtual branch target address is calculated (IVA).

For load/stores, the DF stage is used to do the first half of both the data cache fetch (DC1) and the data virtual to physical address translation (JTLB1). Similarly, the DS stage does the second half of both the data fetch (DC2) and the data translation (JTLB2) as well as the load align or store align (LSA), as appropriate. If the instruction is a branch, the JTLB is used during DF and DS to translate the branch address and refill the ITLB if necessary.

The TC stage is used to perform the tag check for load/stores. During the WB stage the instruction result is written to the register file.

Smooth pipeline flow is interrupted when cache accesses miss, data dependencies are detected, or when exceptions occur. Interruptions that are handled by hardware, such as cache misses, are referred to as *interlocks,* while those that are handled using software are *exceptions.* Collectively, the cases of all interlock and exception conditions are referred to as *faults.*

Interlocks come in two varieties. Those interlocks which are resolved by simply stopping the pipeline are referred to as *stalls,* while those which require part of the pipeline to advance while holding up another part are *slips.*

At each cycle, exception and interlock conditions are checked for all active instructions. The conditions can be referred back to particular instructions, as each exception or interlock condition corresponds to a particular pipeline stage.

When an exception condition occurs, the relevant instruction and all that follow it in the pipeline are cancelled. Accordingly, any stall conditions and any later exception conditions that are referenced to the same instruction are inhibited; there is no value in servicing stalls for a cancelled instruction. A new

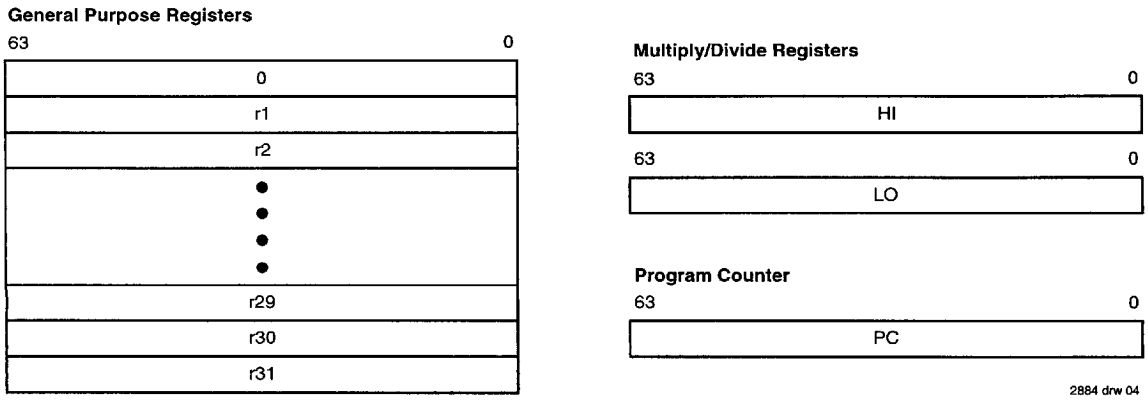


Figure 3. CPU Registers

instruction stream is begun, starting execution at a predefined exception vector. System control coprocessor registers are loaded with information that will identify the type of exception and any necessary auxiliary information, such as the virtual address at which translation exceptions occur.

When a stall condition is detected, all eight instructions, each in a different stage of the pipeline, are frozen at once. Often, the stall condition is only detected after parts of the pipeline have advanced using incorrect data; this occurrence is referred to as *pipeline overrun.* When in the stalled state, parts of the pipeline that are immune to overrun are frozen and the remainder is permitted to continue clocking. Just before resuming execution, the pipeline overrun is reversed by inserting corrected information into the pipeline.

When a slip condition is detected, the pipeline stages which must advance in order to resolve the dependency continue to be retired while the dependent stages are held until the necessary data is available.

Another class of interlocks exists which, since they originate external to the processor, are not referenced to a particular pipeline stage. These interlocks are referred to as *external* stalls and are unaffected by the occurrence of exceptions.

Integer Execution Engine

The R4400 implements the extended MIPS Instruction Set architecture, and thus is fully upwards compatible with applications running on the earlier generation parts. The R4400 includes additions to the instruction set, targeted at improving performance and capability while maintaining binary compatibility with earlier processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, as well as faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability amongst implementations of the MIPS instruction set architecture.

In addition to the instruction extensions detailed above, new instructions have been defined to take advantage of the 64-bit architecture of the processor. When operating as a 32-bit processor, the R4400 will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The programmer model for the R4400 includes the register set illustrated in Figure 3. The register resources include: 32 general purpose orthogonal integer registers, the HI/LO result registers for the intger multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

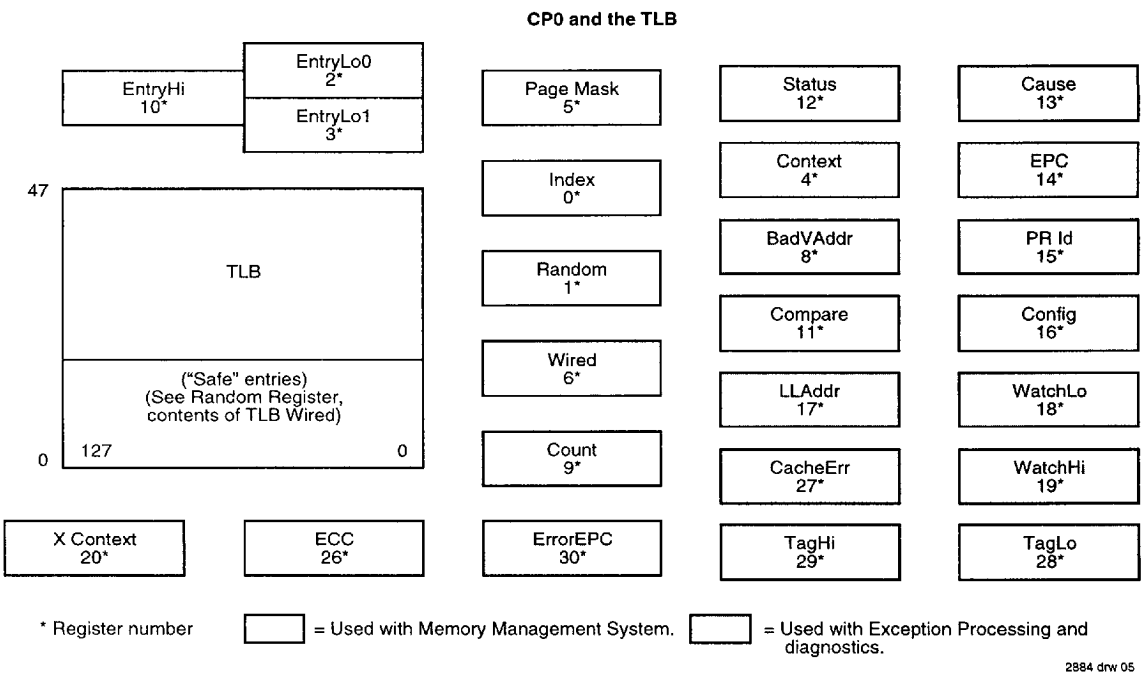


Figure 4. The R4400 CP0 Registers

System Control Co-processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual memory subsystem, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent. The R4400 CP0 is a superset extension of the MMU found in the R3000A.

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction translation buffer (the ITLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

System Control Co-Processor Registers

The R4400 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined, changed (the operating modes, kernel vs. user mode, interrupts enabled or disabled, cache features) and controlled. Also, these registers control exception handling. In addition, the R4400 includes registers to implement a real-time cycle counting facility, to address reference traps for debugging, to aid in cache diagnostic testing, and to assist in data error detection and correction.

Figure 4 illustrates the System Control Co-Processor registers.

Virtual to Physical Address Mapping

The R4400 provides three modes of virtual addressing:

- user mode
- kernel mode
- supervisor mode

This mechanism is available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used. In the user mode, the R4400 provides a single, uniform virtual address space of 2GB.

When operating in the kernel mode, four distinct virtual address spaces, totalling 4GB, are simultaneously available and are differentiated by the high-order bits of the virtual address.

The R4400 processor also support a supervisor mode in which the virtual address space is 2.5GB, divided into two regions based on the high-order bits of the virtual address. The three different modes of virtual addressing are shown in Figure 5. When the R4400 is configured as a 64-bit microprocessor, the virtual address space layout is a compatible extension of the 32-bit virtual address space layout.

Joint TLB

For fast virtual-to-physical address decoding, the R4400 uses a large, fully associative TLB which maps 96 virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64gB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space, and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when a new entry is written. Thus, operating systems can treat various regions of memory distinctly from applications programs and data files. For example, a typical frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement algorithm when a TLB miss occurs. The R4400 uses a Random Replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB, and thus avoid being randomly replaced. This facilitates the design of real-time systems, by allowing deterministic access to critical software.

The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is: uncached, noncoherent, sharable, exclusive, or update. The use of these attributes, coupled with state information in the processor caches, enables a wide variety of multiprocessing strategies to be easily implemented.

Figure 6 shows the format of the TLB entry and registers used to control the TLB.

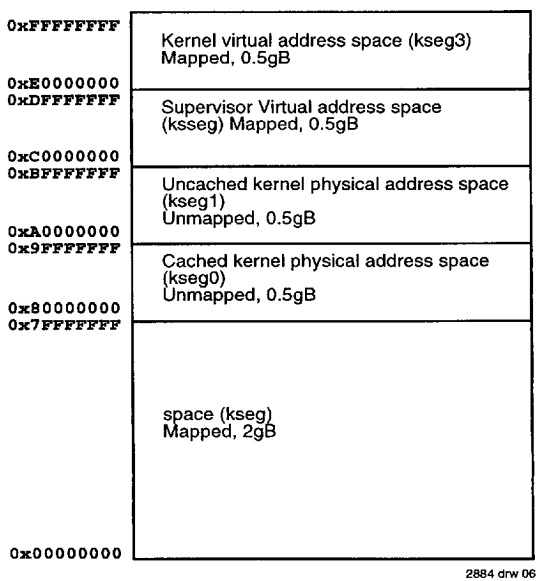


Figure 5. Kernel Mode Virtual Addressing (32-bit mode)

Instruction TLB

The R4400 also incorporates a 2-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation, the ITLB is filled from the JTLB. The operation of the ITLB is invisible to the user.

Register File

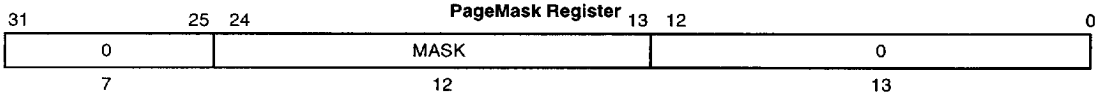
The R4400 has thirty-two general purpose registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and uses bypassing to enable the reading and writing of the same register twice per cycle as well as to minimize the operation latency in the pipeline.

ALU

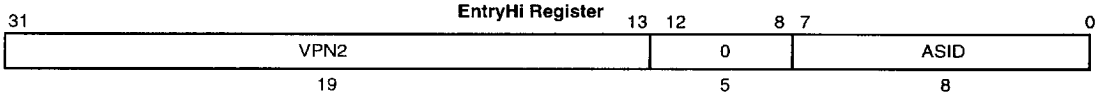
The R4400 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all shift operations. Each of these units is highly optimized and can perform an operation in a single superpipeline cycle.

Integer Multiplier/Divider

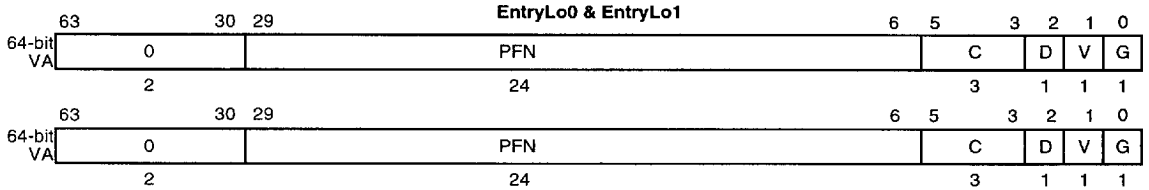
The R4400 integer multplier and divider units perform signed and unsigned multiply and divide operations and execute instructions in parallel with the ALU. The results of the operation are placed in the *MDHI* and *MDLO* registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions. The following table shows the number of processor internal cycles required between a 32-bit integer multiply or divide and a subsequent MFHI or MFLO operation, in order that no interlock or stall



MASK = Page comparison mask
0 = Reserved. Must be written as zero; returns zero when read.



VPN2 = Virtual Page Number divided by two (maps to two pages)
ASID = Address Space ID field. An 8-bit field which lets multiple processes share the TLB while each process has a distinct mapping of otherwise identical virtual page numbers. This is the same ASID described at the beginning of this chapter.
0 = Reserved. Must be written as zero; returns zero when read.



PFN = Page Frame Number. Upper bits of the physical address.
C = Specifies the cache algorithm to be used.
D = Dirty. If this bit is set, the page is marked as dirty and, therefore, writable. This bit is actually a write-protect bit that software can use to prevent alteration of data.
V = Valid. If this bit is set, it indicates that the TLB entry is valid; otherwise, a TLBL or TLBS Miss occurs.
G = Global. If this bit is set in both Lo0 and Lo1, then ignore the ASID.
0 = Reserved. Must be written as zero; returns zero when read.

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Figure 6. Fields of an R4400 TLB Entry

occurs.

Operation	Single Word	Double Word
MULT	10	20
DIV	69	133

FLOATING-POINT UNIT

The R4400 incorporates an entire floating-point unit on chip, including a floating-point register file and execution unit. The floating-point unit forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

Floating-point Co-Processor

The R4400 floating-point execution unit supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into separate multiply, divide, and add/convert/square root units, which allow for overlapped operations. The multiplier is pipelined, allowing a new multiply to begin every 4 cycles.

As in the IDT79R3010, the R4400 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. Thes operations comply with the IEEE Standard 754.

The following table gives the latencies of some of the floating-point instructions in internal processor cycles.

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	7	8
DIV	23	36
SQRT	54	112
CMP	3	3
FIX	4	4
ROUND	4	4
TRUNC	4	4
FLOAT	5	5
ABS	2	2
MOV	1	1
NEG	2	2
LWC1,LDC1	3	3
SWC1,SDC1	1	1

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Floating-Point General Register File

The floating-point register file is made up of sixteen 64-bit registers which can also be viewed as thirty-two 32-bit floating-point registers. The MIPS architecture supports a coprocessor load and store double so, when configured as 64-bit registers, the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store a doubleword instruction in every cycle.

Floating-Point Control Register File

The floating-point control registers contain a register for determining configuration and revision information for the coprocessor and control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

CACHE MEMORY

In order to keep the high-performance superpipeline full and operating efficiently, the R4400 incorporates on-chip instruction and data caches. Each cache has its own 64-bit data path that can be accessed twice a cycle, so the instruction and data caches can be accessed in parallel with full pipelining. Combining this feature with a pipelined, single master clock cycle access of each cache, the cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 2GB per second at a system clock frequency of 75MHz.

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Instruction Cache

The IDT79R4400 incorporates a direct-mapped on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with byte parity.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed twice per master clock cycle, although the current IDT79R4400 CPU fetches on 32-bit unit/master cycle for a peak instruction bandwidth of 400MB/sec. The line size can be configured as four or eight words to allow different applications to have a line size that delivers optimum performance.

Data Cache

For fast, single cycle data access, the IDT79R4400 includes an 16KB on-chip data cache.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

The Data Cache is direct mapped, and its line size can be configured as four or eight words. The write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck

of waiting for each store operation to finish before issuing a subsequent memory operation.

Associated with the Data Cache is the store buffer. When the R4400 executes a store instruction, this 2-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data gets written into the Data Cache in the next cycle that the Data Cache is not accessed. The store buffer allows the R4400 to execute two stores per master cycle and to perform back-to-back stores without penalty. Likewise, the R4400 can perform two loads or a load and store per master cycle without penalty, yielding 1.2GB/sec bandwidth without restrictions on instruction combinations.

When the Data Cache line does need to be written back to slower memory (either secondary cache or main memory), the processor writes the data to an internal write buffer which can hold a line (4 or 8 words) of data. By writing the data to the fast write buffer, the processor can continue executing instructions without having to wait until the write completes to the slower memory.

The IDT79R4400 caches are designed for easy and flexible integration in many types of multiprocessor systems. The Data Cache contains all the necessary state bits to allow the R4400 to maintain cache coherency across all R4400 processors in a system.

SECONDARY CACHE INTERFACE

The R4400SC and R4400MC support a secondary cache that can range in size from 128KBs to 4MBs. The cache can be configured as a unified cache or split into an instruction cache and a data cache, and it can be designed using industry standard SRAMs. The IDT R4400 provides all of the secondary cache control circuitry on chip, including ECC.

The secondary cache interface consists of a 128-bit data bus, a 25-bit tag bus, and 18-bit address bus, and SRAM control signals. The wide data bus improves performance by providing a high bandwidth data path to fill the primary caches. ECC check bits are added to both the data and tag buses to improve data integrity. All double-bit errors can be detected and all single bit-errors can be detected and all single bit-errors can be corrected on both buses.

The secondary cache access time is configurable, providing system designers with the flexibility to tailor the cache design to specific applications. The line size of the secondary cache is also configurable and can be 4-, 8-, 16-, or 32-words. The line size of the primary cache must always be less than or equal to the line size of the secondary cache.

The secondary cache is physically tagged and physically indexed. The physical cache prevents problems that could arise due to virtual address aliasing. Also, a physical cache makes multiprocessing cache coherency protocols easier to implement. The R4400MC provides a set of cache states and a mechanism for manipulating the contents and state of the cache, which are sufficient to implement a variety of cache coherency protocols, using either bus snooping or directory based schemes.

SYSTEM INTERFACE

The R4400 supports a 64-bit system interface that can be used to construct systems as simple as a uniprocessor with a direct DRAM interface and no secondary cache or as sopisticated as a fully cache coherent multiprocessor. The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 600MB/sec at 75MHz.

Figure 7 shows a typical desktop system using the R4400PC. Similarly, a high-performance desktop workstation/server system can be built using the IDT79R4400SC and adding a secondary cache.

The system interface allows the processor to access external resources in order to satisfy cache misses and uncached operations. The IDT79R4400MC, in addition to handling simple memory and I/O transactions, supports a number of cache coherency transactions of sufficient generality to support a variety of cache coherent multiprocessing models. In particular, the interface is designed to support both bus snooping and directory based multiprocessor models and supports both write-update and write-invalidate coherency protocols.

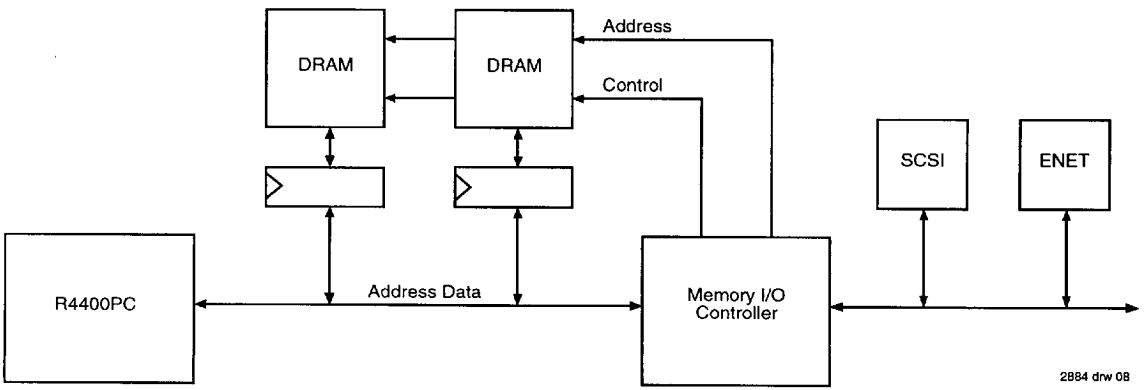


Figure 7. Typical Desktop System Block Diagram

Figure 8 shows a typical multiprocessor system using the IDT79R4400MC, an interface agent, and a secondary cache.

System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4400 and the rest of the system. It is protected with an 8-bit check bus, SysADC. The check bits can be configured as either parity or ECC, for flexibility in interfacing to either parity or ECC memory systems.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The data rate and the bus frequency at which the R4400 transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no write buffering or a fast, high performance interface can be designed to communicate with the R4400. Again, the system designer has the flexibility to make these price/perfomance tradeoffs.

System Command Bus

The R4400 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this line of data is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4400. Processor requests are initiated by the R4400 and responded to by an external device. External requests are issued by an external device and require the R4400 to respond.

The R4400 supports byte, halfword, tribyte, word, doubleword, and block transfers on the SysAD bus. In the case of a sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

Handshake Signals

There are eight handshake signals on the system interface. Two of these, $\overline{RdRdy}$ and $\overline{WrRdy}$ are used by an external device to indicate to the IDT79R4400 whether it can accept a new read or write transaction. The IDT79R4400 samples these signals before deasserting the address on read and write requests.

$\overline{ExtRqst}$ and $\overline{Release}$ are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts $\overline{ExtRqst}$. The IDT79R4400 responds by asserting $\overline{Release}$ to release the system interface to slave state.

$\overline{ValidOut}$ and $\overline{ValidIn}$ are used by the IDT79R4400 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4400 asserts $\overline{ValidOut}$ when it is driving these buses with a valid command or data, and the external device drives $\overline{ValidIn}$ when it has control of the buses and is driving a valid command or data.

Finally, there are two signals that are available on the MC version only and are used in multiprocessing systems. They are $\overline{IvdAck}$ and $\overline{IvdErr}$, and they are driven by an external device to indicate the completion status of the current processor invalidate or update request.

R4400 Requests

The R4400 is capable of issuing requests to a memory and I/O subsystem. The system interface supports two modes of operation:

- Secondary Cache mode
- No Secondary Cache mode

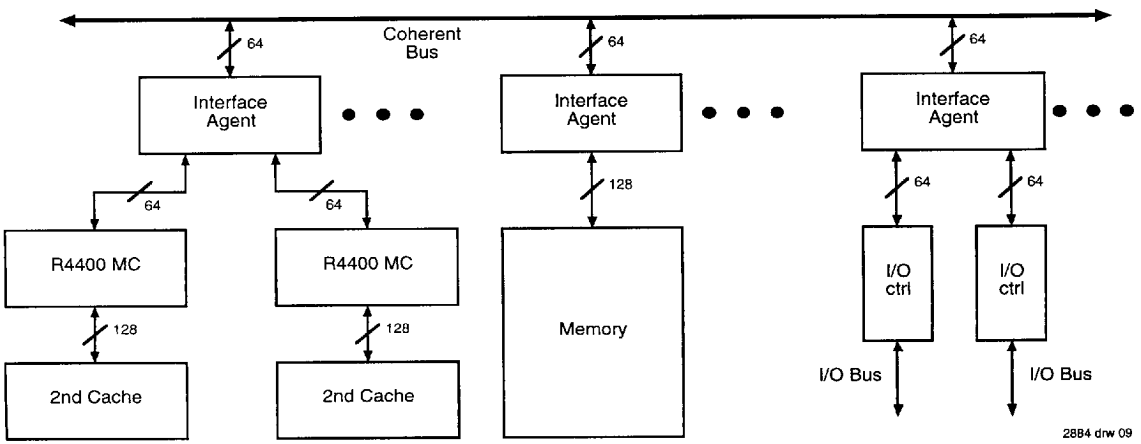


Figure 8. Multiprocessor System Using the R4400 MC

No Secondary Cache Mode

The R4400 without a secondary cache requires a non-overlapping system interface. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4400 issues another request. The R4400PC can issue read and write requests to an external device, and an external device can issue read and write requests to the R4400.

Figure 9 shows a processor read request. The R4400 asserts $\overline{\text{ValidOut}}$ and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has $\overline{\text{RdRdy}}$ asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting $\overline{\text{Release}}$. The external device can then begin sending the data to the IDT79R4400.

Secondary Cache Mode

The R4400 with a secondary cache operates in an overlapping bus transfer mode in which multiple system interface transactions may be issued in parallel. The processor may issue a combination of read request, an update or invalidate request, and a write request. For instance, when a dirty cache line needs to be replaced, the processor issues a read request immediately followed by a write request, without waiting for the read data to return. This has the advantage of "hiding" the write transaction between the read request and read response, thus increasing overall system performance. This mode of operation is not necessary or useful in R4400 systems without secondary cache since the processor contains a write buffer capable of accepting an entire primary cache line of data. Overlapping is a superset of non-overlapping system operation.

Figure 10 illustrates a processor request in overlap mode. This request is made up of a read, invalidate, and write request. Note that the protocol for the read, the invalidate, and the write are all similar to each other, with the exception that the processor also sends out valid data during the write request. In Figure 10 the processor write transaction not only occurs before the read response from the external device, but it also illustrates how an external device can hold off a write request through the deassertion of WrRdy.

External Requests

The R4400 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4400 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue cache coherency requests to the processor, such as a request for the R4400 to update, invalidate, or snoop upon its caches, or to supply a cache line of data. Additionally, an external device may need to write to the R4400 interrupt register.

The following is a list of the supported external requests:

- Read
- Write
- Invalidate

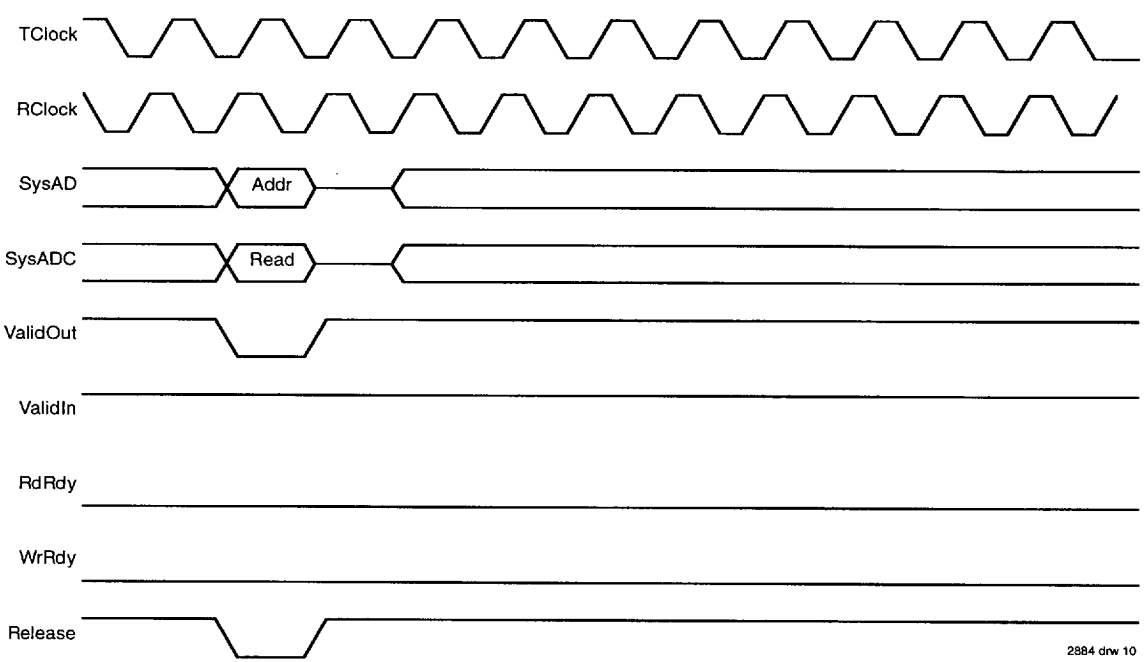


Figure 9. Processor Read Request

- Update
- Snoop
- Intervention
- Null

Figure 11 shows an example of an external snoop request. The process by which the external device issues the request is very similar to the way the R4400 issues a request. The external device first gains ownership of the system interface by asserting $\overline{\text{ExtRqst}}$ and waiting for the R4400 to assert $\overline{\text{Release}}$. The external device then sends in a valid command by asserting $\overline{\text{ValidIn}}$ and driving the SysCmd and SysAD buses with the snoop command and address. The R4400 responds to the request by asserting $\overline{\text{ValidOut}}$ and driving the SysCmd bus with the cache state of the snooped upon line.

CACHE COHERENCY CAPABILITY

With the IDT79R4400MC, cache coherence is maintained in hardware. The system control coprocessor permits the specification of different caching protocols on a per-page basis. A page may be:

- uncached
- cached but non-coherent
- cached and coherent exclusive (only one processor cache contains the data on loads and stores).
- cached and coherent exclusive on writes (write invalidate scheme-only one processor cache contains the data when that datum is written to).
- cached and coherent with updates on writes (write-update scheme).

Depending upon the amount and type of data sharing in an application, the operating system can choose the most appropriate caching strategy.

Support for processor synchronization is provided by the Load Linked and Store Conditional instructions. The Load Linked and Store Conditional instructions:

1. Provide a simple mechanism for generating all of the common synchronization primitives including test-and-set, bit-level locks, semaphores, counters, sequencers, etc. with no additional hardware overhead.
2. Operate in such a fashion that bus traffic is only generated when the state of the cache line changes.
3. Need not lock a system bus—a very important feature for larger systems.

ADVANCED FEATURES

The R4400 supports a number of other capabilities in addition to the standard processor model described above. Many of these capabilities are selected by the system designer during the processor reset sequence, via the boot time mode control interface. Features are included to support fault tolerance, system test, or other system environments.

Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (Master clock divided by 256). The low

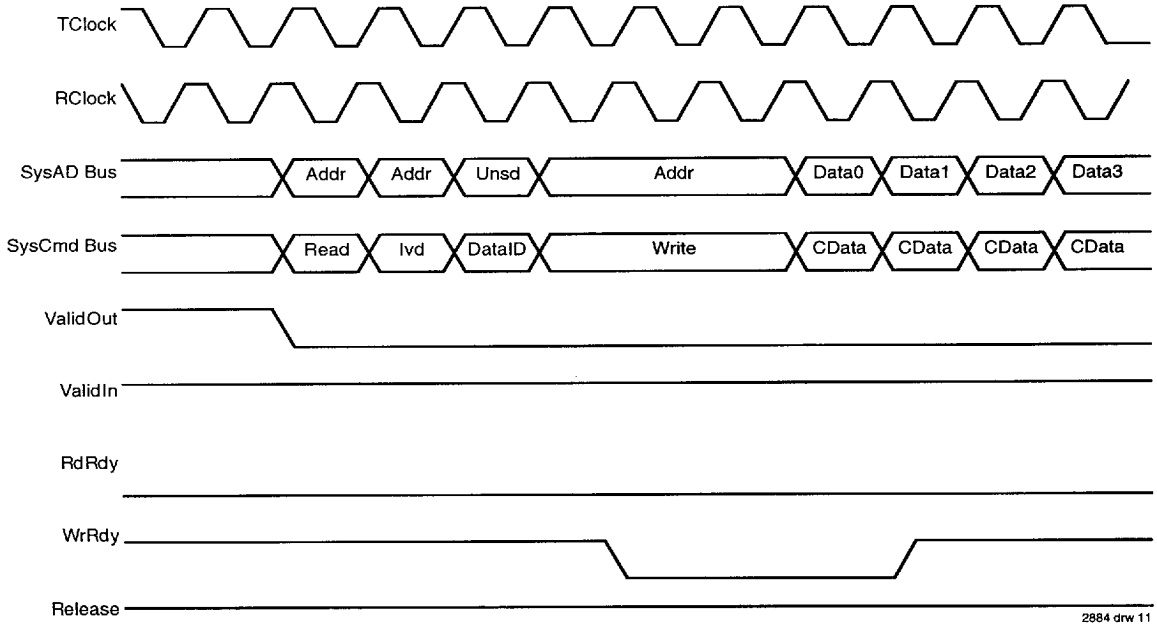


Figure 10. Processor Read, Invalidate, Write Request

frequency operation allows the initialization information to be kept in a low cost EPROM.

Immediately after the VCCOk Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

JTAG INTERFACE

The JTAG boundary scan mechanism provides a capability for testing the interconnect between the IDT79R4400 processor, the printed circuit board to which it is attached, and the other components on the board. In addition the JTAG boundary scan mechanism provides a rudimentary capability for low-speed logical testing of the secondary cache RAMs. The JTAG boundary scan mechanism does not provide any capability for testing the R4400 processor itself.

In accordance with the JTAG specification the R4400 processor contains a TAP controller, JTAG instruction register, JTAG boundary scan register, JTAG identification register, and JTAG bypass register. However, the R4400 JTAG implementation provides only the *external test* functionality of the boundary scan register.

FAULT TOLERANT SUPPORT

The R4400 has been designed to support varying models of fault tolerance. These modes include: master/checker operation and triple-modular redundancy. In addition to explicit fault-tolerant modes of operation, the design of internal processor operation is such to support processor synchronization; for example, both the TLB random replacement algorithm, and the on-chip timer, can be forced to known states via software. Thus, the IDT R4400 family can be used to build "non-stop" machines across a number of different system models.

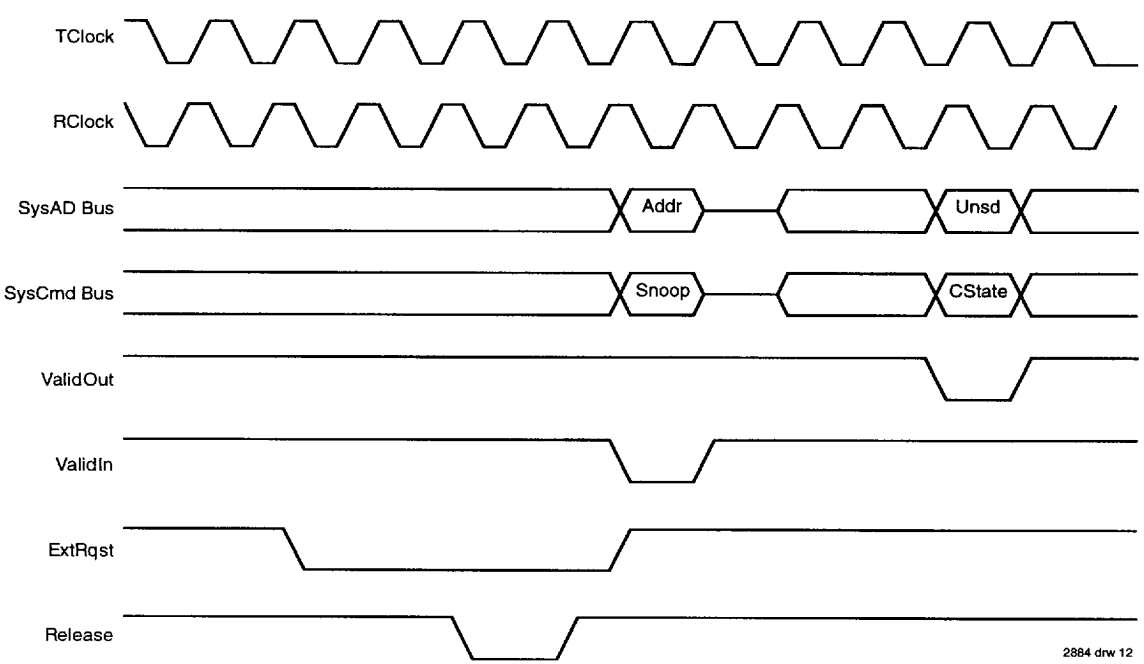


Figure 11. External Snoop Request

BOOT-TIME MODES

Serial Bit	Value	Mode Setting
0		**BlkOrder:** Block read response ordering.
	0	Sequential ordering.
	1	Sub-block ordering.
1		**EIBParMode:** System interface check bus checking.
	0	SECDED error checking and correcting mode.
	1	Byte parity.
2		**EndBit:** Byte ordering.
	0	Little Endian.
	1	Big Endian.
3		**DShMdDis:** Dirty shared mode, enables transition to dirty shared state on processor update successful.
	0	Dirty Shared Enabled.
	1	Dirty Shared Disabled.
4		**NoSCMode:** Specifies presence of secondary cache.
	0	Present.
	1	Not Present.
5:6		**SysPort:** System Interface port width (Bit 6 Most Significant).
	0	64 bits.
	1-3	Reserved(1)
7		**SC64BitMd:** Secondary cache interface port width.
	0	128 bits.
	1	Reserved(1)
8		**ElSpltMd:** Secondary cache organization
	0	Unified
	1	Reserved(1)
9:10		**SCBlkSz:** Secondary cache line size (Bit 10 Most Significant).
	0	4 words.
	1	8 words.
	2	16 words.
	3	32 words.
11:14		**XmitDatPat:** System Interface Data Rate (Bit 14 Most Significant).
	0	D
	1	DDx
	2	DDxx
	3	DxDx
	4	DDxxx
	5	DDxxxx
	6	DxxDxx
	7	DDxxxxxx
	8	DxxxDxxx
	9-15	Reserved(1)
15:17		**SysCkRatio:** PClock to SClock divisor: frequency relationship between SClock, RClock, and TClock and PClock (Bit 17 MostSignificant).
	0	Divide by 2
	1	Divide by 3
	2	Divide by 4
	3	Divide by 6
	4	Divide by 8
	5-7	Reserved(1)
18	0	Reserved (Required value)
19		**TimIntDis:** Timer Interrupt enable allows timer interrupts, otherwise the interrupt used by the timer becomes a general-purpose interrupt.
	0	Enabled
	1	Disabled
20		**PotUpdDis:** Potential invalidate enable (allows potential invalidates to be issued. Otherwise only normal invalidates are issued).

2884 tbl 03

5

Serial Bit	Value	Mode Setting
	0 1	Enabled Disabled
21:24		**TWrSUp:** Secondary cache write deassertion delay, T_{WrSup} in PCycles (Bit 24 Most Signifi cant).
	0-2 3-15	Undefined Number of PCLK cycles (Min 3; Max 15)
25:26		**TWr2Dly:** Secondary cache write assertion delay 2, T_{Wr2Dly} in PCycles (Bit 26 Most Signifi cant).
	0 1-3	Undefined Number of PCLK cycles (Min 1; Max 3)
27:28		**TWr1Dly:** Secondary cache write assertion delay 1, T_{Wr1Dly} in PCycles (Bit 28 Most Signifi cant).
	0 1-3	Undefined Number of PCLK cycles (Min 1; Max 3)
29		**TWrRc:** Secondary cache write recovery time, T_{WrRc} in PCycles either 0 or 1 cycles.
	0 1	0 cycle 1 cycle
30:32		**TDis:** Secondary cache disable time, T_{Dis} in PCycles (Bit 32 Most Significant).
	0 1	Undefined Number of PCLK cycles (Min 2; Max 7)
33:36		**TRd2Cyc:** Secondary cache read cycle time 2, T_{RdCyc2} in PCycles (Bit 36 Most Significant).
	0-2 3-15	Undefined Number of PCLK cycles (Min 3; Max 15)
37:40		**TRd2Cyc:** Secondary cache read cycle time 1, T_{RdCyc1} in PCycles, (Bit 40 Most Significant).
	0-3 4-15	Undefined Number of PCLK cycles (Min 4; Max 15)
41		**NoMPmode:** Secondary cache line is not invalidated
	0	NoMPmode off: after a secondary cache miss, the existing valid caceline is invalidated (following writeback if necessary)
	1	NoMPmode on: after a secondary cache miss, the existing valid cache line is not invali dated. Available on the R4400SC to improve performance.
42		**SCMaster Md:** selects the type of Master/Checker mode (also see description of mode bit 18).
	SCMasterMd 0 1 1 0	SIMasterMd (Bit 18) 0 Complete Master (required for single-chip operation) 1 Complete Listener (paired with Complete Master) 0 System Interface Master (SIMaster) 1 Secondary Cache Master (SCMaster, paired with SIMaster)
43:45[2]	0	Reserved.
46		**Pkg179:** R4400 type.
	0 1	Large (447 pin). SC/MC Small (179). PC
47:49		**CycDivisor:** This mode determines the clock divisior for the reduced power mode. When the RP bit in the Status Register is set to one, the pipeline clock is divided by one of the following values (Bit 49 is Most Significant).
	0 1 2 3 4-7	Divide by 2 Divide by 4 Divide by 8 Divide by 16 Reserved[1]
50:52		**Drv0_50, Drv0_75, Drv1_00:** Drive the outputs in N x MasterClock period (Bit 52 Most Significant) .
	0-1 2-3 4-7	Drive at 0.5 x MasterClockperiod. Drive at 0.75 x MasterClock period. Drive at 1.0 x MasterClock period.

2884 tbl 04

53:56		**InitP:** Initial values for the state bits that determine the pull-down di/dt and switching speed of the output buffers (Bit 53 Most Significant).
	0	Fastest pull-down rate.
	1-14	Intermediate pull-down rate.
	15	Slowest pull-down rate.
57:60		**InitN:** Initial values for the state bits that determine the pull-up di/dt and switching speed of the output buffers (Bit 57 Most Significant).
	0	Slowest pull-up rate.
	1-14	Intermediate pull-up rates.
	15	Fastest pull-up rate.
61		**EnbIDPLLR:** Enables the negative feedback loop that determines the di/dt and switching speed of the output buffers only during ColdReset.
	0	Disable di/dt control mechanism.
	1	Enable di/dt control mechanism.
Serial Bit	**Value**	**Mode Setting**
62		**EnbIDPLL:** Enables the negative feedback loop that determines the di/dt and switching speed of the output buffers during ColdReset and during normal operation.
	0	Disable di/dt control mechanism.
	1	Enable di/dt control mechanism.
63		**DsbIDPLL**: Enables PLLs that match MasterIn and produce RClock, TClock, SClock and the internal clocks.
	0	Enable PLLs.
	1	Disable PLLs.
64		**SRTristate:** Controls when output-only pins are trestated
	0	Only whe $\overline{\text{ColdReset}}$ is asserted.
	1	When $\overline{\text{Reset}}$ or $\overline{\text{ColdReset}}$ are asserted
65-255	0[2]	Reserved (must be scanned in as zeros).

2884 tbl 05

NOTES:
1. Selecting a Reserved value results in undefined processor behavior.
2. 0's must be presented for these reserved values.

PIN DESCRIPTION

The following is a list of interface, interrupt and maintenance pins available on the different package configurations.

Pin Name	Type	Description
Secondary cache interface pins available *only* on the SC and MC configuration:		
SCAddr(17:1)	Output	Secondary cache address bus A 17-bit address bus for the secondary cache.
SCAddr0(W:Z)	Output	Secondary cache address lsb To minimize loading effect, there are 4 identical copies of this signal.
SCAPar(2:0)	Output	Secondary cache address parity bus A 3-bit bus that carries the parity of the SCAddr bus and the cache control lines $\overline{\text{SCOE}}$, $\overline{\text{SCWR}}$, $\overline{\text{SCDCS}}$ and $\overline{\text{SCTCS}}$.
SCData(127:0)	Input/Output	Secondary cache data bus A 128-bit bus used to read or write cache data from/to the secondary cache.
SCDChk(15:0)	Input/Output	Secondary cache data ECC bus A 16-bit bus that carries two 8-bit ECC fields that covers the 128 bits of the SCData from/to the secondary cache. SCDChk(15:8) corresponds to SCData(127:64) and SCDChk(7:0) corresponds to SCData(63:0).
$\overline{\text{SCDCS}}$	Output	Secondary cache data chip select Chip select enable signal for the secondary cache Ram associated with SCData and SCDChk.
$\overline{\text{SCOE}}$	Output	Secondary cache output enable Output enable for the secondary cache RAM.
SCTag(24:0)	Input/Output	Secondary cache tag bus A 25-bit bus used to read or write cache tags from/to the secondary cache.
SCTChk(6:0)	Input/Output	Secondary cache tag ECC bus A 7-bit bus that carries an ECC field covering the SCTag from/to the secondary cache.

PIN DESCRIPTION (Cont.)

Pin Name	Type	Description
$\overline{SCTCS}$	Output	Secondary cache tag chip select Chip select enable signal for the secondary cache tag RAM associated with SCTag and SCTChk.
$\overline{SCWr}$(W:Z)	Output	Secondary Cache write enable Write enable for the secondary cache RAM.
System interface pins available on all parts:		
$\overline{ExtRqst}$	Input	External request Signals that the system interface needs to submit an external request.
$\overline{Release}$	Output	Release interface Signals that the processor is releasing the system interface to slave state
$\overline{RdRdy}$	Input	Read Ready Signals that an external agent can now accept a processor read, invalidate, or update request in both secondary cache and no secondary cache mode or can accept a read followed by a write request in secondary cache mode.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing check bits for the SysAD bus.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	System command/data identifier bus parity A single, even-parity bit for the SysCmd bus.
$\overline{ValidIn}$	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
$\overline{ValidOut}$	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
$\overline{WrRdy}$	Input	Write Ready Signals that an external agent can now accept a processor write request in both non-overlap and overlap mode.
System interface pins available only on the MC configuration.		
$\overline{IvdAck}$	Input	Invalidate acknowledge Signals successful completion of a processor invalidate or update request.
$\overline{IvdErr}$	Input	Invalidate error Signals unsuccessful completion of a processor invalidate or update request.
Interrupt pins available only on the PC configuration:		
$\overline{Int(5:1)}$	Input	Interrupt Five of six general processor interrupts, bit-wise ORed with bits 5:1 of the interrupt register.
Interrupt pin available on all devices:		
$\overline{Int(0)}$	Input	Interrupt One of six general processor interrupts, bit-wise ORed with bit 0 of the interrupt register.
Non-maskable interrupt pin available on all devices:		
$\overline{NMI}$	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.

2884 tbl 06

PIN DESCRIPTION (Cont.)

Pin Name	Type	Description
Boot-time mode control interface pins available on all devices:		
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.
JTAG interface pins available on all devices:		
JTDI	Input	JTAG data in JTAG serial data in.
JTCK	Input	JTAG clock input JTAG serial clock input.
JTDO	Output	JTAG data out JTAG serial data out.
JTMS	Input	JTAG command JTAG command signal, signals that the incoming serial data is command data.
Maintenance pins available on all devices:		
IOOut	Output	I/O output Output slew rate control feedback loop output. Must be connected to IOIn through a delay loop that models the IO path from the R4000 to an external agent.
IOIn	Input	I/O input Output slew rate control feedback loop input (see IOOut).
MasterClock	Input	Master clock Master clock input at the processor operating frequency.
MasterOut	Output	Master clock out Master clock output aligned with MasterClock.
RClock(1:0)	Output	Receive clocks Two identical receive clocks at the system interface frequency.
SyncOut	Output	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn	Input	Synchronization clock in Synchronization clock input. See SyncOut.
TClock(1:0)	Output	Transmit clocks Two identical transmit clocks at the system interface frequency.
VCCOk	Input	VCC is OK When asserted, this signal indicates to the R4000 that the +5 volt power supply has been above 4.75 volts for more than 100 milliseconds and will remain stable. The assertion of VCCOk initiates the reading of the boot-time mode control serial stream.
$\overline{\text{ColdReset}}$	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of $\overline{\text{ColdReset}}$. $\overline{\text{ColdReset}}$ must be de-asserted synchronously with MasterOut.
$\overline{\text{Reset}}$	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. $\overline{\text{Reset}}$ must be de-asserted synchronously with MasterOut.
$\overline{\text{Fault}}$	Output	Fault Mismatch output of boundary comparators.
VccP	Input	Quiet VCC for PLL Quiet Vcc for the internal phase locked loop.

5

PIN DESCRIPTION (Cont.)

VssP	Input	Quiet VSS for PLL Quiet Vss for the internal phase locked loop.
Maintenance pins available only on the SC and MC configurations:		
Status(7:0)	Status	Output An 8-bit bus that indicates the current operation status of the processor.

2884 tbl 07

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TC	Operating Temperature	0 to +85 (Case)	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

2884 tbl 09

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = -3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
R4400 Com.	0°C to +85°C (Case)	0V	5.0 ±5%
RV4400 Com.	0°C to +85°C (Case)	0V	3.3 ±5%

2884 tbl 10

DC ELECTRICAL CHARACTERISTICS—R4400 COMMERCIAL TEMPERATURE RANGE

(VCC = 5.0V ± 5%; TCase = 0°C to +85°C)

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	IOH = –4mA	3.5	—	3.5	—	3.5	—	V
VOHC	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)(3)	IOH = –4mA	4.0	—	4.0	—	4.0	—	V
VOL	Output LOW Voltage	IOL = 4mA	—	0.4	—	0.4	—	0.4	V
VIH	Input HIGH Voltage		2.0	VCC + .5	2.0	VCC + .5	2.0	VCC + .5	V
VIL	Input LOW Voltage(1,2)		–0.5(1)	0.8	–0.5(1)	0.8	–0.5(1)	0.8	V
VIHC	Input HIGH Voltage (MasterClock, SyncIn)		0.8 VCC	VCC + .5	0.8 VCC	VCC + .5	0.8 VCC	VCC + .5	V
VILC	Input LOW Voltage (MasterClock, SyncIn)		–0.5(1)	0.2 VCC	–0.5(1)	0.2 VCC	–0.5(1)	0.2 VCC	V
CIn	Input Capacitance		—	10	—	10	—	10	pF
COut	Output Capacitance		—	10	—	10	—	10	pF
ILeak	Input Leakage		—	10	—	10	—	10	µA
IOLeak	Input/Output Leakage		—	20	—	20	—	20	µA
ICC	Operating Current	VCC = 5V, TC=25°C	—	2.8	—	3.2	—	3.6	A

2884 tbl 11

NOTES:
1. VIL (min.) = –3.0V for pulse width less than 15ns.
2. Except for MasterClock input.
3. Applies to TClock, RClock, MasterOut, and ModeClock outputs.

AC ELECTRICAL CHARACTERISTICS—R4400 COMMERCIAL TEMPERATURE RANGE

(Vcc=5.0V ± 5%; Tcase = 0°C to +85°C) MasterClock and Clock Parameters[2]

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMCkHigh	MasterClock High	[3]	4	—	3	—	3	—	ns
TMCkLow	MasterClock Low	[3]	4	—	3	—	3	—	ns
	MasterClock Freq[1]		25	50	25	67	25	75	MHz
TMCP	MasterClock Period		20	40	15	40	13.3	40	ns
TMCJitter	Clock Jitter (on RClock, TClock, MasterOut, SyncOut)		—	±500	—	±500	—	±500	ps
TMCRise	MasterClock Rise Time		—	5	—	4	—	3.5	ns
TMCFall	MasterClock Fall Time		—	5	—	4	—	3.5	ns
TModeCKP	ModeClock Period		—	256*TMCP	—	256*TMCP	—	256*TMCP	ns
TJTAGCKP	JTAG Clock Period		4*TMCP	—	4*TMCP	—	4*TMCP	—	ns

2884 tbl 12

NOTES:
1. Operation of the R4400 is only guaranteed with the phase lock loop enabled.
2. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
3. Transition ≤ 5ns for 50, 67MHz; transition ≤ 3.5ns for 75MHz.

5

SYSTEM INTERFACE PARAMETERS—R4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TDO[1,2,3]	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	3.5	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
TDS	Data Setup		5	—	5	—	3.5	—	ns
TDH	Data Hold		1.5	—	1.5	—	1	—	ns

2884 tbl 13a

NOTES:
1. When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the clock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

BOOT MODE INTERFACE PARAMETERS—R4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMDS	Mode Data Setup		3	—	3	—	3	—	MCLK cycles
TMDH	Mode Data Hold		0	—	0	—	0	—	MCLK cycles

2884 tbl 13b

SECONDARY CACHE INTERFACE PARAMETERS—R4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{SCO}[1,2,3]	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	2	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
T_{SCDS}	Data Setup		5	—	5	—	3.5	—	ns
T_{SCDH}	Data Hold		2	—	1.5	—	1	—	ns
T_{Rd1Cyc}[4]	Cycle length of 4 word Rd		4	15	4	15	4	15	Pcycles
T_{Dis}[4]	Cycles between Rd & Wr		2	7	2	7	2	7	Pcycles
T_{Rd2Cyc}[4]	Cycle length of 8 word Rd		3	15	3	15	3	15	Pcycles
T_{Wr1Dly}[4]	Cycles bet. Addr & $\overline{SCWr}$		1	3	1	3	1	3	Pcycles
T_{WrRc}[4]	Cycles bet. deassertion of $\overline{SCWr}$ to start of next cycle		0	1	0	1	0	1	Pcycles
T_{WrSUp}[4]	Cycles from second doubleword to $\overline{SCWr}$		2	15	2	15	3	15	Pcycles
T_{Wr2Dly}[4]	Cycles between1st & 2nd word in 8-word write		1	3	1	3	1	3	Pcycles

2884 tbl 14

NOTES:
1. When the dynamic output slew rate control Mode bits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the Pclock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Number of cycles is configured through the boot time mode control.

CAPACITIVE LOAD DERATION

Symbol	Parameter	50MHz		67MHz		75MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
CLD	Load Derate	—	2	—	2	—	2	ns/25pF

2884 tbl 15

DC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(V_{CC} = 3.3V ± 5%; Tcase = 0°C to +85°C)

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA	2.4	—	2.4	—	2.4	—	V
V_{OHC}	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)(3)	I_{OH} = –4mA	2.7	—	2.7	—	2.7	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + .5	2.0	V_{CC} + .5	2.0	V_{CC} + .5	V
V_{IL}	Input LOW Voltage(1,2)		–0.5(1)	0.8	–0.5(1)	0.8	–0.5(1)	0.8	V
V_{IHC}	Input HIGH Voltage (MasterClock, SyncIn)		0.8 V_{CC}	V_{CC} + .5	0.8 V_{CC}	V_{CC} + .5	0.8 V_{CC}	V_{CC} + .5	V
V_{ILC}	Input LOW Voltage (MasterClock, SyncIn)		–0.5(1)	0.2 V_{CC}	–0.5(1)	0.2 V_{CC}	–0.5(1)	0.2 V_{CC}	V
C_{In}	Input Capacitance		—	10	—	10	—	10	pF
C_{Out}	Output Capacitance		—	10	—	10	—	10	pF
I_{Leak}	Input Leakage		—	10	—	10	—	10	µA
I_{OLeak}	Input/Output Leakage		—	20	—	20	—	20	µA
I_{CC}	Operating Current	V_{CC} = 3.3V, Tc=25°C	—	2.0	—	2.4	—	2.8	A

2884 tbl 11

NOTES:
1. V_{IL} (min.) = -3.0V for pulse width less than 15ns.
2. Except for MasterClock input.
3. Applies to TClock, RClock, MasterOut, and ModeClock outputs.

DC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(V_{CC} = 3.3V ± 5%; Tcase = 0°C to +85°C)

Symbol	Parameter	Conditions	88MHz		100MHz		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V
V_{OHC}	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)(3)	I_{OH} = –4mA	2.7	—	2.7	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + .5	2.0	V_{CC} + .5	V
V_{IL}	Input LOW Voltage(1,2)		–0.5(1)	0.8	–0.5(1)	0.8	V
V_{IHC}	Input HIGH Voltage (MasterClock, SyncIn)		0.8 V_{CC}	V_{CC} + .5	0.8 V_{CC}	V_{CC} + .5	V
V_{ILC}	Input LOW Voltage (MasterClock, SyncIn)		–0.5(1)	0.2 V_{CC}	–0.5(1)	0.2 V_{CC}	V
C_{In}	Input Capacitance		—	10	—	10	pF
C_{Out}	Output Capacitance		—	10	—	10	pF
I_{Leak}	Input Leakage		—	10	—	10	µA
I_{OLeak}	Input/Output Leakage		—	20	—	20	µA
I_{CC}	Operating Current	V_{CC} = 3.3V, Tc=25°C	—	TBD	—	TBD	A

2884 tbl 11

NOTES:
1. V_{IL} (min.) = –3.0V for pulse width less than 15ns.
2. Except for MasterClock input.
3. Applies to TClock, RClock, MasterOut, and ModeClock outputs.

AC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(Vcc=3.3V ± 5%; Tcase = 0°C to +85°C) MasterClock and Clock Parameters[2]

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMCkHigh	MasterClock High	[3]	4	—	3	—	3	—	ns
TMCkLow	MasterClock Low	[3]	4	—	3	—	3	—	ns
	MasterClock Freq[1]		25	50	25	67	25	75	MHz
TMCP	MasterClock Period		20	40	15	40	13.3	40	ns
TMCJitter	Clock Jitter (on RClock, TClock, MasterOut, SyncOut)		—	±500	—	±500	—	±500	ps
TMCRise	MasterClock Rise Time		—	5	—	4	—	3.5	ns
TMCFall	MasterClock Fall Time		—	5	—	4	—	3.5	ns
TModeCKP	ModeClock Period		—	256*TMCP	—	256*TMCP	—	256*TMCP	ns
TJTAGCKP	JTAG Clock Period		4*TMCP	—	4*TMCP	—	4*TMCP	—	ns

NOTES:
1. Operation of the R4400 is only guaranteed with the phase lock loop enabled.
2. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
3. Transition ≤ 5ns for 50, 67MHz; transition ≤ 3.5ns for 75MHz.

2884 tbl 12

AC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(Vcc=3.3V ± 5%; Tcase = 0°C to +85°C) MasterClock and Clock Parameters[2]

Symbol	Parameter	Conds.	88MHz		100MHz		Units
			Min.	Max.	Min.	Max.	
TMCkHigh	MasterClock High	[3]	2.5	—	2.5	—	ns
TMCkLow	MasterClock Low	[3]	2.5	—	2.5	—	ns
	MasterClock Freq[1]		25	88	25	100	MHz
TMCP	MasterClock Period		11.3	40	10	40	ns
TMCJitter	Clock Jitter (on RClock, TClock, MasterOut, SyncOut)			±500		±500	ps
TMCRise	MasterClock Rise Time			2.5	—	2.5	ns
TMCFall	MasterClock Fall Time			2.5		2.5	ns
TModeCKP	ModeClock Period			256*TMCP		256*TMCP	ns
TJTAGCKP	JTAG Clock Period		4*TMCP	—	4*TMCP	—	ns

NOTES:
1. Operation of the R4400 is only guaranteed with the phase lock loop enabled.
2. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
3. Transition ≤ 2.5ns5.

2884 tbl 12

SYSTEM INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{DO}[1,2,3]	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	3.5	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
T_{DS}	Data Setup		5	—	5	—	3.5	—	ns
T_{DH}	Data Hold		1.5	—	1.5	—	1	—	ns

2884 tbl 13a

NOTES:
1. When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the clock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

SYSTEM INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	88MHz		100MHz		Units
			Min.	Max.	Min.	Max.	
T_{DO}[1,2,3]	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	1	5	1	5	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	5	10	6	10	ns
T_{DS}	Data Setup		3.5	—	3.5	—	ns
T_{DH}	Data Hold		1	—	1	—	ns

2884 tbl 13a

NOTES:
1. When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56] = 15, Modebits [57:60] = 0.
2. Timings are measured from 1.5V of the clock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

BOOT MODE INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{MDS}	Mode Data Setup		3	—	3	—	3	—	MCLK cycles
T_{MDH}	Mode Data Hold		0	—	0	—	0	—	MCLK cycles

2884 tbl 13b

BOOT MODE INTERFACE PARAMETERS—R4400

Symbol	Paramete	88MHz		100MHz		Units
		Min.	Max.	Min.	Max.	
T_{MDS}	Mode Data Setup	3		3		MCLK cycles
T_{MDH}	Mode Data Hold	0		0		MCLK cycles

2884 tbl 13b

SECONDARY CACHE INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{SCO}[1,2,3]	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	2	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
T_{SCDS}	Data Setup		5	—	5	—	3.5	—	ns
T_{SCDH}	Data Hold		2	—	1.5	—	1	—	ns
T_{Rd1Cyc}[4]	Cycle length of 4 word Rd		4	15	4	15	4	15	Pcycles
T_{Dis}[4]	Cycles between Rd & Wr		2	7	2	7	2	7	Pcycles
T_{Rd2Cyc}[4]	Cycle length of 8 word Rd		3	15	3	15	3	15	Pcycles
T_{Wr1Dly}[4]	Cycles bet. Addr & $\overline{SCWr}$		1	3	1	3	1	3	Pcycles
T_{WrRc}[4]	Cycles bet. deassertion of $\overline{SCWr}$ to start of next cycle		0	1	0	1	0	1	Pcycles
T_{WrSUp}[4]	Cycles from second doubleword to $\overline{SCWr}$		2	15	2	15	3	15	Pcycles
T_{Wr2Dly}[4]	Cycles between1st & 2nd word in 8-word write		1	3	1	3	1	3	Pcycles

2884 tbl 14

SECONDARY CACHE INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	88MHz		100MHz		Units
			Min.	Max	Min	Max.	
T_{SCO}[1,2,3]	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	1	5	1	5	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	5		5		ns
T_{SCDS}	Data Setup		3.5		3.5		ns
T_{SCDH}	Data Hold		1		1		ns
T_{Rd1Cyc}[4]	Cycle length of 4 word Rd		4		4		Pcycles
T_{Dis}[4]	Cycles between Rd & Wr		2		2		Pcycles
T_{Rd2Cyc}[4]	Cycle length of 8 word Rd		3		3		Pcycles
T_{Wr1Dly}[4]	Cycles bet. Addr & $\overline{SCWr}$		1		1		Pcycles
T_{WrRc}[4]	Cycles bet. deassertion of $\overline{SCWr}$ to start of next cycle		0		0		Pcycles
T_{WrSUp}[4]	Cycles from second doubleword to $\overline{SCWr}$		2		2		Pcycles
T_{Wr2Dly}[4]	Cycles between1st & 2nd word in 8-word write		1		1		Pcycles

2884 tbl 14

NOTES:

1. When the dynamic output slew rate control Mode bits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the Pclock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Number of cycles is configured through the boot time mode control.

CAPACITIVE LOAD DERATION

Symbol	Parameter	50MHz		67MHz		75MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
CLD	Load Derate	—	2	—	2	—	2	ns/25pF

2884 tbl 15

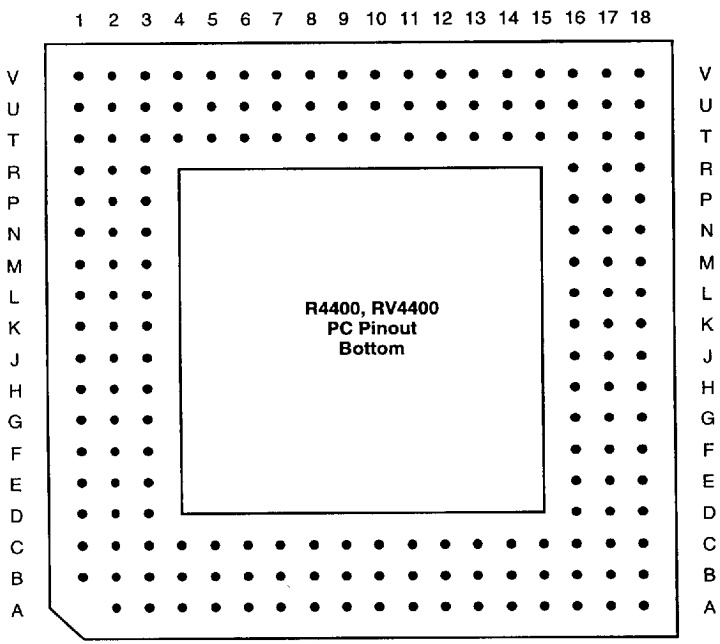
CAPACITIVE LOAD DERATION

Symbol	Parameter	Conditions	88MHz		100MHz		Units
			Min.	Max	Min	Max.	
CLD	Load Derate			2		2	ns/25pF

PRELIMINARY

2884 tbl 15

PHYSICAL SPECIFICATIONS



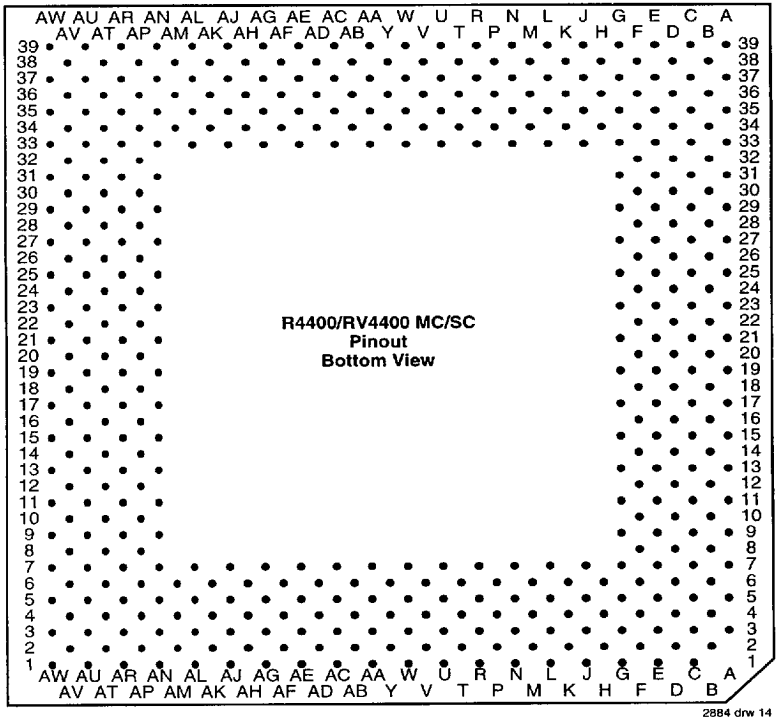
2884 drw 13

IDT79R4400/RV4400 PC PACKAGE PINOUT

R4400 Function	PC Pkg Pin	R4400 Function	PC Pkg Pin	R4400 Function	PC Pkg Pin
ColdReset	T14	SysAD29	T16	VssP	K16
ExtRqst	U2	SysAD30	R17	Vcc	A2
Fault	B16	SysAD31	M16	Vcc	A4
Reserved (NC)	U10	SysAD32	H2	Vcc	A7
Vcc	T9	SysAD33	G3	Vcc	A9
IOIn	T13	SysAD34	F3	Vcc	A11
IOOut	U12	SysAD35	D2	Vcc	A13
Int0	N2	SysAD36	C3	Vcc	A16
Int1	L3	SysAD37	B3	Vcc	B18
Int2	K3	SysAD38	C6	Vcc	C1
Int3	J3	SysAD39	C7	Vcc	D18
Int4	H3	SysAD40	C10	Vcc	F1
Int5	F2	SysAD41	C11	Vcc	G18
JTCK	H17	SysAD42	B13	Vcc	H1
JTDI	G16	SysAD43	A15	Vcc	J18
JTDO	F16	SysAD44	C15	Vcc	K1
JTMS	E16	SysAD45	B17	Vcc	L18
MasterClock	J17	SysAD46	E17	Vcc	M1
MasterOut	P17	SysAD47	F17	Vcc	N18
ModeClock	B4	SysAD48	L2	Vcc	R1
ModeIn	U4	SysAD49	M3	Vcc	T18
NMI	U7	SysAD50	N3	Vcc	U1
PLLCap0	****	SysAD51	R2	Vcc	V3
PLLCap1	****	SysAD52	T3	Vcc	V6
RClock0	T17	SysAD53	U3	Vcc	V8
RClock1	R16	SysAD54	T6	Vcc	V10
RdRdy	T5	SysAD55	T7	Vcc	V12
Release	V5	SysAD56	T10	Vcc	V14
Reset	U16	SysAD57	T11	Vcc	V17
SyncIn	J16	SysAD58	U13	Vss	A3
SyncOut	P16	SysAD59	V15	Vss	A6
SysAD0	J2	SysAD60	T15	Vss	A8
SysAD1	G2	SysAD61	U17	Vss	A10
SysAD2	E1	SysAD62	N16	Vss	A12
SysAD3	E3	SysAD63	N17	Vss	A14
SysAD4	C2	SysADC0	C8	Vss	A17
SysAD5	C4	SysADC1	G17	Vss	A18
SysAD6	B5	SysADC2	T8	Vss	B1
SysAD7	B6	SysADC3	L16	Vss	C18
SysAD8	B9	SysADC4	B8	Vss	D1
SysAD9	B11	SysADC5	H16	Vss	F18
SysAD10	C12	SysADC6	U8	Vss	G1
SysAD11	B14	SysADC7	L17	Vss	H18
SysAD12	B15	SysCmd0	E2	Vss	J1
SysAD13	C16	SysCmd1	D3	Vss	K18
SysAD14	D17	SysCmd2	B2	Vss	L1
SysAD15	E18	SysCmd3	A5	Vss	M18
SysAD16	K2	SysCmd4	B7	Vss	N1
SysAD17	M2	SysCmd5	C9	Vss	P18
SysAD18	P1	SysCmd6	B10	Vss	R18
SysAD19	P3	SysCmd7	B12	Vss	T1
SysAD20	T2	SysCmd8	C13	Vss	U18
SysAD21	T4	SysCmdP	C14	Vss	V1
SysAD22	U5	TClock0	C17	Vss	V2
SysAD23	U6	TClock1	D16	Vss	V4
SysAD24	U9	VCCOk	M17	Vss	V7
SysAD25	U11	ValidIn	P2	Vss	V9
SysAD26	T12	ValidOut	R3	Vss	V11
SysAD27	U14	WrRdy	C5	Vss	V13
SysAD28	U15	VccP	K17	Vss	V16
				Vss	V18

2884 tbl 16

PHYSICAL SPECIFICATIONS



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IDT79R4400/RV4400 MC/SC PACKAGE PINOUT

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
ColdReset	AW37	SCDChk9	N37	SCData53	AR13
ExtRqst	AV2	SCDChk10	AU17	SCData54	AR15
Fault	C39	SCDChk11	AG37	SCData55	AT18
Reserved (NC)	AV24	SCDChk12	E19	SCData56	AU23
IOIn	AV32	SCDChk13	R35	SCData57	AT26
IOOut	AV28	SCDChk14	AR19	SCData58	AR27
Int0	AL1	SCDChk15	AE35	SCData59	AN29
IvdAck(1)	AA35	SCData0	R3	SCData60	AP32
IvdErr(1)	AA39	SCData1	R7	SCData61	AN35
JTCK	U39	SCData2	L5	SCData62	AJ35
JTDI	N39	SCData3	F8	SCData63	AE33
JTDO	J39	SCData4	C9	SCData64	V4
JTMS	G37	SCData5	F12	SCData65	R5
MasterClock	AA37	SCData6	G15	SCData66	N5
MasterOut	AJ39	SCData7	E17	SCData67	E5
ModeClock	B8	SCData8	G21	SCData68	G9
ModeIn	AV8	SCData9	C25	SCData69	E11
NMI	AV16	SCData10	G25	SCData70	G13
PLLCap0	****	SCData11	E29	SCData71	D14
PLLCap1	****	SCData12	G31	SCData72	C21
RClock0	AM34	SCData13	C35	SCData73	D22
RClock1	AL33	SCData14	K36	SCData74	E25
RdRdy	AW7	SCData15	N35	SCData75	G27
Release	AV12	SCData16	AE3	SCData76	C31
Reset	AU39	SCData17	AG5	SCData77	F32
Reserved (NC)	Y2	SCData18	AK4	SCData78	J35
SCAPar0	U5	SCData19	AN9	SCData79	M34
SCAPar1	U1	SCData20	AU9	SCData80	AC7
SCAPar2	P4	SCData21	AN13	SCData81	AE5
SCAddr1	AL5	SCData22	AT14	SCData82	AG7
SCAddr2	AG1	SCData23	AR17	SCData83	AR5
SCAddr3	AE7	SCData24	AT22	SCData84	AR9
SCAddr4	AC1	SCData25	AU25	SCData85	AR11
SCAddr5	AC5	SCData26	AN27	SCData86	AN15
SCAddr6	AC3	SCData27	AR29	SCData87	AP16
SCAddr7	AA1	SCData28	AN31	SCData88	AU21
SCAddr8	AB4	SCData29	AR35	SCData89	AN23
SCAddr9	AA5	SCData30	AK36	SCData90	AR25
SCAddr10	AA7	SCData31	AG35	SCData91	AP28
SCAddr11	AA3	SCData32	T6	SCData92	AU31
SCAddr12	W3	SCData33	L3	SCData93	AR33
SCAddr13	Y6	SCData34	L7	SCData94	AL35
SCAddr14	W5	SCData35	E7	SCData95	AH34
SCAddr15	W7	SCData36	G11	SCData96	U7
SCAddr16	W1	SCData37	E13	SCData97	N3
SCAddr17	U3	SCData38	E15	SCData98	N7
SCAddr0W	AN7	SCData39	G17	SCData99	C5
SCAddr0X	AN5	SCData40	C23	SCData100	E9
SCAddr0Y	AM6	SCData41	F24	SCData101	C11
SCAddr0Z	AL7	SCData42	E27	SCData102	C13
SCDCS	M6	SCData43	D30	SCData103	F16
SCDChk0	G19	SCData44	C33	SCData104	E21
SCDChk1	T34	SCData45	E35	SCData105	G23
SCDChk2	AP20	SCData46	L35	SCData106	C27
SCDChk3	AD34	SCData47	R33	SCData107	F28
SCDChk4	C19	SCData48	AF4	SCData108	E31
SCDChk5	R37	SCData49	AJ3	SCData109	G33
SCDChk6	AU19	SCData50	AJ7	SCData110	J37
SCDChk7	AE37	SCData51	AP8	SCData111	N33
SCDChk8	C17	SCData52	AT10	SCData112	AD6

2884 tbl 17

IDT79R4400/RV4400 MC/SC PACKAGE PINOUT (continued)

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
SCData113	AG3	Status7	AC33	SysAD57	AW27
SCData114	AJ5	SyncIn	W39	SysAD58	AW31
SCData115	AU5	SyncOut	AN39	SysAd59	AW35
SCData116	AN11	SysAD0	T2	SysAD60	AU37
SCData117	AU11	SysAD1	M2	SysAD61	AR39
SCData118	AU13	SysAD2	J3	SysAD62	AL39
SCData119	AN17	SysAD3	G3	SysAD63	AG39
SCData120	AR21	SysAD4	C1	SysADC0	A17
SCData121	AP24	SysAD5	A3	SysADC1	R39
SCData122	AU27	SysAD6	A9	SysADC2	AW17
SCData123	AT30	SysAD7	A13	SysADC3	AD38
SCData124	AU33	SysAD8	A21	SysADC4	A19
SCData125	AN33	SysAD9	A25	SysADC5	T38
SCData126	AL37	SysAD10	A29	SysADC6	AW19
SCData127	AG33	SysAD11	A33	SysADC7	AC39
$\overline{\text{SCOE}}$	N1	SysAd12	B38	SysCmd0	G1
$\overline{\text{SCTCS}}$	J1	SysAD13	E37	SysCmd1	E3
SCTChk0	AN21	SysAD14	G39	SysCmd2	B2
SCTChk1	AN19	SysAD15	L39	SysCmd3	B12
SCTChk2	AU15	SysAD16	AD2	SysCmd4	B16
SCTChk3	AP12	SysAD17	AH2	SysCmd5	B20
SCTChk4	AU7	SysAD18	AL3	SysCmd6	B24
SCTChk5	AR7	SysAD19	AN3	SysCmd7	B28
SCTChk6	AH6	SysAD20	AU1	SysCmd8	B32
SCTag0	K4	SysAD21	AW3	SysCmdP	A37
SCTag1	G7	SysAD22	AW9	TClock0	H34
SCTag2	C7	SysAD23	AW13	TClock1	J33
SCTag3	D10	SysAD24	AW21	VCCOk	AE39
SCTag4	C15	SysAD25	AW25	$\overline{\text{ValidIn}}$	AN1
SCTag5	D18	SysAD26	AW29	$\overline{\text{ValidOut}}$	AR3
SCTag6	F20	SysAD27	AW33	$\overline{\text{WrRdy}}$	A7
SCTag7	E23	SysAD28	AV38	VccSense	W33
SCTag8	D26	SysAD29	AR37	VssSense	U37
SCTag9	C29	SysAD30	AM38	VccP	AA33
SCTag10	G29	SysAD31	AH38	VssP	Y34
SCTag11	E33	SysAD32	R1	Vcc	A39
SCTag12	G35	SysAD33	L1	Vcc	B6
SCTag13	L33	SysAD34	H2	Vcc	B10
SCTag14	L37	SysAD35	E1	Vcc	B18
SCTag15	P36	SysAD36	C3	Vcc	B26
SCTag16	AF36	SysAD37	A5	Vcc	B34
SCTag17	AJ37	SysAD38	A11	Vcc	D4
SCTag18	AJ33	SysAd39	A15	Vcc	D8
SCTag19	AN37	SysAD40	A23	Vcc	D16
SCTag20	AU35	SysAD41	A27	Vcc	D24
SCTag21	AR31	SysAd42	A31	Vcc	D32
SCTag22	AU29	SysAD43	A35	Vcc	D36
SCTag23	AN25	SysAd44	C37	Vcc	F2
SCTag24	AR23	SysAD45	E39	Vcc	F14
$\overline{\text{SCWrW}}$	J5	SysAD46	H38	Vcc	F22
$\overline{\text{SCWrX}}$	J7	SysAD47	M38	Vcc	F30
$\overline{\text{SCWrY}}$	H6	SysAD48	AE1	Vcc	F38
$\overline{\text{SCWrZ}}$	G5	SysAD49	AJ1	Vcc	H4
Status0	U33	SysAD50	AM2	Vcc	H36
Status1	U35	SysAD51	AR1	Vcc	K6
Status2	V36	SysAD52	AU3	Vcc	K38
Status3	W35	SysAD53	AW5	Vcc	P2
Status4	W37	SysAD54	AW11	Vcc	P34
Status5	AC37	SysAD55	AW15	Vcc	T4
Status6	AC35	SysAD56	AW23		

2884 tbl 18

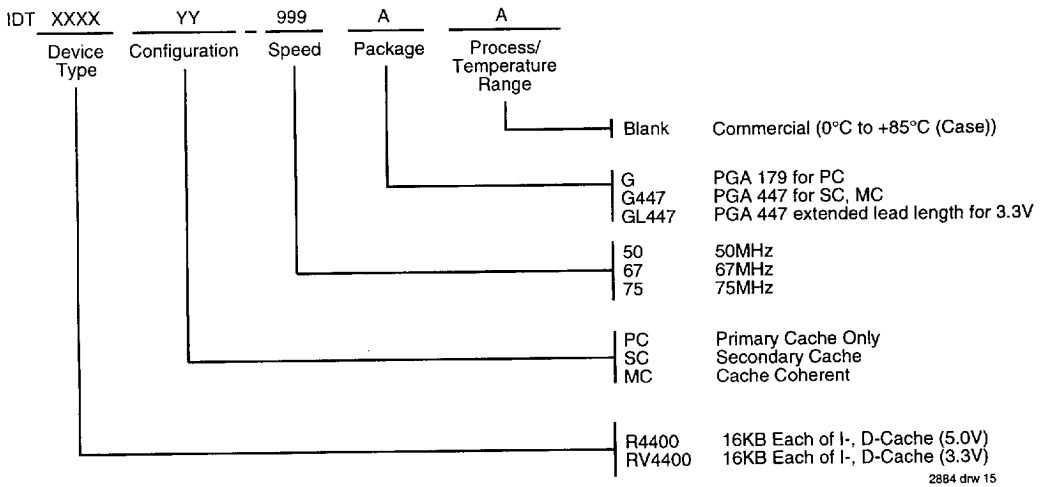
IDT79R4400 MC/SC PACKAGE PINOUT (continued)

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
Vcc	T36	Vcc	AV34	Vss	Y4
Vcc	V6	Vcc	AW1	Vss	Y36
Vcc	V38	Vcc	AW39	Vss	AB6
Vcc	Y38	Vss	B4	Vss	AB36
Vcc	AB2	Vss	B14	Vss	AB38
Vcc	AB34	Vss	B22	Vss	AF2
Vcc	AD4	Vss	B30	Vss	AF34
Vcc	AD36	Vss	B36	Vss	AH4
Vcc	AF6	Vss	D2	Vss	AH36
Vcc	AF38	Vss	D6	Vss	AK6
Vcc	AK2	Vss	D12	Vss	AK38
Vcc	AK34	Vss	D20	Vss	AP4
Vcc	AM4	Vss	D28	Vss	AP6
Vcc	AM36	Vss	D34	Vss	AP14
Vcc	AP2	Vss	D38	Vss	AP22
Vcc	AP10	Vss	F4	Vss	AP30
Vcc	AP18	Vss	F6	Vss	AP34
Vcc	AP26	Vss	F10	Vss	AP36
Vcc	AP38	Vss	F18	Vss	AT2
Vcc	AT4	Vss	F26	Vss	AT6
Vcc	AT8	Vss	F34	Vss	AT12
Vcc	AT16	Vss	F36	Vss	AT20
Vcc	AT24	Vss	K2	Vss	AT28
Vcc	AT32	Vss	K34	Vss	AT34
Vcc	AT36	Vss	M4	Vss	AT38
Vcc	AV6	Vss	M36	Vss	AV4
Vcc	AV14	Vss	P6	Vss	AV10
Vcc	AV20	Vss	P38	Vss	AV18
Vcc	AV22	Vss	V2	Vss	AV26
Vcc	AV30	Vss	V34	Vss	AV36

NOTE:
1. Available in IDT79R4400MC only. For IDT79R4400SC, these inputs must be pulled to Vcc.

2884 tbl 19

ORDERING INFORMATION



2884 drw 15

5

VALID COMBINATIONS

R4400 PC — 50, 67, 75	G
R4400 SC — 50, 67, 75	G447
R4400 MC — 50, 67, 75	G447
RV4400 SC — 50, 67, 75, 100	GL447
RV4400 MC — 50, 67, 75, 100	GL447