M35076-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35076-XXXSP is a character pattern display control IC can display on the digital camera, the digital video, the digital television, the CRT display, the liquid crystal display and the plasma display. It can display 2 pages (24 characters × 12 lines per 1 page) at the same time. It uses a silicon gate CMOS process and it housed in a 20-pin shrink DIP package (M35076-XXXSP).
For M35076-001SP that is a standard ROM version of M35076-XXXSP respectively, the character pattern is also mentioned.

FEATURES

- Screen composition ..... 24 characters × 12 lines × 2 pages
- Number of characters displayed ..... 288 (Max.) × 2 pages
- Character composition ..... 12 × 18 dot matrix
- Characters available ..... 0 page:256 characters
  1 page:256 characters
- Character sizes available ..... 4 (vertical) × 2 (horizontal)
- Display locations available
  Horizontal direction ..... 2007 locations
  Vertical direction ..... 1023 locations
- Blinking ..... Character units
  Cycle : division of vertical synchronization signal into 32 or 64
  Duty : 25%, 50%, or 75%
- Data input ..... By the 16-bit serial input function
  ..... By the I^2C-BUS serial input function(at V_{DD}=5V only)
- Coloring for ROM character
  Character color ..... 8 colors (Character unit)
  Background coloring ..... 8 colors (Character unit)
  Border (shadow) coloring ..... 8 colors (RGB output)
  Specified by register
  Raster coloring ..... 8 colors (RGB output)
  Specified by register
- Blanking — Character size blanking
  Border size blanking
  Matrix-outline blanking
  All blanking (all raster area)
- Output ports
  8 shared output ports (toggled between RGB output)
- Display RAM erase function
- Display oscillation stop function

<VDD=5V>

- Display input frequency range
  External clock mode 1 ..... F_{OSC} = 6.3 MHz to 80.0 MHz
  External clock mode 2 ..... F_{OSC} = 20.0 MHz to 110.0 MHz
  Internal clock mode ..... F_{OSC} = 20.0 MHz to 110.0 MHz
- Horizontal synchronous input frequency
  ..... H.sync = 15 kHz to 130 kHz

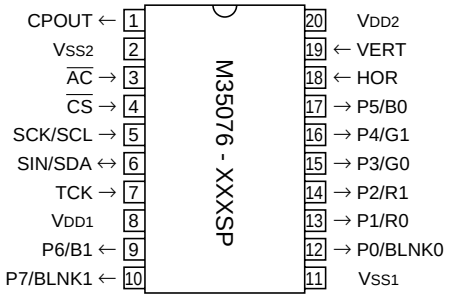
<VDD=3V>

- Display input frequency range
  External clock mode 1 ..... F_{OSC} = 6.3 MHz to 40 MHz
- Horizontal synchronous input frequency
  ..... H.sync = 15 kHz to 60 kHz

APPLICATION

Digital camera, Digital video, Digital television, CRT display, Liquid crystal display, Plasma display

PIN CONFIGURATION (TOP VIEW)



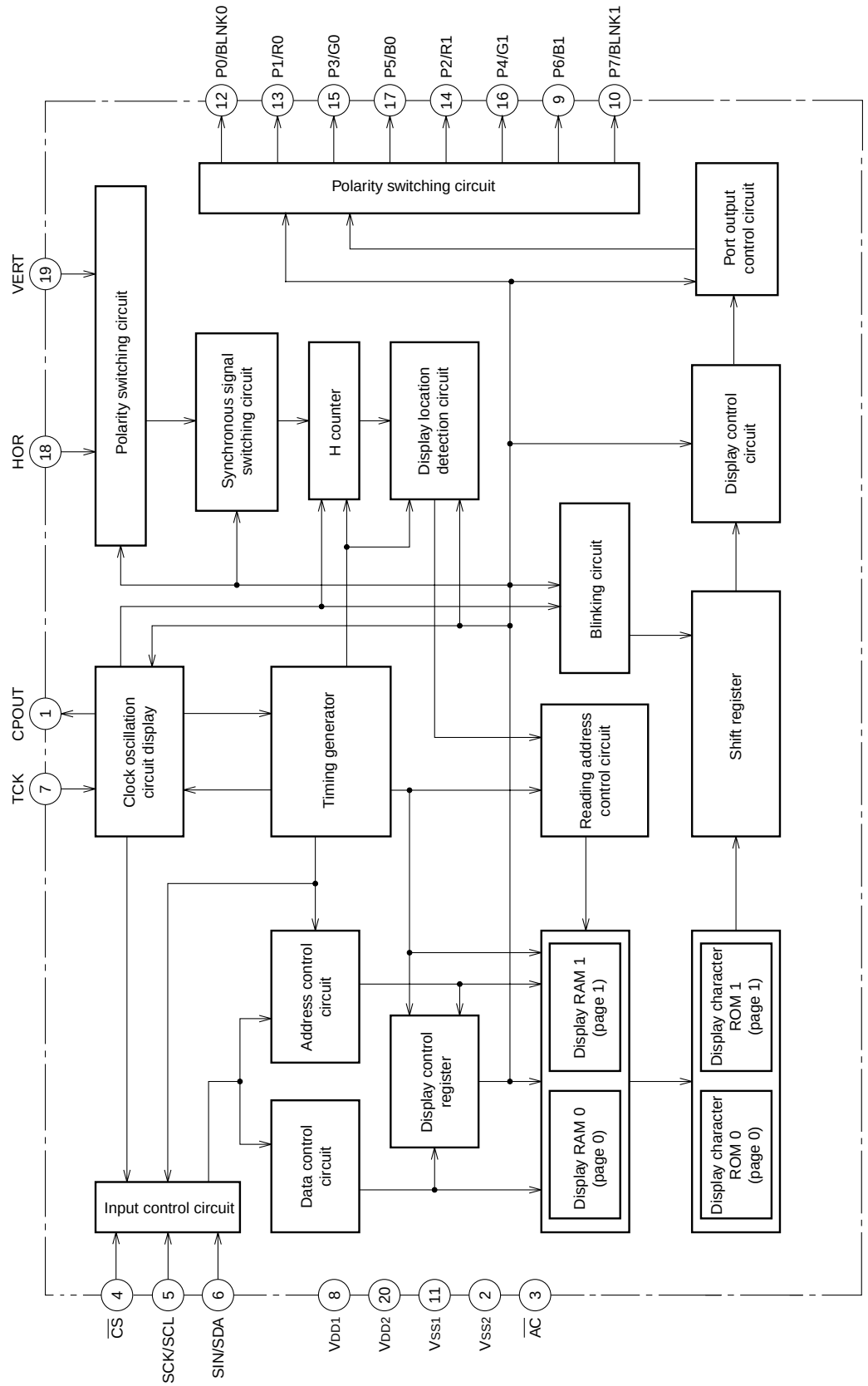
Outline 20P4B

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input/ Output	Function
1	CPOUT	Filter output	Output	Filter output. Connect loop filter to this pin.
2	V_{SS2}	Earthing pin	–	Connect to GND.
3	$\overline{AC}$	Auto-clear input	Input	When “L”, this pin resets the internal IC circuit. Hysteresis input. Built-in pull-up resistor.
4	$\overline{CS}$	Chip select input	Input	<at the 16-bit serial communication> Chip select pin. Set this pin to "L" level at serial data transfer. Hysteresis input. Built-in pull-up resistor.
				<at the I²C-BUS serial communication> Set this pin to “H” level.
5	SCK/SCL	Clock input	Input	<at the 16-bit serial communication> SIN pin serial data is taken in when SCK rises at $\overline{CS}$ pin "L" level. Hysteresis input.
				<at the I²C-BUS serial communication> SDA pin serial data is taken in synchronized with SCL.
6	SIN/SDA	Data input	Input	<at the 16-bit serial communication> This is the pin for serial input of display control register and display RAM data. Hysteresis input.
		Data I/O	I/O	<at the I²C-BUS serial communication> Hysteresis input. This is the pin for serial input of display control register and display RAM data. Also this pin output acknowledge signal.
7	TCK	External clock	Input	This is the pin for external clock input.
8	V_{DD1}	Power pin	–	Please connect to +5V with the power pin.
9	P6/B1	Port P6 output	Output	This pin can be toggled between port pin output and B1 signal output.
10	P7/BLNK1	Port P7 output	Output	This pin can be toggled between port pin output and BLNK1 signal output.
11	V_{SS1}	Earthing pin	–	Please connect to GND using circuit earthing pin.
12	P0/BLNK0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
13	P1/R0	Port P1 output	Output	This pin can be toggled between port pin output and R0 signal output.
14	P2/R1	Port P2 output	Output	This pin can be toggled between port pin output and R1 signal output.
15	P3/G0	Port P3 output	Output	This pin can be toggled between port pin output and G0 signal output.
16	P4/G1	Port P4 output	Output	This pin can be toggled between port pin output and G1 signal output.
17	P5/B0	Port P5 output	Output	This pin can be toggled between port pin output and B0 signal output.
18	HOR	Horizontal synchro-nous signal input	Input	This pin inputs the horizontal synchronous signal. Hysteresis input.
19	VERT	Vertical synchro-nous signal input	Input	This pin inputs the vertical synchronous signal. Hysteresis input.
20	V_{DD2}	Power pin	–	Please connect to +5V with the power pin.

BLOCK DIAGRAM



MEMORY CONSTITUTION

Address 000_{16} to $11F_{16}$ are assigned to the display RAM, address 120_{16} to 128_{16} are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120_{16} to 128_{16}) are set to "0" when the $\overline{AC}$ pin level is "L". And then, RAM is not erased and be undefinited. This memory is consisted of 2 pages : page 0 memory and page 1 memory (their addresses are common), page controlled by DAF bit of each address when writing data. For detail, see "Data input". Memory constitution is shown in Figure 1 and 2.

Addresses	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000_{16}	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
001_{16}	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blink-ing	Character color			Character code							
$11E_{16}$	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
$11F_{16}$	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
120_{16}	0	EXCK0	DISV2	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
121_{16}	0	RSEL0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
122_{16}	0	RSEL1	SPACE2	SPACE1	SPACE0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123_{16}	0	EXCK1	TEST3	TEST2	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
124_{16}	0	TEST9	PTC67	TEST4	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
125_{16}	0	TEST10	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
126_{16}	0	POPUP	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
127_{16}	0	MODE0	TEST12	HSZ20	TEST11	HSZ10	BETA14	TEST8	TEST7	TEST6	FB	FG	FR	RB	RG	RR
128_{16}	0	MODE1	BLINK2	BLINK1	BLINK0	DSPON	STOP	RAMERS	SYAD	BLK1	BLK0	POLH	POLV	VMASK	B/$\overline{F}$	BCOL

Fig. 1 Memory constitution (page 0 memory)

Addresses	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000_{16}	1	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
001_{16}	1	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blink-ing	Character color			Character code							
$11E_{16}$	1	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
$11F_{16}$	1	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0
120_{16}	1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
121_{16}	1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
122_{16}	1	–	SPACE2	SPACE1	SPACE0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123_{16}	1	–	TEST3	VJT	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
124_{16}	1	–	–	TEST4	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
125_{16}	1	–	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
126_{16}	1	–	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V18SZ1	V18SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
127_{16}	1	–	TEST12	HSZ20	TEST11	HSZ10	BETA14	TEST8	TEST7	TEST6	FB	FG	FR	RB	RG	RR
128_{16}	1	–	BLINK2	BLINK1	BLINK0	DSPON	TEST13	RAMERS	SYAD	BLK1	BLK0	–	–	–	–	BCOL

Fig. 2 Memory constitution (page 1 memory)

Note: Page 0 and page 1 registers are found in their respective pages. For example, HP10 to HP0 of the page 0 memory sets the horizontal display start position of page 0, whereas HP10 to HP0 (same register name) of the page 1 memory sets the horizontal display start position of page 1. Also, registers common to both page 0 and page 1 are found only in the page 0 memory. For example, PTC0 is the control register of the P0 pin and is found only in the page 0 memory.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM (page 0 and page 1 are common). The screen constitution is shown in Figure 3.

Row / Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000_{16}	001_{16}	002_{16}	003_{16}	004_{16}	005_{16}	006_{16}	007_{16}	008_{16}	009_{16}	$00A_{16}$	$00B_{16}$	$00C_{16}$	$00D_{16}$	$00E_{16}$	$00F_{16}$	010_{16}	011_{16}	012_{16}	013_{16}	014_{16}	015_{16}	016_{16}	017_{16}
2	018_{16}	019_{16}	$01A_{16}$	$01B_{16}$	$01C_{16}$	$01D_{16}$	$01E_{16}$	$01F_{16}$	020_{16}	021_{16}	022_{16}	023_{16}	024_{16}	025_{16}	026_{16}	027_{16}	028_{16}	029_{16}	$02A_{16}$	$02B_{16}$	$02C_{16}$	$02D_{16}$	$02E_{16}$	$02F_{16}$
3	030_{16}	031_{16}	032_{16}	033_{16}	034_{16}	035_{16}	036_{16}	037_{16}	038_{16}	039_{16}	$03A_{16}$	$03B_{16}$	$03C_{16}$	$03D_{16}$	$03E_{16}$	$03F_{16}$	040_{16}	041_{16}	042_{16}	043_{16}	044_{16}	045_{16}	046_{16}	047_{16}
4	048_{16}	049_{16}	$04A_{16}$	$04B_{16}$	$04C_{16}$	$04D_{16}$	$04E_{16}$	$04F_{16}$	050_{16}	051_{16}	052_{16}	053_{16}	054_{16}	055_{16}	056_{16}	057_{16}	058_{16}	059_{16}	$05A_{16}$	$05B_{16}$	$05C_{16}$	$05D_{16}$	$05E_{16}$	$05F_{16}$
5	060_{16}	061_{16}	062_{16}	063_{16}	064_{16}	065_{16}	066_{16}	067_{16}	068_{16}	069_{16}	$06A_{16}$	$06B_{16}$	$06C_{16}$	$06D_{16}$	$06E_{16}$	$06F_{16}$	070_{16}	071_{16}	072_{16}	073_{16}	074_{16}	075_{16}	076_{16}	077_{16}
6	078_{16}	079_{16}	$07A_{16}$	$07B_{16}$	$07C_{16}$	$07D_{16}$	$07E_{16}$	$07F_{16}$	080_{16}	081_{16}	082_{16}	083_{16}	084_{16}	085_{16}	086_{16}	087_{16}	088_{16}	089_{16}	$08A_{16}$	$08B_{16}$	$08C_{16}$	$08D_{16}$	$08E_{16}$	$08F_{16}$
7	090_{16}	091_{16}	092_{16}	093_{16}	094_{16}	095_{16}	096_{16}	097_{16}	098_{16}	099_{16}	$09A_{16}$	$09B_{16}$	$09C_{16}$	$09D_{16}$	$09E_{16}$	$09F_{16}$	$0A0_{16}$	$0A1_{16}$	$0A2_{16}$	$0A3_{16}$	$0A4_{16}$	$0A5_{16}$	$0A6_{16}$	$0A7_{16}$
8	$0A8_{16}$	$0A9_{16}$	$0AA_{16}$	$0AB_{16}$	$0AC_{16}$	$0AD_{16}$	$0AE_{16}$	$0AF_{16}$	$0B0_{16}$	$0B1_{16}$	$0B2_{16}$	$0B3_{16}$	$0B4_{16}$	$0B5_{16}$	$0B6_{16}$	$0B7_{16}$	$0B8_{16}$	$0B9_{16}$	$0BA_{16}$	$0BB_{16}$	$0BC_{16}$	$0BD_{16}$	$0BE_{16}$	$0BF_{16}$
9	$0C0_{16}$	$0C1_{16}$	$0C2_{16}$	$0C3_{16}$	$0C4_{16}$	$0C5_{16}$	$0C6_{16}$	$0C7_{16}$	$0C8_{16}$	$0C9_{16}$	$0CA_{16}$	$0CB_{16}$	$0CC_{16}$	$0CD_{16}$	$0CE_{16}$	$0CF_{16}$	$0D0_{16}$	$0D1_{16}$	$0D2_{16}$	$0D3_{16}$	$0D4_{16}$	$0D5_{16}$	$0D6_{16}$	$0D7_{16}$
10	$0D8_{16}$	$0D9_{16}$	$0DA_{16}$	$0DB_{16}$	$0DC_{16}$	$0DD_{16}$	$0DE_{16}$	$0DF_{16}$	$0E0_{16}$	$0E1_{16}$	$0E2_{16}$	$0E3_{16}$	$0E4_{16}$	$0E5_{16}$	$0E6_{16}$	$0E7_{16}$	$0E8_{16}$	$0E9_{16}$	$0EA_{16}$	$0EB_{16}$	$0EC_{16}$	$0ED_{16}$	$0EE_{16}$	$0EF_{16}$
11	$0F0_{16}$	$0F1_{16}$	$0F2_{16}$	$0F3_{16}$	$0F4_{16}$	$0F5_{16}$	$0F6_{16}$	$0F7_{16}$	$0F8_{16}$	$0F9_{16}$	$0FA_{16}$	$0FB_{16}$	$0FC_{16}$	$0FD_{16}$	$0FE_{16}$	$0FF_{16}$	100_{16}	101_{16}	102_{16}	103_{16}	104_{16}	105_{16}	106_{16}	107_{16}
12	108_{16}	109_{16}	$10A_{16}$	$10B_{16}$	$10C_{16}$	$10D_{16}$	$10E_{16}$	$10F_{16}$	110_{16}	111_{16}	112_{16}	113_{16}	114_{16}	115_{16}	116_{16}	117_{16}	118_{16}	119_{16}	$11A_{16}$	$11B_{16}$	$11C_{16}$	$11D_{16}$	$11E_{16}$	$11F_{16}$

* The hexadecimal numbers in the boxes show the display RAM address.

Fig. 3 Screen constitution

DISPLAY RAM

Address 000_{16} to $11F_{16}$

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>C0</td><td>0
1</td><td rowspan="8">Set the displayed ROM character code.

To write data into page 0 (Note 2), select the data from the ROM characters (256 types) for page 0 and set the character code. To write data into page 1, do the same from the ROM characters (256 types) for page 1.</td><td rowspan="8">Set display character</td></tr>
<tr><td>1</td><td>C1</td><td>0
1</td></tr>
<tr><td>2</td><td>C2</td><td>0
1</td></tr>
<tr><td>3</td><td>C3</td><td>0
1</td></tr>
<tr><td>4</td><td>C4</td><td>0
1</td></tr>
<tr><td>5</td><td>C5</td><td>0
1</td></tr>
<tr><td>6</td><td>C6</td><td>0
1</td></tr>
<tr><td>7</td><td>C7</td><td>0
1</td></tr>
<tr><td>8</td><td>R</td><td>0
1</td><td rowspan="4"><table><tr><th>B</th><th>G</th><th>R</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="4">Set character color (character unit)</td></tr>
<tr><td>9</td><td>G</td><td>0
1</td></tr>
<tr><td>A</td><td>B</td><td>0
1</td></tr>
<tr><td>B</td><td>BLINK</td><td>0
1</td><td>Do not blink.
Blinking</td><td>Set blinking
See register BLINK2 to BLINK0 (address128_{16})</td></tr>
<tr><td>C</td><td>BR</td><td>0
1</td><td rowspan="4"><table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table></td><td rowspan="4">Set character background (character unit)</td></tr>
<tr><td>D</td><td>BG</td><td>0
1</td></tr>
<tr><td>E</td><td>BB</td><td>0
1</td></tr>
</table>

Notes 1. The display RAM is undefined state at the $\overline{AC}$ pin.

2. The display RAM consists of 2 pages, page 0 and page 1 (common address). The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.

REGISTERS DESCRIPTION

(1) Address 120_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DIV0
(Note 3)</td><td>⓪
1</td><td rowspan="10">Set division value (multiply value) of horizontal oscillation frequency.

$N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$

N1 : division value (multiply value)</td><td rowspan="10">Set display frequency by division value (multiply value) setting.
For details, see REGISTER SUPPLEMENTARY DESCRIPTION (1).

Also, set the display frequency range by registers DIVS0, DIVS1(address 120_{16}), RSEL0(address 121_{16}) and RSEL1(address 122_{16}) in accordance with the display frequency.

Any of this settings above is required only when EXCK1 = 0, EXCK0 = 1 and EXCK1 = 1, EXCK0 = 1.</td></tr>
<tr><td>1</td><td>DIV1
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>2</td><td>DIV2
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>3</td><td>DIV3
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>4</td><td>DIV4
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>5</td><td>DIV5
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>6</td><td>DIV6
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>7</td><td>DIV7
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>8</td><td>DIV8
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>9</td><td>DIV9
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>A</td><td>DIV10
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>B</td><td>DIVS0
(Note 3)</td><td>⓪
1</td><td rowspan="3">For setting, see REGISTER SUPPLEMENTARY DESCRIPTION (2).</td><td rowspan="3">Set display frequency range.</td></tr>
<tr><td>C</td><td>DIVS1
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>D</td><td>DISV2
(Note 3)</td><td>⓪
1</td></tr>
<tr><td>E</td><td>EXCK0
(Note 3)</td><td>⓪
1</td><td>
<table>
<tr><th>EXCK1</th><th>EXCK0</th><th>Display clock input</th></tr>
<tr><td>0</td><td>0</td><td>External clock mode 1</td></tr>
<tr><td>0</td><td>1</td><td>Internal clock mode</td></tr>
<tr><td>1</td><td>0</td><td>Do not set</td></tr>
<tr><td>1</td><td>1</td><td>External clock mode 2</td></tr>
</table>
</td><td>Display clock setting
See REGISTER SUPPLEMENTARY DESCRIPTION (1)
EXCK1 : address123_{16}</td></tr>
</table>

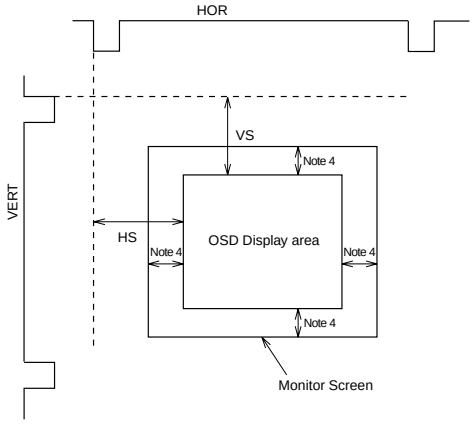
Notes 1. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

(2) Address 121_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0 (Note 3)	⓪	P0 output (port P0).	P0 pin output control.
		1	BLNK0 output.	
1	PTC1 (Note 3)	⓪	P1 output (port P1).	P1 pin output control.
		1	R0 signal output.	
2	PTC2 (Note 3)	⓪	P2 output (port P2).	P2 pin output control.
		1	R1 signal output.	
3	PTC3 (Note 3)	⓪	P3 output (port P3).	P3 pin output control.
		1	G0 signal output.	
4	PTC4 (Note 3)	⓪	P4 output (port P4).	P4 pin output control.
		1	G1 signal output.	
5	PTC5 (Note 3)	⓪	P5 output (port P5).	P5 pin output control.
		1	B0 signal output.	
6	PTD0 (Note 3)	⓪	“L” output or negative polarity output (BLNK0 output).	P0 pin data control.
		1	“H” output or positive polarity output (BLNK0 output).	
7	PTD1 (Note 3)	⓪	“L” output or negative polarity output (R0 signal output).	P1 pin data control.
		1	“H” output or positive polarity output (R0 signal output).	
8	PTD2 (Note 3)	⓪	“L” output or negative polarity output (R1 signal output).	P2 pin data control.
		1	“H” output or positive polarity output (R1 signal output).	
9	PTD3 (Note 3)	⓪	“L” output or negative polarity output (G0 signal output).	P3 pin data control.
		1	“H” output or positive polarity output (G0 signal output).	
A	PTD4 (Note 3)	⓪	“L” output or negative polarity output (G1 signal output).	P4 pin data control.
		1	“H” output or positive polarity output (G1 signal output).	
B	PTD5 (Note 3)	⓪	“L” output or negative polarity output (B0 signal output).	P5 pin data control.
		1	“H” output or positive polarity output (B0 signal output).	
C	PTD6 (Note 3)	⓪	“L” output or negative polarity output (B1 signal output).	P6 pin data control.
		1	“H” output or positive polarity output (B1 signal output).	
D	PTD7 (Note 3)	⓪	“L” output or negative polarity output (BLNK1 signal output).	P7 pin data control.
		1	“H” output or positive polarity output (BLNK1 signal output).	
E	RSEL0 (Note 3)	⓪	For setting, see REGISTER SUPPLYMENTARY DESCRIPTION (2).	Set display frequency range.
		1		

Notes 1. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

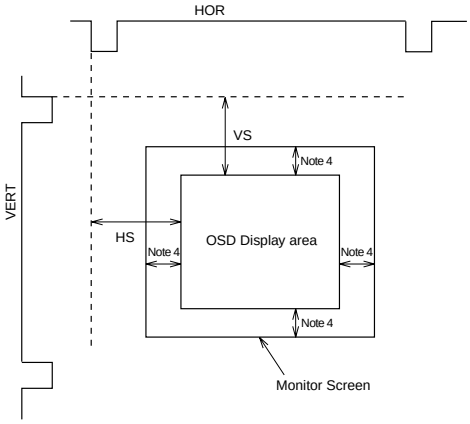
(3) Address 122_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>HP0</td><td>⓪
1</td><td rowspan="11">If HS is the horizontal display start location,
$HS = T \times (\sum_{n=0}^{10} 2^n HP_n + 6)$
T : Period of display frequency
2007 settings are possible.
 
</td><td rowspan="11">Horizontal display start location is specified using the 11 bits from HP10 to HP0.
HP10 to HP0 = (00000000000_2) and (00000100111_2) setting is forbidden.

HS* (shown left) shows horizontal display start location that is register B/$\overline{F}$ (address 128_{16}) = 0 is set.</td></tr>
<tr><td>1</td><td>HP1</td><td>⓪
1</td></tr>
<tr><td>2</td><td>HP2</td><td>⓪
1</td></tr>
<tr><td>3</td><td>HP3</td><td>⓪
1</td></tr>
<tr><td>4</td><td>HP4</td><td>⓪
1</td></tr>
<tr><td>5</td><td>HP5</td><td>⓪
1</td></tr>
<tr><td>6</td><td>HP6</td><td>⓪
1</td></tr>
<tr><td>7</td><td>HP7</td><td>⓪
1</td></tr>
<tr><td>8</td><td>HP8</td><td>⓪
1</td></tr>
<tr><td>9</td><td>HP9</td><td>⓪
1</td></tr>
<tr><td>A</td><td>HP10</td><td>⓪
1</td></tr>
<tr><td>B</td><td>SPACE0</td><td>⓪
1</td><td rowspan="2">SPACE 2 1 0 | Number of Lines and Space <(S) represents space>
0 0 0 | 12
0 0 1 | 1 (S) 10 (S) 1
0 1 0 | 2 (S) 8 (S) 2
0 1 1 | 3 (S) 6 (S) 3
1 0 0 | 4 (S) 4 (S) 4
1 0 1 | 5 (S) 2 (S) 5
1 1 0 | 6 (S) 6
1 1 1 | 6 (S)(S) 6
(S) represents one line worth of spac</td><td rowspan="2">Leave one line worth of space in the vertical direction.
For example, 6 (S) 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7.
A line is 18 × N horizontal scan lines.
N is determined by the character size in the vertical direction</td></tr>
<tr><td>C</td><td>SPACE1</td><td>⓪
1</td></tr>
<tr><td>D</td><td>SPACE2</td><td>⓪
1</td></tr>
<tr><td>E</td><td>RSEL1
(Note 3)</td><td>⓪
1</td><td>For setting, see REGISTER SUPPLEMENTARY DESCRIPTION (2).</td><td>Set display frequency range.</td></tr>
</table>

Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".
4. Set up the horizontal and vertical display start location so that display range may not exceed it.
Set the character code "FF_{16}" (blank without background) for the display RAM of the part which the display range exceeds.

(4) Address 123_{16}

DA	Register	Contents		Remarks
		Status	Function	
0	VP0	⓪	If VS is the vertical display start location, $VS = H \times \sum_{n=0}^{9} 2^n VP_n$ H: Cycle with the horizontal synchronizing pulse 1023 settings are possible.  	The vertical start location is specified using the 10 bits from VP9 to VP0. VP9 to VP0 = (0000000000_2) setting is forbidden. HS* (shown left) shows horizontal display start location that is register B/F (address 128_{16}) = 0 is set.
		1		
1	VP1	⓪		
		1		
2	VP2	⓪		
		1		
3	VP3	⓪		
		1		
4	VP4	⓪		
		1		
5	VP5	⓪		
		1		
6	VP6	⓪		
		1		
7	VP7	⓪		
		1		
8	VP8	⓪		
		1		
9	VP9	⓪		
		1		
A	TEST0	⓪	It should be fixed to “0”.	
		1	Can not be used.	
B	TEST1	⓪	It should be fixed to “0”.	
		1	Can not be used.	
C	VJT	⓪	It should be fixed to “0”.	
		1	Can not be used.	
D	TEST3	⓪	It should be fixed to “0”.	
		1	Can not be used.	
E	EXCK1 (Note 3)	⓪	For setting, see Register EXCK0 (address 120_{16}).	Display clock setting
		1		

Notes 1. The mark ○ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".
4. Set up the horizontal and vertical display start location so that display range may not exceed it.
Set the character code "FF_{16}" (blank without background) for the display RAM of the part which the display range exceeds.

(5) Address 124_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>DSP0</td><td>⓪</td><td rowspan="13">The display mode (blanking mode) for line n on the display screen is set line-by-line, using DSPn (n = 0 to 11).

The display mode is determined by the combination of registers BLK1 and BLK0 (address 128_{16}). Settings are given below.

<table><tr><th>BLK1</th><th>BLK0</th><th>DSPn= “0”</th><th>DSPn= “1”</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline border</td><td>Matrix-outline</td></tr><tr><td>0</td><td>1</td><td>Character</td><td>Border</td></tr><tr><td>1</td><td>0</td><td>Border</td><td>Matrix-outline</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline</td><td>Character</td></tr></table>(At register BCOL = “0”)

For detail, see DISPLAY FORM1(1).</td><td>Sets the display mode of line 1.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>1</td><td>DSP1</td><td>⓪</td><td>Sets the display mode of line 2.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>2</td><td>DSP2</td><td>⓪</td><td>Sets the display mode of line 3.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>3</td><td>DSP3</td><td>⓪</td><td>Sets the display mode of line 4.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>4</td><td>DSP4</td><td>⓪</td><td>Sets the display mode of line 5.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>5</td><td>DSP5</td><td>⓪</td><td>Sets the display mode of line 6.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>6</td><td>DSP6</td><td>⓪</td><td>Sets the display mode of line 7.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>7</td><td>DSP7</td><td>⓪</td><td>Sets the display mode of line 8.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>8</td><td>DSP8</td><td>⓪</td><td>Sets the display mode of line 9.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>9</td><td>DSP9</td><td>⓪</td><td>Sets the display mode of line 10.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>A</td><td>DSP10</td><td>⓪</td><td>Sets the display mode of line 11.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>B</td><td>DSP11</td><td>⓪</td><td>Sets the display mode of line 12.</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>C</td><td>TEST4</td><td>⓪</td><td>It should be fixed to “0”.</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
<tr><td>D</td><td>PTC67
(Note 3)</td><td>⓪</td><td>P6 output (port P6) and P7 output (port P7).</td><td rowspan="2">P6 pin and P7 pin output control.</td></tr>
<tr><td></td><td></td><td>1</td><td>B1 output and BLNK output.</td></tr>
<tr><td>E</td><td>TEST9
(Note 3)</td><td>⓪</td><td>Set to “0” in internal clock mode.</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Set to “1” in external clock mode.</td><td></td></tr>
</table>

Notes 1. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

(6) Address 125_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>LIN2</td><td>⓪
1</td><td rowspan="9">The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17).

Dot size can be selected between 2 types for each dot line.

For dot size, see the below registers. Line 1 and lines 2 to 12 can be set independent of one another.

<table><tr><th></th><th>LINn = “0”</th><th>LINn = “1”</th></tr><tr><td>1st line</td><td>Refer to VSZ1L0 and VSZ1L1</td><td>Refer to VSZ1H0 and VSZ1H1</td></tr><tr><td>2nd to 12th line</td><td>Refer to VSZ2L0 and VSZ2L1</td><td>Refer to VSZ2H0 and VSZ2H1</td></tr></table></td><td>Character size setting in the vertical direction for the 2nd line.</td></tr>
<tr><td>1</td><td>LIN3</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 3rd line.</td></tr>
<tr><td>2</td><td>LIN4</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 4th line.</td></tr>
<tr><td>3</td><td>LIN5</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 5th line.</td></tr>
<tr><td>4</td><td>LIN6</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 6th line.</td></tr>
<tr><td>5</td><td>LIN7</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 7th line.</td></tr>
<tr><td>6</td><td>LIN8</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 8th line.</td></tr>
<tr><td>7</td><td>LIN9</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 9th line.</td></tr>
<tr><td>8</td><td>V1SZ0</td><td>⓪
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V1SZ1</th><th>V1SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the 1st line.
(display monitor 1 to 12 line)</td></tr>
<tr><td>9</td><td>V1SZ1</td><td>⓪
1</td></tr>
<tr><td>A</td><td>VSZ1L0</td><td>⓪
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ1L1</th><th>VSZ1L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor 1 line) at “0” state in register LIN2 to LIN17 (address 125_{16}, 126_{16}).</td></tr>
<tr><td>B</td><td>VSZ1L1</td><td>⓪
1</td></tr>
<tr><td>C</td><td>VSZ1H0</td><td>⓪
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ1H1</th><th>VSZ1H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor 1 line) at “1” state in register LIN2 to LIN17 (address 125_{16}, 126_{16}).</td></tr>
<tr><td>D</td><td>VSZ1H1</td><td>⓪
1</td></tr>
<tr><td>E</td><td>TEST10
(Note 3)</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
</table>

Notes 1. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

(7) Address 126_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>LIN10</td><td>⓪
1</td><td rowspan="8">The vertical dot size for line n in the character dot lines (18 vertical lines) is set using LINn (n = 2 to 17).

Dot size can be selected between 2 types for each dot line.

For dot size, see the below registers. Line 1 and lines 2 to 12 can be set independent of one another.

<table><tr><th></th><th>LINn = “0”</th><th>LINn = “1”</th></tr><tr><td>1st line</td><td>Refer to VSZ1L0 and VSZ1L1</td><td>Refer to VSZ1H0 and VSZ1H1</td></tr><tr><td>2nd to 12th line</td><td>Refer to VSZ2L0 and VSZ2L1</td><td>Refer to VSZ2H0 and VSZ2H1</td></tr></table></td><td>Character size setting in the vertical direction for the 10th line.</td></tr>
<tr><td>1</td><td>LIN11</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 11th line.</td></tr>
<tr><td>2</td><td>LIN12</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 12th line.</td></tr>
<tr><td>3</td><td>LIN13</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 13th line.</td></tr>
<tr><td>4</td><td>LIN14</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 14th line.</td></tr>
<tr><td>5</td><td>LIN15</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 15th line.</td></tr>
<tr><td>6</td><td>LIN16</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 16th line.</td></tr>
<tr><td>7</td><td>LIN17</td><td>⓪
1</td><td>Character size setting in the vertical direction for the 17th line.</td></tr>
<tr><td>8</td><td>V18SZ0</td><td>⓪
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>V18SZ1</th><th>V18SZ0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction for the 18th line.
(display monitor 1 to 12 line)</td></tr>
<tr><td>9</td><td>V18SZ1</td><td>⓪
1</td></tr>
<tr><td>A</td><td>VSZ2L0</td><td>⓪
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2L1</th><th>VSZ2L0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor for 2 to 12 line) at “0” state in register LIN2 to LIN17 (address 125_{16}, 126_{16}).</td></tr>
<tr><td>B</td><td>VSZ2L1</td><td>⓪
1</td></tr>
<tr><td>C</td><td>VSZ2H0</td><td>⓪
1</td><td rowspan="2">H: Cycle with the horizontal synchronizing pulse
<table><tr><th>VSZ2H1</th><th>VSZ2H0</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table></td><td rowspan="2">Character size setting in the vertical direction (display monitor for 2 to 12 line) at “0” state in register LIN2 to LIN17 (address 125_{16}, 126_{16}).</td></tr>
<tr><td>D</td><td>VSZ2H1</td><td>⓪
1</td></tr>
<tr><td>E</td><td>POPUP
(Note 3)</td><td>⓪
1</td><td>Page 1 priority display
Page 0 priority display</td><td>Sets the priority page for when 2 pages are displayed at the same time. The setting is effective only when the standard display mode is set as MODE0 = "0" , MODE1 = "0". See "DISPLAY FORM 2" .</td></tr>
</table>

Notes 1. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

(8) Address 127_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td>0</td><td>RR</td><td>⓪
1</td><td>
<table>
<tr><th>RB</th><th>RG</th><th>RR</th><th>Color</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>White</td></tr>
</table>
</td><td>Sets the raster color of all blankings.</td></tr>
<tr><td>1</td><td>RG</td><td>⓪
1</td><td></td><td></td></tr>
<tr><td>2</td><td>RB</td><td>⓪
1</td><td></td><td></td></tr>
<tr><td>3</td><td>FR</td><td>⓪
1</td><td>
<table>
<tr><th>FB</th><th>FG</th><th>FR</th><th>Color</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>White</td></tr>
</table>
</td><td>Sets the blanking color of the Border size, or the shadow size.</td></tr>
<tr><td>4</td><td>FG</td><td>⓪
1</td><td></td><td></td></tr>
<tr><td>5</td><td>FB</td><td>⓪
1</td><td></td><td></td></tr>
<tr><td>6</td><td>TEST6</td><td>⓪</td><td>It should be fixed to “0”.</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
<tr><td>7</td><td>TEST7</td><td>⓪</td><td>It should be fixed to “0”.</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
<tr><td>8</td><td>TEST8</td><td>⓪</td><td>It should be fixed to “0”.</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
<tr><td>9</td><td>BETA14</td><td>⓪</td><td>Matrix-outline display (12 × 18 dot)</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Matrix-outline display (14 × 18 dot)</td><td></td></tr>
<tr><td>A</td><td>HSZ10</td><td>⓪
1</td><td>
<table>
<tr><th>HSZ10</th><th>Horizontal direction size</th></tr>
<tr><td>0</td><td>1T/dot</td></tr>
<tr><td>1</td><td>2T/dot</td></tr>
</table>
</td><td>Character size setting in the horizontal direction for the first line.
T : Display frequency cycle</td></tr>
<tr><td>B</td><td>TEST11</td><td>⓪</td><td>It should be fixed to “0”.</td><td></td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td><td></td></tr>
<tr><td>C</td><td>HSZ20</td><td>⓪
1</td><td>
<table>
<tr><th>HSZ20</th><th>Horizontal direction size</th></tr>
<tr><td>0</td><td>1T/dot</td></tr>
<tr><td>1</td><td>2T/dot</td></tr>
</table>
</td><td></td></tr>
<tr><td>D</td><td>TEST12</td><td>⓪</td><td>It should be fixed to “0”.</td><td rowspan="2">Character size setting in the horizontal direction for the 2nd line to 12th line.
T : Display frequency cycle</td></tr>
<tr><td></td><td></td><td>1</td><td>Can not be used.</td></tr>
<tr><td>E</td><td>MODE0
(Note 3)</td><td>⓪
1</td><td>
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Output system</th><th>Display mode</th></tr>
<tr><td>0</td><td>0</td><td>1 system</td><td>Standard.(Note4)</td></tr>
<tr><td>0</td><td>1</td><td>1 system</td><td>AND</td></tr>
<tr><td>1</td><td>0</td><td>2 system</td><td>—</td></tr>
<tr><td>1</td><td>1</td><td>1 system</td><td>OR</td></tr>
</table>
</td><td>Sets the RGB signal output system and the display mode for when 2 pages are displayed at the same time.
See “DISPLAY FORM 2”.
MODE1(address128_{16}) .</td></tr>
</table>

Notes 1. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".
4. 2 way settings are available by POPUP (address 126_{16}).

(9) Address 128_{16}

<table>
<tr><th rowspan="2">DA</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remarks</th></tr>
<tr><th>Status</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BCOL</td><td>⓪</td><td>Blanking of BLK0, BLK1</td><td rowspan="2">Sets all raster blanking</td></tr>
<tr><td>1</td><td>All raster blanking</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">B/$\overline{F}$
(Note 3)</td><td>⓪</td><td>Synchronize with the leading edge of horizontal synchronization.</td><td rowspan="2">Synchronize with the front porch or back porch of the horizontal synchronazation signal.</td></tr>
<tr><td>1</td><td>Synchronize with the trailing edge of horizontal synchronization.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">VMASK
(Note 3)</td><td>⓪</td><td>Do not mask by VERT input signal</td><td rowspan="2">Set mask at phase comparison operating.</td></tr>
<tr><td>1</td><td>Mask by VERT input signal</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">POLV
(Note 3)</td><td>⓪</td><td>VERT pin is negative polarity</td><td rowspan="2">Set VERT pin polarity.</td></tr>
<tr><td>1</td><td>VERT pin is positive polarity</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">POLH
(Note 3)</td><td>⓪</td><td>HOR pin is negative polarity</td><td rowspan="2">Set HOR pin polarity.</td></tr>
<tr><td>1</td><td>HOR pin is positive polarity</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BLK0</td><td>⓪</td><td rowspan="3"><table><tr><th>BLK1</th><th>BLK0</th><th>Blanking mode</th></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table>(When DSPn (address 124_{16}) = “0”)</td><td rowspan="3">Set blanking mode.
See “DISPLAY SHAPE 2”.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BLK1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">SYAD</td><td>⓪</td><td>Border display of character</td><td rowspan="2">See “DISPLAY FORM1 (2)”.</td></tr>
<tr><td>1</td><td>Shadow display of character</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">RAMERS</td><td>⓪</td><td>RAM not erased</td><td rowspan="2">When register RAMERS is set to “1”,do not stop the display clock. There is no need to reset because there is no register for this bit.</td></tr>
<tr><td>1</td><td>RAM erased</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">STOP</td><td>⓪</td><td>Oscillation of clock for display</td><td rowspan="2">It is a test bit (TEST13) in the page 1 register, therefore fix it to “0”.</td></tr>
<tr><td>1</td><td>Stop the oscillation of clock for display</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">DSPON</td><td>⓪</td><td>Display OFF</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display ON</td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">BLINK0</td><td>⓪</td><td rowspan="3"><table><tr><th colspan="2">BLINK</th><th rowspan="2">Duty</th></tr><tr><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>Blinking OFF</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table></td><td rowspan="3">Set blinking duty ratio.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">BLINK1</td><td>⓪</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">D</td><td rowspan="2">BLINK2</td><td>⓪</td><td>Divided into 64 of vertical synchronous signal</td><td rowspan="2">Set blinking frequency.</td></tr>
<tr><td>1</td><td>Divided into 32 of vertical synchronous signal</td></tr>
<tr><td rowspan="2">E</td><td rowspan="2">MODE1
(Note 3)</td><td>⓪</td><td rowspan="2">For setting, see MODE0 (address 127_{16}).</td><td rowspan="2">Sets the RGB signal output system and the display mode for when 2 pages are displayed at the same time.</td></tr>
<tr><td>1</td></tr>
</table>

Notes 1. The mark ◯ around the status value means the reset status by the "L" level is input to $\overline{AC}$ pin.
2. The page in which data is written is controlled by the DAF bit. When set to "0", data is written into page 0, whereas when set to "1", data is written into page 1.
3. Registers marked with (Note 3) are found only in page 0, therefore the register value does not change when the DAF bit is set to "1".

REGISTER SUPPLEMENTARY DESCRIPTION

(1) Setting external clock input and display frequency mode

Setting external clock input and display frequency mode (by use of EXCK0 (120_{16}), EXCK1 (123_{16}) and DIV10 to DIV0 (120_{16}), as explained here following.

(a) When (EXCK1, EXCK0) = (0, 0) .....External clock mode 1

Fosc = 6.3 to 80 MHz (V_{DD} = 4.75 to 5.25 V)

Fosc = 6.3 to 40 MHz (V_{DD} = 2.50 to 3.50 V)

Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant period continuous horizontal synchronous signal.

Never stop inputting the clock while displaying.

Do not have to set a display frequency because the clock just as it is entered from outside is used as the display clock.

(b) When (EXCK1, EXCK0) = (0, 1) .....Internal clock mode

Fosc = 20 to 110 MHz (V_{DD} = 4.75 to 5.25 V)

Clock input from the TCK pin is unnecessary. The multiply clock of the internally generated horizontal synchronous signal is used as the display clock.

The display frequency is set by setting the multiply value of the horizontal synchronous frequency (of the display frequency) in DIV10 to DIV0 (address 120_{16}). Also, set the display frequency range. (See the next page.)

Display frequency is calculated using the below expression.

Display frequency = Horizontal synchronous frequency x Multiply value

(c) When (EXCK1, EXCK0) = (1, 0) ..... Setting disabled

(d) When (EXCK1, EXCK0) = (1, 1) .....External clock mode 2

Fosc = 20 to 110 MHz (V_{DD} = 4.75 to 5.25 V)

Input from the TCK pin a constant-period continuous external clock that synchronizes with the horizontal synchronous signal. And input from HOR pin a constant-period continuous horizontal synchronous signal.

Never stop inputting the clock while displaying.

An internal clock which is in sync with the external input clock is used as the display clock.

Because the display frequency equals the external clock frequency, set N1 (division value) that satisfies the below expressions to DIV10 to DIV0 (address 120_{16}) for make the display frequency is equal to the external clock frequency.

N1 = external clock frequency / horizontal synchronous frequency

$$N1 = \sum_{n=0}^{10} 2^n DIV_n$$

Also, set the display frequency range. (See the next page.)

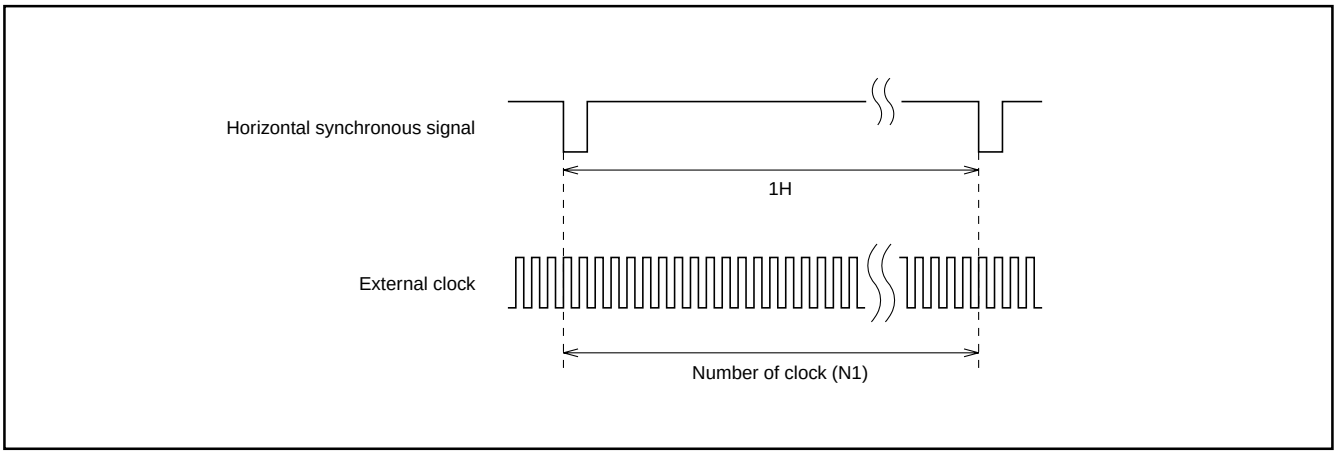


Fig. 4 Example of external clock input

(2) To set display frequency range

Whenever setting display frequency (when EXCK1 = "0", EXCK0 = "1", or EXCK1 = "1", EXCK0 = "1"), always set the display frequency range in accordance with the display frequency. This range is set from DIVS0, DIVS1, DIVS2 (address 120_{16}), RSEL0 address 121_{16}) and RSEL1 (address 122_{16}). Frequency ranges are given here below.

RSEL1	RSEL0	DIVS2	DIVS1	DIVS0	Display frequency range(MHz)
1	1	0	0	0	100.0 to 110.0
1	0	0	0	0	—
0	1	0	0	0	92.0 to 100.0
0	0	0	0	0	73.0 to 92.0
1	1	0	0	1	66.5 to 73.0
1	0	0	0	1	—
0	1	0	0	1	61.0 to 66.5
0	0	0	0	1	49.0 to 61.0
1	1	0	1	0	—
1	0	0	1	0	—
0	1	0	1	0	45.5 to 49.0
0	0	0	1	0	36.5 to 45.5
1	1	0	1	1	33.5 to 36.5
1	0	0	1	1	—
0	1	0	1	1	30.5 to 33.5
0	0	0	1	1	24.5 to 30.5
1	1	1	0	0	—
1	0	1	0	0	—
0	1	1	0	0	23.0 to 24.5
0	0	1	0	0	20.0 to 23.0

(3) Notes on setting display frequency

To change external clock (display) frequency or horizontal synchronization frequency, always use the following procedures.

To set EXCK1 = "0", EXCK0 = "1"

(a) Turn the display OFF. … DSPON (address 128_{16}) = "0"
(b) Set the display frequency. … Set from DIV10 to DIV0, DIVS0, DIVS1, DIVS2 (address 120_{16}), RSEL0 (address 121_{16}) and RSEL1 (address 122_{16}).
(c) Wait 20 ms while the horizontal synchronization signal is being input.
(d) Turn the display ON. … DSPON (address 128_{16}) = "1"

To set EXCK1 = "1", EXCK0 = "1"

(a) Turn the display OFF. … DSPON (address 128_{16}) = "0"
(b) Set the display frequency. … Set from DIV10 to DIV0, DIVS0, DIVS1, DIVS2 (address 120_{16}), RSEL0 (address 121_{16}) and RSEL1 (address 122_{16}).
(c) Wait 20 ms while the horizontal synchronization signal and external clock are being input.
(d) Turn the display ON. … DSPON (address 128_{16}) = "1"

DISPLAY FORM 1

M35076-XXXSP has the following four display forms.

(1) Blanking mode

Character size

: Blanking same as the character size.

Border size

: Blanking the background as a size from character.

Matrix-outline size

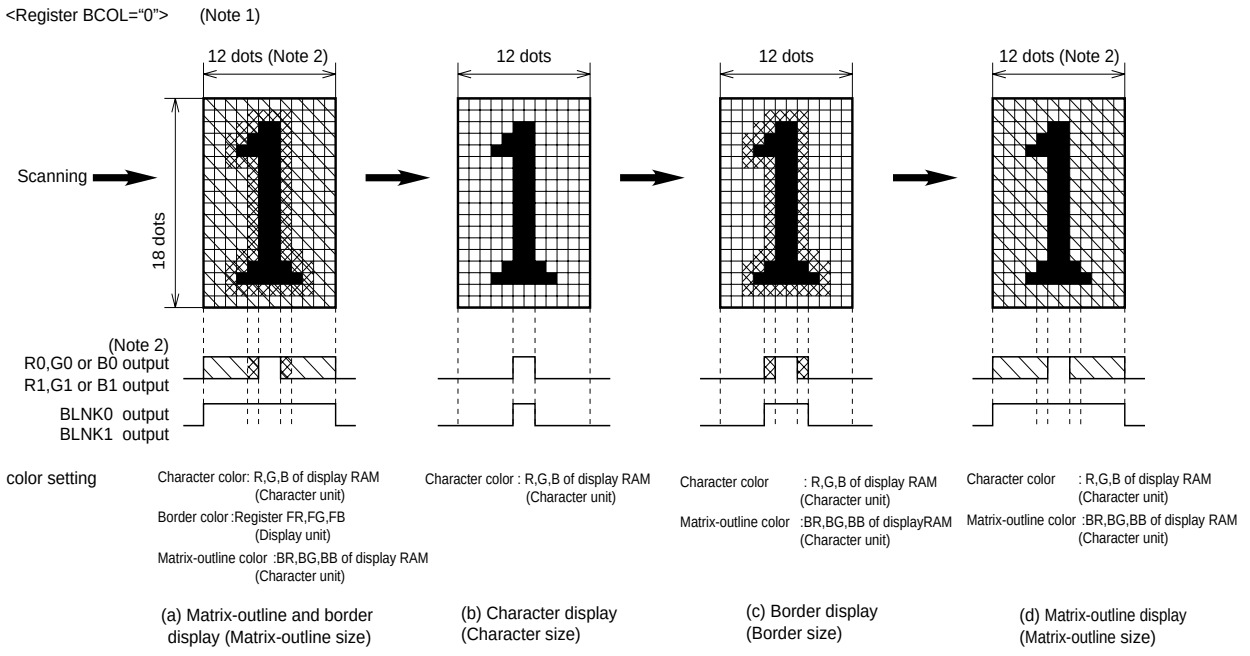
: Blanking the background 12 × 18 dot.

All blanking size

: When set register BCOL to "1", all raster area is blanking.

The display mode and blanking mode can be set line-by-line, as follows, from registers BCOL, BLK1, BLK0 (address 128_{16}), DSP0 to DSP11 (address 124_{16}).

BCOL	BLK1	BLK0	Line of DSPn = "0"		Line of DSPn = "1"	
			Display mode	Blanking mode	Display mode	Blanking mode
0	0	0	All matrix-outline border display	All matrix-outline size	All matrix-outline display	All matrix-outline size
	0	1	Character display	Character size	Border display	Border size
	1	0	Border display	Border size	All matrix-outline display	All matrix-outlinesize
	1	1	All matrix-outline display	All matrix-outline size	Character display	Character size
1	0	0	All matrix-outline border display	All blanking size	All matrix-outline display	All blanking size
	0	1	Character display		Border display	
	1	0	Border display		All matrix-outline display	
	1	1	All matrix-outline display		Character display	



Note 1. When register BCOL is set to "1", the raster range of the display modes set respectively by BLK1 and BLK0 are colored by registers RR, RG, and RB (address 127_{16}). And the blanking mode is set all blanking size (all raster size) regardless of the BLK1 and BLK0 settings.

Note 2. When register MODE1,0=1,0 setting, RGB signal of page 0 is output from R0,G0,B0 and BLNK0 pin, and RGB signal of page 1 is output from R1, G1,B1 and BLNK1 pin.

Note 3. The horizontal size of the full matrix-outline size can be set to 14 dots by register BETA14 (address 127_{16}). BLNK0 and BLNK1 can also be output at 14 dots.

Fig. 5 Example of R0,G0,B0,BLNK0,R1,G1,B1 and BLNK1 signal output

(2) Shadow display

When border display mode, if set SYAD (address 128_{16}) = “0” to “1”, it change to shadow display mode.

Border and shadow display are shown below.

Set shadow display color by BR, BG or BB of display RAM or by register FR, FG and FB (address 127_{16}).

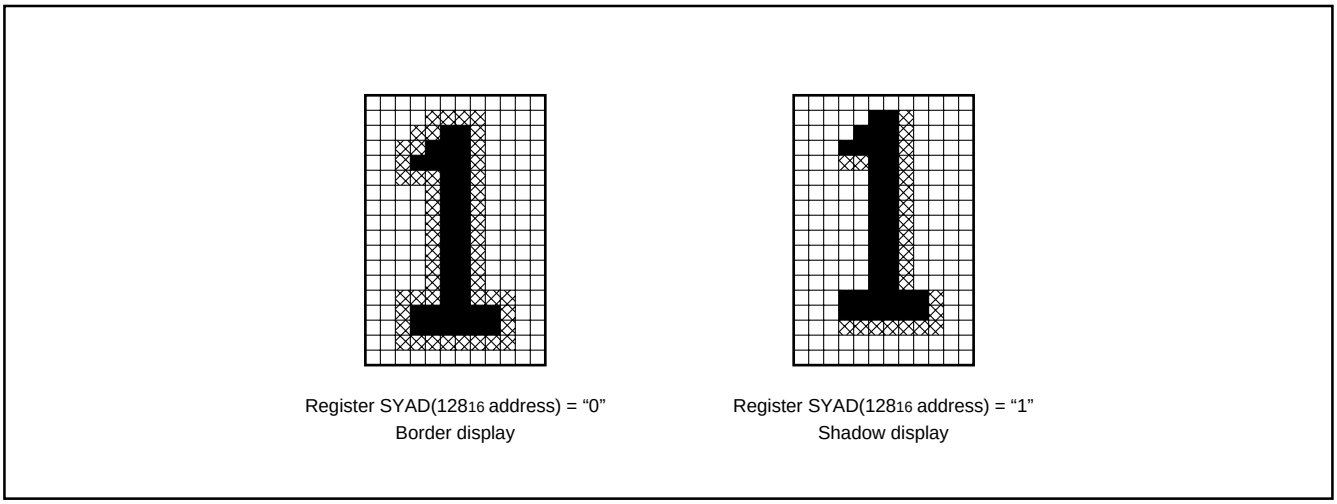


Fig. 6 Border and shadow display

DISPLAY FORM 2

This IC can display both page 0 and page 1 at the same time.

Page 0: Set the DAF bit in each addresses to "0".

Page 1: Set the DAF bit in each addresses to "1".

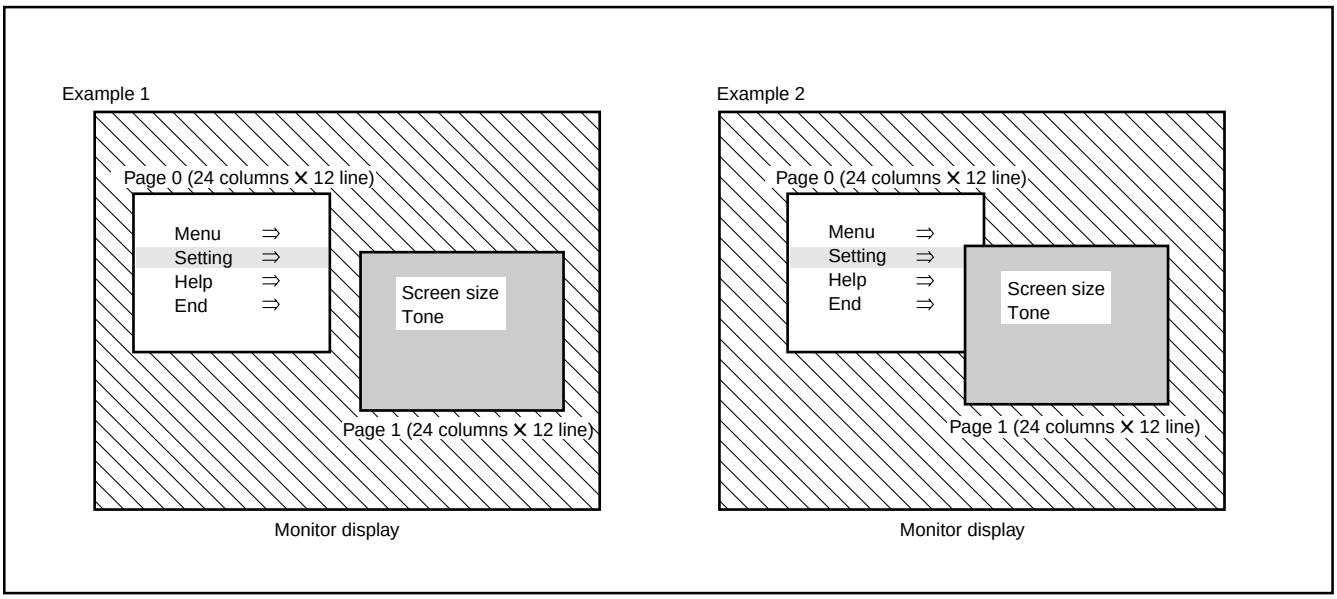


Fig. 7 Example of 2 pages display

Example 1: Display position, display size, color, etc., can be freely set for each page, and the 2 pages can be displayed on top of each other or side-by-side.

Example 2: RGB output of two pages can be outputted by one line or two lines by registers MODE0 (address 127_{16}) and MODE1 (address 128_{16}) and POPUP (address 126_{16}). And, when the display range of the 2 pages overlap on the monitor screen at the time of an one-line output, they can perform the following displays. (The POPUP register is effective only when MODE0 = "0" and MODE1 = "0".)

MODE1	MODE0	POPUP	Output system	Display mode
0	0	0	1 system	Standard (Page 1 priority)
		1	1 system	Standard (Page 0 priority)
0	1	—	1 system	AND
1	0	—	2 systems	–
1	1	—	1 system	OR

(1) Output system

(a) 1 system : Output RBG signal of both of page 0 and 1 from R0,G0,B0 and BLNK0 pin (For overlapping areas, refer to below.)

(b) 2 systems : RBG signal of page 0 is output from R0,G0,B0 and BLNK0 pin, RBG signal of page 1 is output from R1,G1,B1 and BLNK1 pin.

(2) Display mode (Overlapping areas of Page 0 and 1)

(a) Standard (page 1 priority).. Page 1 has priority in overlapping areas. Page 0 is not displayed in those areas.

(b) Standard (page 0 priority).. Page 0 has priority in overlapping areas. Page 1 is not displayed in those areas.

(c) AND ..... In overlapping areas, the RGB output of the 2 pages is AND processed and output.

(d) OR ..... In overlapping areas, the RGB output of the 2 pages is OR processed and output.

Note : Set 0 (port output) to control register PTC2, PTC4 and PT67 except at 2 systems output setting (MODE1=1,MODE0=0.)

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

Character code FF_{16} is fixed as a blank without background. Therefore, cannot register a character font in this code.

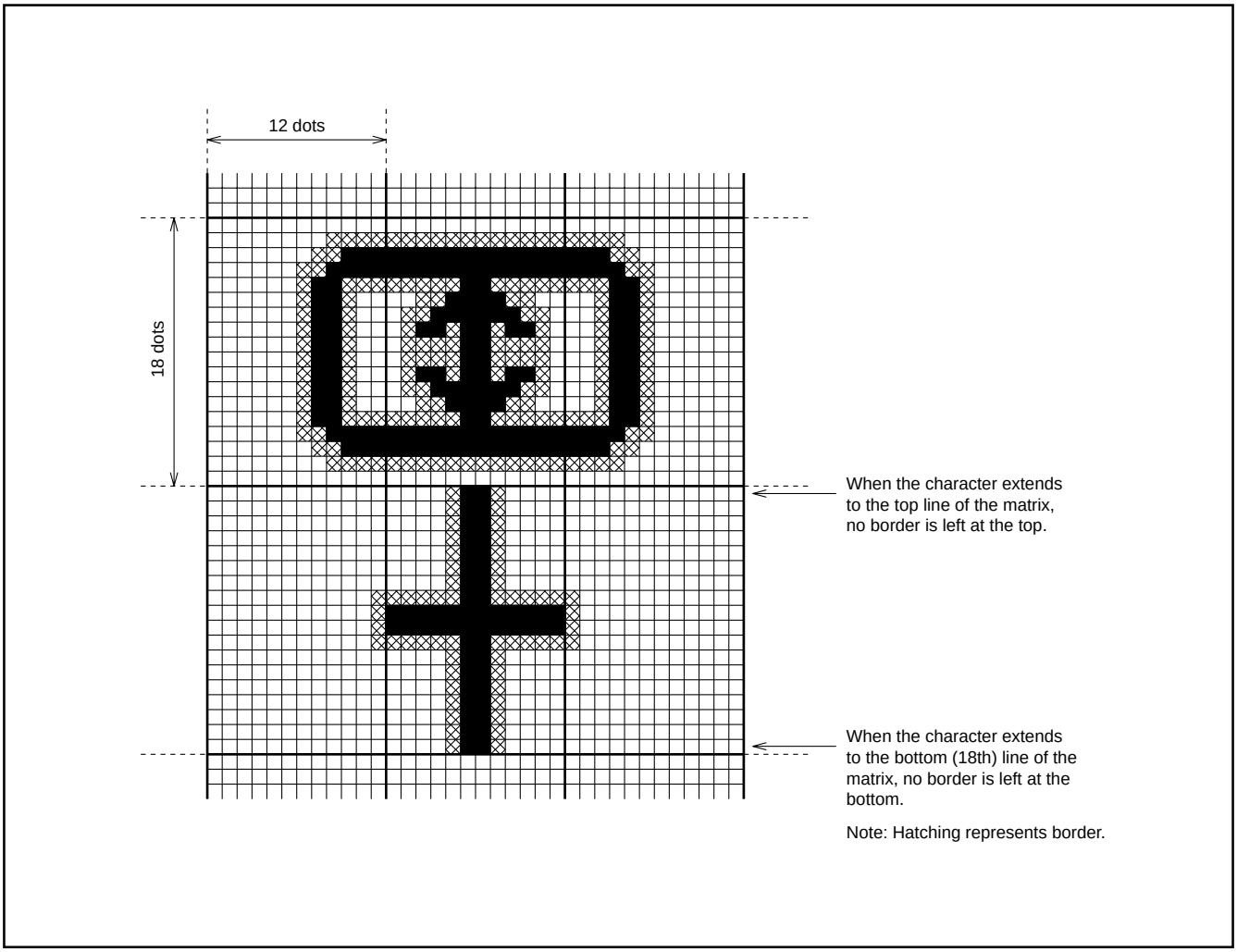


Fig. 8 Example of border display

DATA INPUT EXAMPLE

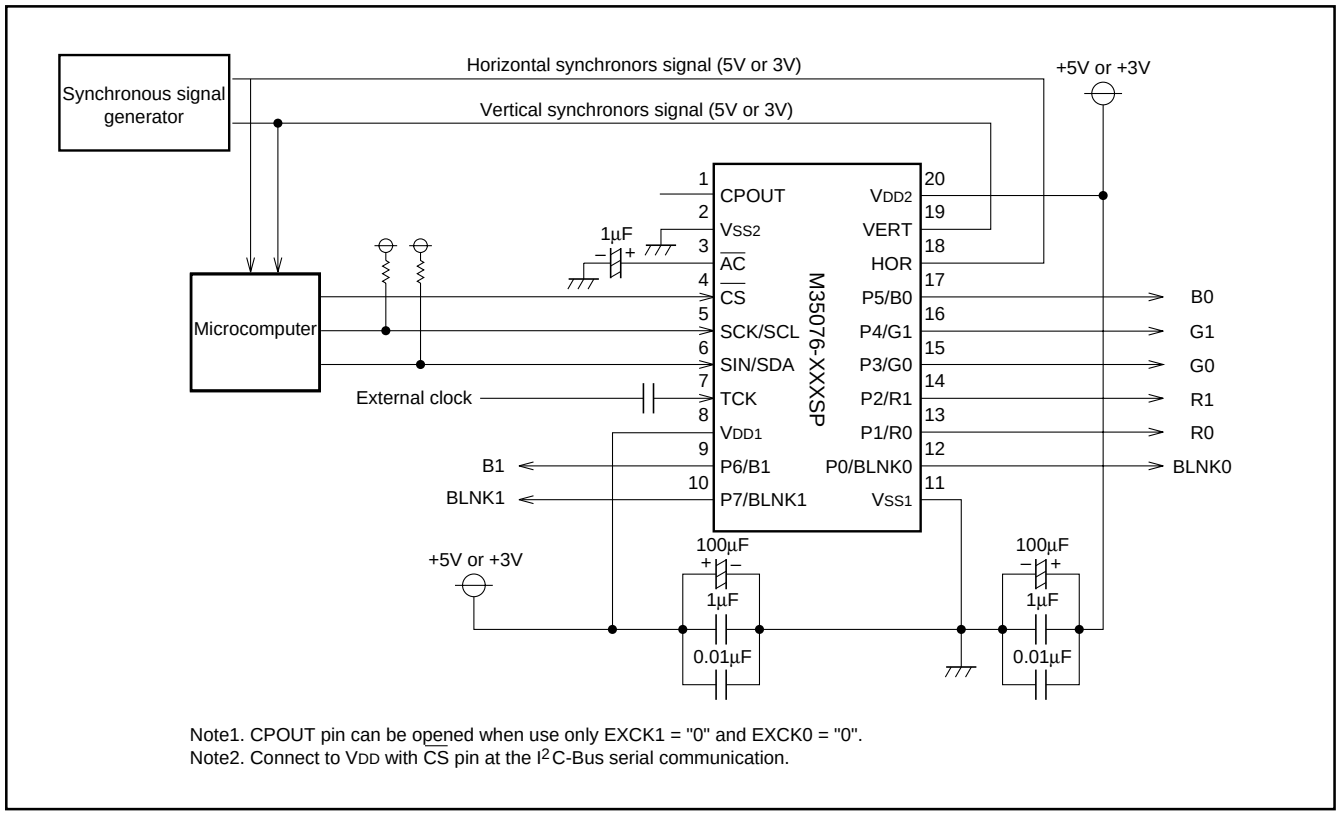
Data of display RAM and display control registers can be set by the 16-bit serial input function or the I²C-BUS serial input function. Example of data setting is shown in Figure 9 (at EXCK0 = "1", EXCK1 = "0" setting).

Data input example (M35076-XXXSP)

Address/data	DAF (Note1)	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0		Remarks
	200m sec hold																	System set up (Note 4)
Address 120₁₆	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0		Address setting
Data 120₁₆	0	1	DIVS2	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0		Frequency value setting (Note2)
Data 121₁₆	0	RSEL0	PTD7	PTD6	1	PTD4	1	PTD2	1	1	1	0	1	0	1	1		Output setting
Data 122₁₆	0	RSEL1	0	0	0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0		Horizontal display location setting
Data 123₁₆	0	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	0 page	Vertical display location setting
Data 124₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Display form setting
Data 125₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Character size setting
Data 126₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Character size setting
Data 127₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Color, character size setting
Data 128₁₆	0	0	0	0	0	0	0	0	0	0	0	POLH	POLV	0	0	0		Page 0 display OFF
Address 122₁₆	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0		Address setting
Data 122₁₆	1	0	0	0	0	HP10	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0		Horizontal display location setting
Data 123₁₆	1	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0		Vertical display location setting
Data 124₁₆	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 page	Display form setting
Data 125₁₆	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Character size setting
Data 126₁₆	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Character size setting
Data 127₁₆	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Color, character size setting
Data 128₁₆	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Page 1 display OFF
	200m sec hold																	Be stable / Waiting time
Data 000₁₆	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0		
⋮	⋮	Background coloring			Blink-ing	Character color			Character code								0 page	Character setting
Data 11F₁₆	0	BB	BG	BR	BLINK	B	G	R	C7	C6	C5	C4	C3	C2	C1	C0		
Address 000₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Data 000₁₆	1	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0		
⋮	⋮	Background coloring			Blink-ing	Character color			⋮	Character code							1 page	Character setting
Data 11F₁₆	1	BB	BG	BR	BLINK	B	0	R	0	C6	C5	C4	C3	C2	C1	C0		
Address 128₁₆	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0		Address setting
Data 128₁₆	1	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0		Page 1 display ON Display form setting (Note 3)
Address 128₁₆	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0		Address setting
Data 128₁₆	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0		Page 0 display ON Display form setting (Note 3)

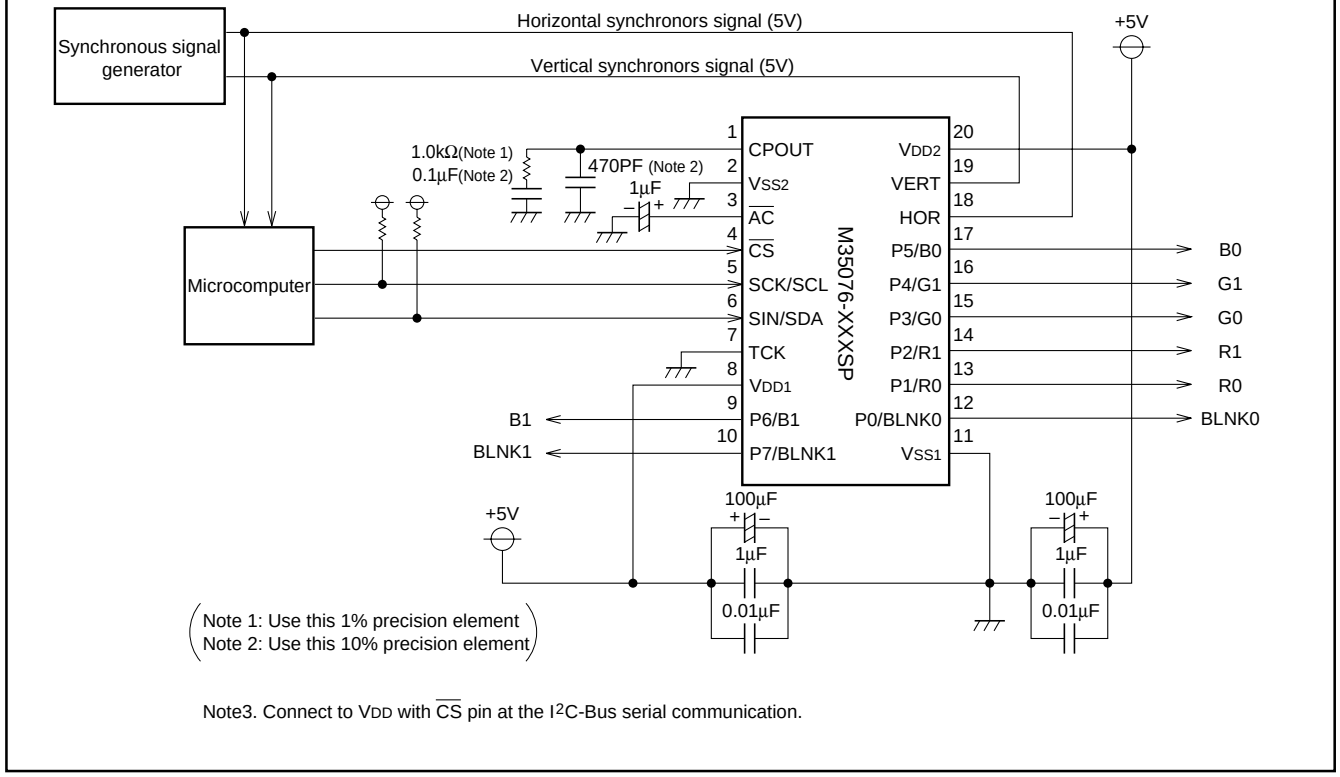
Notes 1 : The page in which data is written is controlled by the address. To write data into page 0, set "0". To write data into page 1, set "1".
2 : Input a continuous clock of constant period from the TCK pin. Also, input a horizontal synchronous signal into the HOR pin and a vertical synchronous signal into the VERT pin.
3 : Matrix-outline display in this data.
4 : Secure the waiting time of 200ms after releasing AC, and set data from setting the display frequency (setting of the register).
5 : Set data to display RAM at internal clock (display clock) is stabilized.

Fig 9. Example of data setting



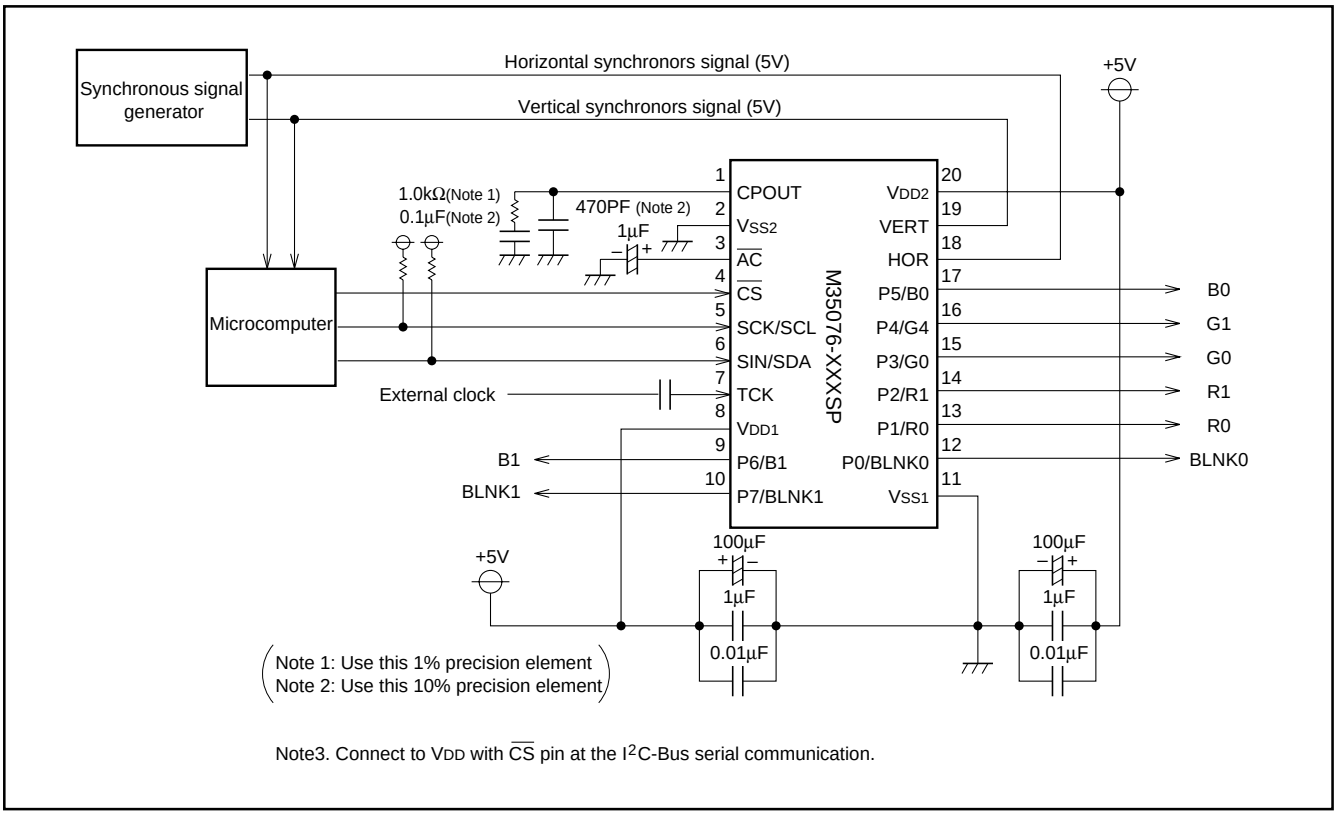
Note1. CPOUT pin can be opened when use only EXCK1 = "0" and EXCK0 = "0".
Note2. Connect to V_{DD} with $\overline{CS}$ pin at the I²C-Bus serial communication.

Fig 10. Example of the M35076-XXXSP peripheral circuit (External clock mode 1. At EXCK1 = “0”, EXCK0 = “0”)



Note3. Connect to V_{DD} with $\overline{CS}$ pin at the I²C-Bus serial communication.

Fig 11. Example of the M35076-XXXSP peripheral circuit (Internal clock mode. At EXCK1 = “0”, EXCK0 = “1”)



Note3. Connect to V_{DD} with $\overline{CS}$ pin at the I^2C-Bus serial communication.

Fig 12. Example of the M35076-XXXSP circuit (External clock mode 2. At EXCK1 = “1”, EXCK0 = “1”)

DATA INPUT 1

(1) The16-bit communication function

(a)Serial data should be input with the LSB first.

(b)The address consists of 16 bits.

(c)The data consists of 16 bits.

(d)The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits. Therefore, it is not necessary to in put the address from the second data.

Note. Stop the input to $\overline{SCK}$ pin and fix it to “H” at $\overline{CS}$ pin “H” level.

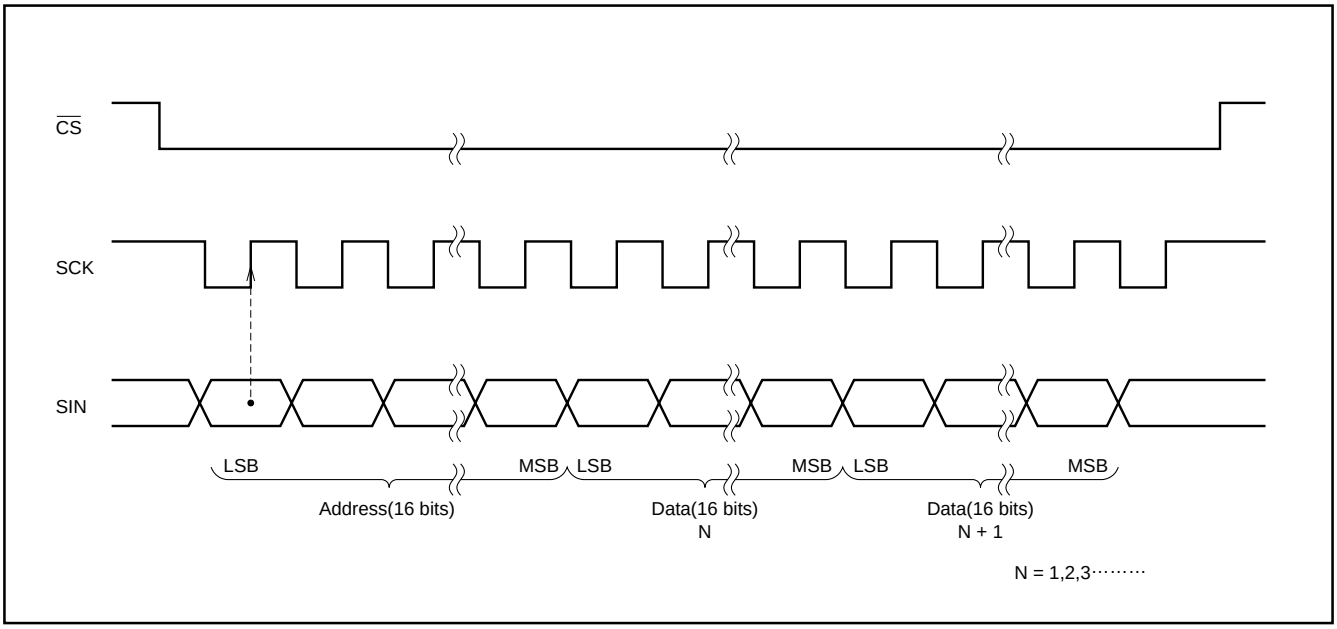


Fig.13 Serial input timing

(2)Timing requirements
Data input

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_{w(SCK)}$	SCK width	200	—	—	ns	See Figure 14
$t_{su(\overline{CS})}$	$\overline{CS}$ setup time	200	—	—	ns	
$t_{h(\overline{CS})}$	$\overline{CS}$ hold time	2	—	—	µs	
$t_{su(SIN)}$	SIN setup time	200	—	—	ns	
$t_{h(SIN)}$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	10	—	—	µs	

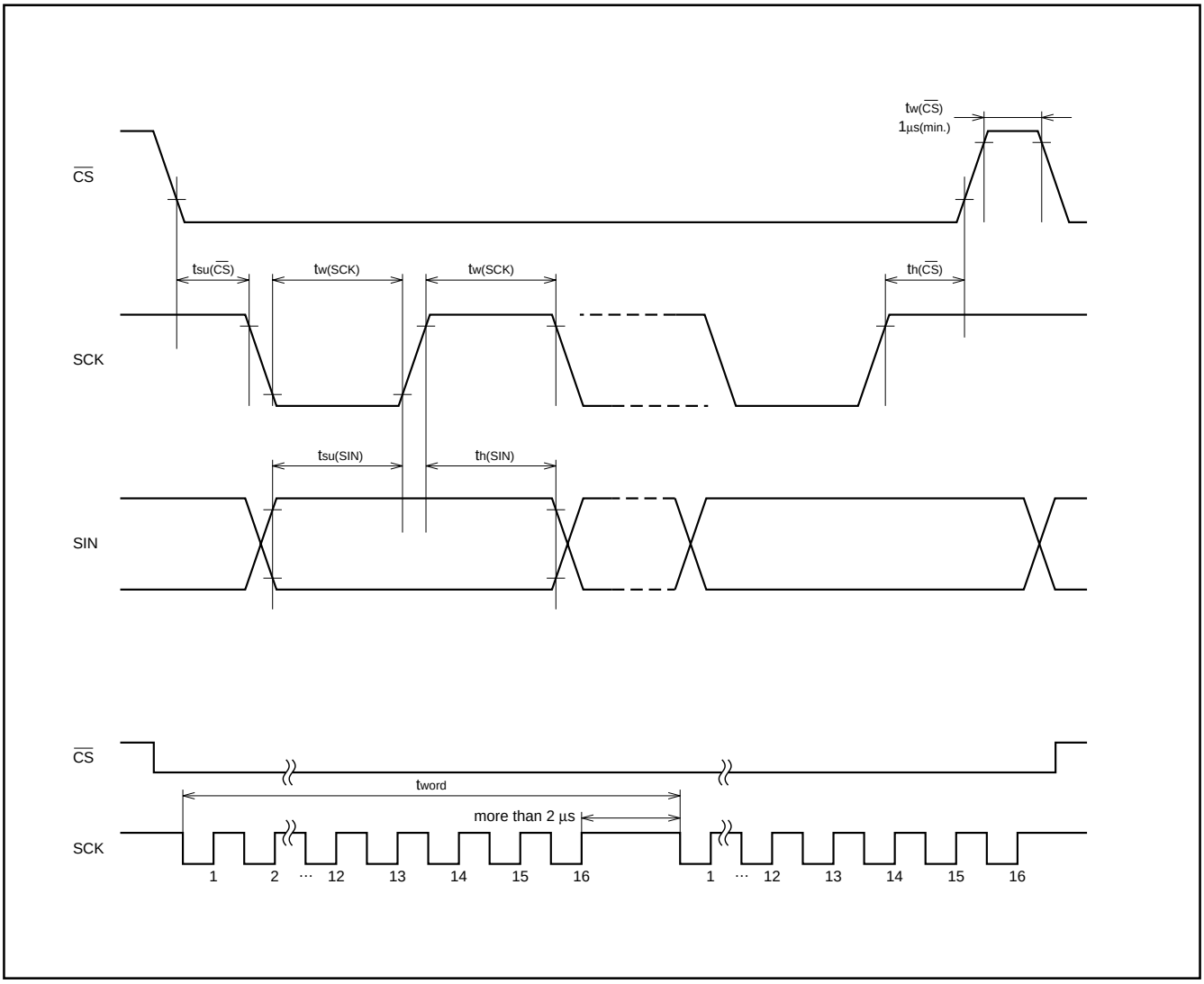


Fig. 14 Serial input timing requirements

DATA INPUT 2

(1) The I^2C-Bus communication function (at VDD=5V only)

This IC has a built-in data transmission interface which utilizes 2 unidirectional buses. In communications, this IC functions as a slave reception device. Set $\overline{CS}$ pin to "H" level at the I^2C-Bus serial input communication.

The IC is synchronized with the serial clock (SCL) sent from the master device and receives the data (SDA). Communications are controlled from the start/stop states. Also, always input the control byte after attaining the start state.

The below chart shows the start/stop state and control byte configuration.

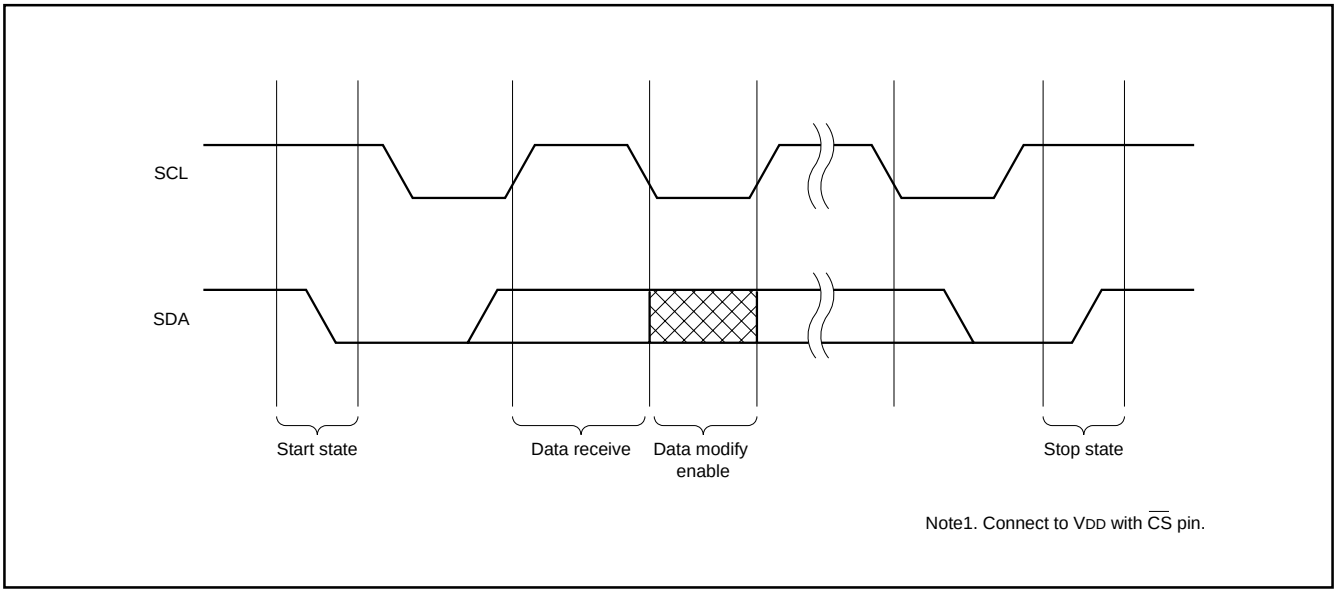


Fig. 15 Start state / Stop state

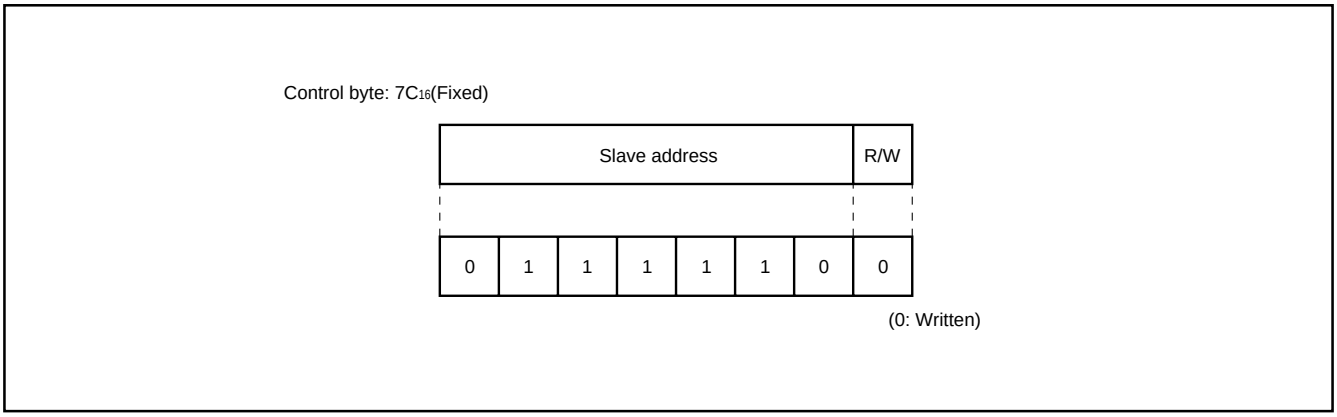


Fig. 16 Control byte configuration

(2) Data input (Sequence)

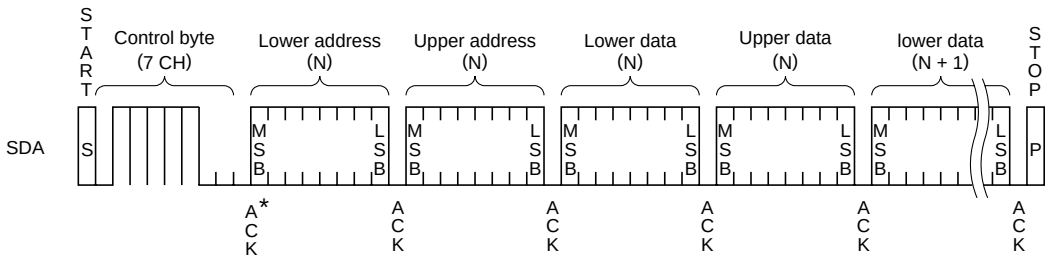
(a) Addresses are consists of 16 bits.

(b) Data is consists of 16 bits.

(c) Addresses and data are communicated in 8-bit units. Input the lower 8 bits before the upper 8 bits. Make input from the MSB side.

(d) After the start state has been attained and the control byte (7CH) received, the next 16 bits (2 bytes) are for inputting the address. Addresses are increased in increments for every 16 bits (2 bytes) of data input thereafter. As a result, it is not necessary to input the address from the second data.

Note: During external synchronous, stop the external clock input from the TCK pin while inputting data.



ACK* (Acknowledge) : Output the acknowledge signal whenever one byte input after the start state. Output the acknowledge signal and recieve the data thereafter when mach the slave address (7CH).

Fig. 17 Data input sequence

(3) Timing requirement
Data input

Symbol	Parameter	Limits				Unit	Remarks
		Typ. mode		High-speed mode			
		Min.	Max.	Min.	Max.		
f_{CLK}	Clock frequency	0	100	0	400	KHz	
t_{HIGH}	HIGH period of Clock	4000	–	600	–	ns	
t_{LOW}	LOW period of Clock	4700	–	1300	–	ns	
t_R	SDA & SCL rise time	–	1000	20+(Note) 0.1C_B	300	ns	
t_F	SDA & SCL fall time	–	300	20+(Note) 0.1C_B	300	ns	
t_{HD} : STA	Hold time at START status	4000	–	600	–	ns	
t_{SU} : STA	Set up time at START status	4700	–	600	–	ns	Only at START state repeating generation
t_{HD} : DAT	Data input hold time	0	–	0	–	ns	
t_{SU} : DAT	Data input setup time	250	–	100	–	ns	
t_{SU} : STO	Set up time at STOP state	4000	–	600	–	ns	
t_{BUF}	Bus release time	4700	–	1300	–	ns	Time must be released bus before next transmission
t_{SP}	Input filter / spike suppress (SDA & SCL pin)	N/A	N/A	0	50	ns	

Note. C_B = total capacitance of 1 bus line.

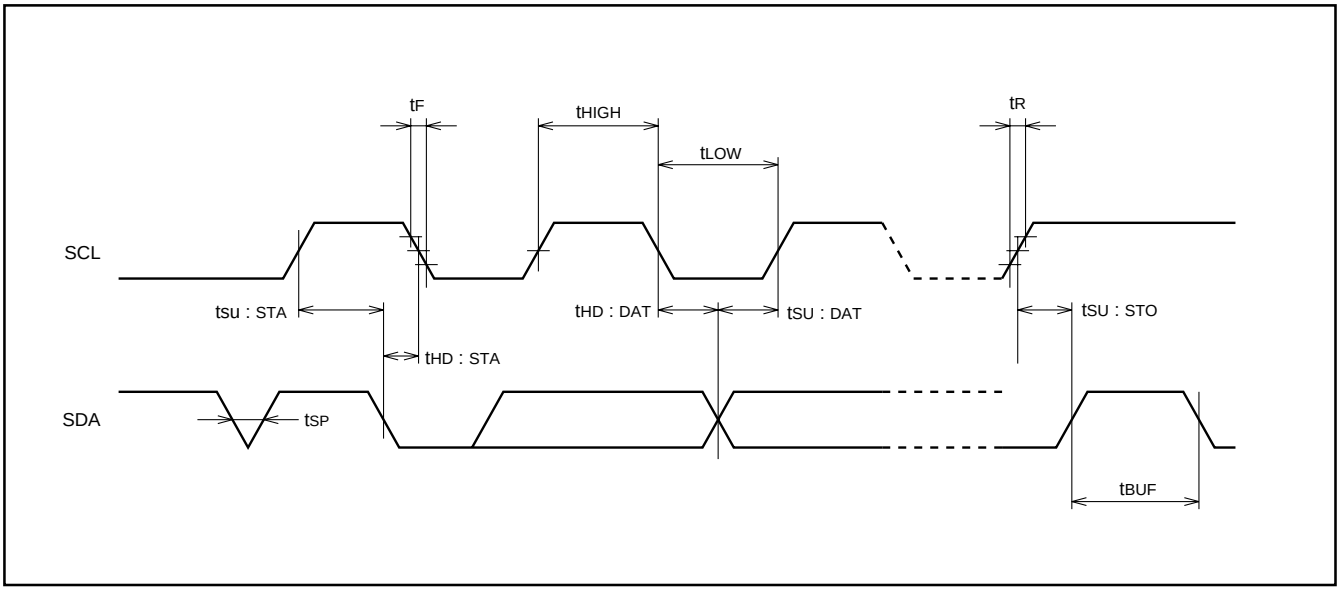


Fig. 18 Data input timing

ABSOLUTE MAXIMUM RATINGS (V_{DD} = 5.00V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to V_{SS}.	–0.3 to +6.0	V
V_I	Input voltage		V_{SS} –0.3 ≤ V_I ≤ V_{DD} +0.3	V
V_O	Output voltage		V_{SS} ≤ V_O ≤ V_{DD}	V
P_d	Power dissipation	Ta = +25°C	+300	mW
T_{opr}	Operating temperature		–20 to +85	°C
T_{stg}	Storage temperature		–40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (V_{DD} = 5.00V, Ta = –20 to +85°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage	5V		4.75	5.0	5.25	V
		3V		2.50	3.0	3.50	V
V_{IH}	"H" level input voltage	$\overline{AC}$, $\overline{CS}$, HOR, VERT		0.8V_{DD}	V_{DD}	V_{DD}	V
		SCK/SCL, SIN/SDA		0.7V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	"L" level input voltage	$\overline{AC}$, $\overline{CS}$, HOR, VERT		0	0	0.2V_{DD}	V
		SCK/SCL, SIN/SDA		0	0	0.3V_{DD}	V
F_{OSC}	Oscillating frequency for display	External clock mode 1	V_{DD} = 4.75 to 5.25 V	6.3	—	80.0	MHz
			V_{DD} = 2.50 to 3.50 V	6.3	—	40.0	MHz
		External clock mode 2	V_{DD} = 4.75 to 5.25 V	20.0	—	110.0	MHz
		Internal clock mode	V_{DD} = 4.75 to 5.25 V	20.0	—	110.0	MHz
H.sync	Horizontal synchronous signal input frequeney		V_{DD} = 4.75 to 5.25 V	15.0	—	130.0	kHz
			V_{DD} = 2.50 to 3.50 V	15.0	—	60.0	kHz

ELECTRICAL CHARACTERISTICS 1 V_{DD}=5V (V_{DD} = 5.00V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage		Ta = –20 to +85°C	4.75	5.0	5.25	V
I_{DD}	Supply current		V_{DD} = 5.00V	—	40	60	mA
V_{OH}	"H" level output voltage	P0 to P7 (Note1)	V_{DD} = 4.75V, I_{OH} = -0.4mA	3.5	—	—	V
		CPOUT	V_{DD} = 4.75V, I_{OH} = -0.05mA				
V_{OL}	"L" level output voltage	P0 to P7 (Note2)	V_{DD} = 4.75V, I_{OL} = 0.4mA	—	—	0.4	V
		CPOUT	V_{DD} = 4.75V, I_{OL} = 0.05mA				
		SIN/SDA	V_{DD} = 4.75V, I_{OL} = 3.0mA				
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$		V_{DD} = 5.00V	10	30	100	kΩ
V_{TCK}	External clock input width		4.75V ≤ V_{DD} ≤ 5.25V	0.6V_{DD}	—	0.9V_{DD}	V

Notes 1. The current from the IC must not exceed – 0.4 mA/port at any of the port pins (P0 to P7).
2. The current flowing into the IC must not exceed 0.4 mA/port at any of port pins (P0 to P7).

ELECTRICAL CHARACTERISTICS 2 V_{DD}=3V (V_{DD} = 3.00V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	Ta = –20 to +85°C	2.50	3.00	3.50	V
I_{DD}	Supply current	V_{DD} = 3.00V	—	20	30	mA
V_{OH}	"H" level output voltage P0 to P7 (Note1)	V_{DD} = 2.70V, I_{OH} = -0.1mA	2.30	—	—	V
V_{OL}	"L" level output voltage P0 to P7 (Note2)	V_{DD} = 2.70V, I_{OH} = 0.1mA	—	—	0.4	V
R_I	Pull-up resistance $\overline{AC}$, $\overline{CS}$	V_{DD} = 3.00V	30	—	150	kΩ
V_{TCK}	External clock input width	2.20V ≤ V_{DD} ≤ 3.50V	0.7V_{DD}	—	V_{DD}	V

Notes 1. The current from the IC must not exceed – 0.1 mA/port at any of the port pins (P0 to P7).
2. The current flowing into the IC must not exceed 0.1 mA/port at any of port pins (P0 to P7).

NOTE FOR SUPPLYING POWER

(1)Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35076-XXXSP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin in hysteresis input with the pull-up resistor.

The timing about power supplying of $\overline{AC}$ pin is shown in Figure 19.

After supplying the power (V_{DD} and V_{SS}) to M35076-XXXSP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep V_{IL} time; tw of the $\overline{AC}$ pin for more than 1ms.

Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than $0.8 \times V_{DD}$ and keeping 200ms wait time.

(2)Timing of power supplying to V_{DD1} and V_{DD2}.

Supply power to V_{DD1} and V_{DD2} at the same time.

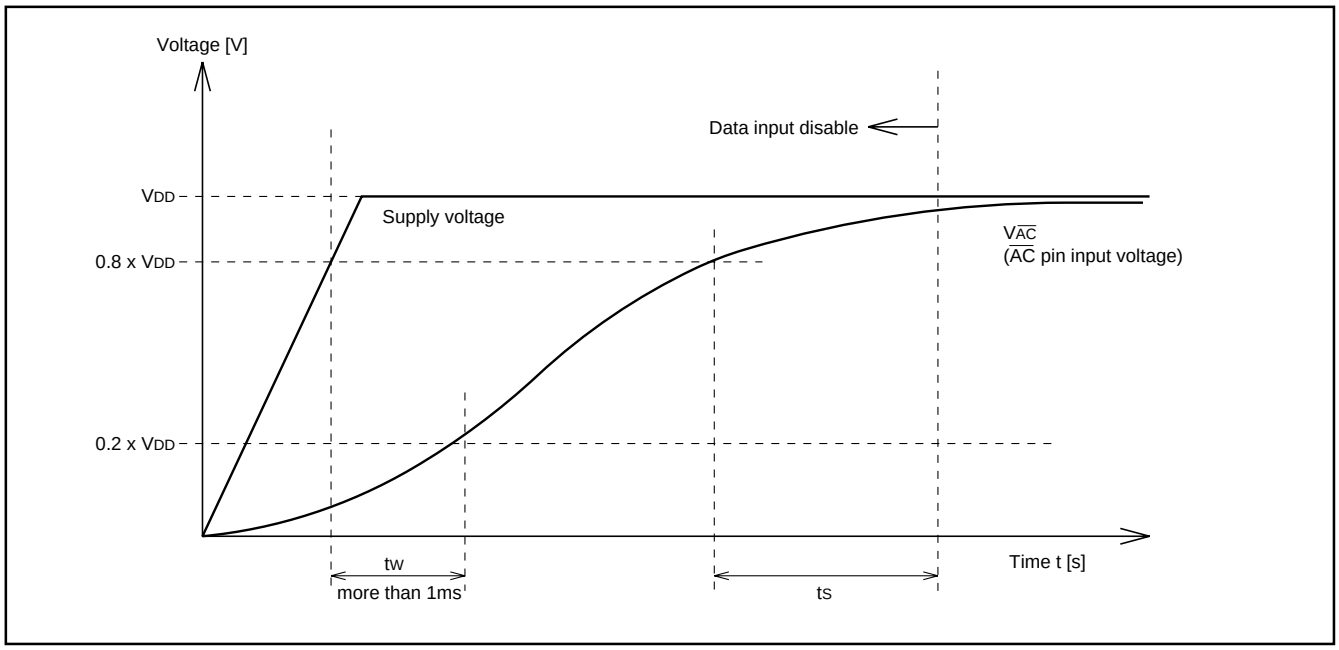


Fig. 19 Timing of power supplying to $\overline{AC}$ pin

PRECAUTION FOR USE

Notes on noise and latch-up

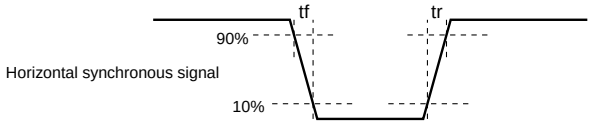
In order to avoid noise and latch-up, connect a bypass capacitor (≈0.1μF) directly between the V_{DD1} pin and V_{SS1} pin, and the V_{DD2} pin and V_{SS2} pin using a heavy wire.

Note for waveform timing of the horizontal signals to the HOR pin

Set horizontal synchronous signal edge* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/$\overline{F}$ register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by B/$\overline{F}$ register.



DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

(1) M35076-XXXSP mask ROM order confirmation form

(2) 20P4B mark specification form

(3) ROM data : EPROMs or floppy disks

*In the case of EPROMs, thres sets of EPROMs are required per pattern.

*In the case of floppy disks, 3.5-inch 2HD disk (1BM format) is required per pattern.

STANDARD ROM TYPE : M35076-001SP

M35076-001SP is a standard ROM type of M35076-XXXSP. The character patterns for 0 page are fixed to the contents of Figure 20 to 23, the character patterns for page 1 are fixed to the contents of Figure 24 to 27.

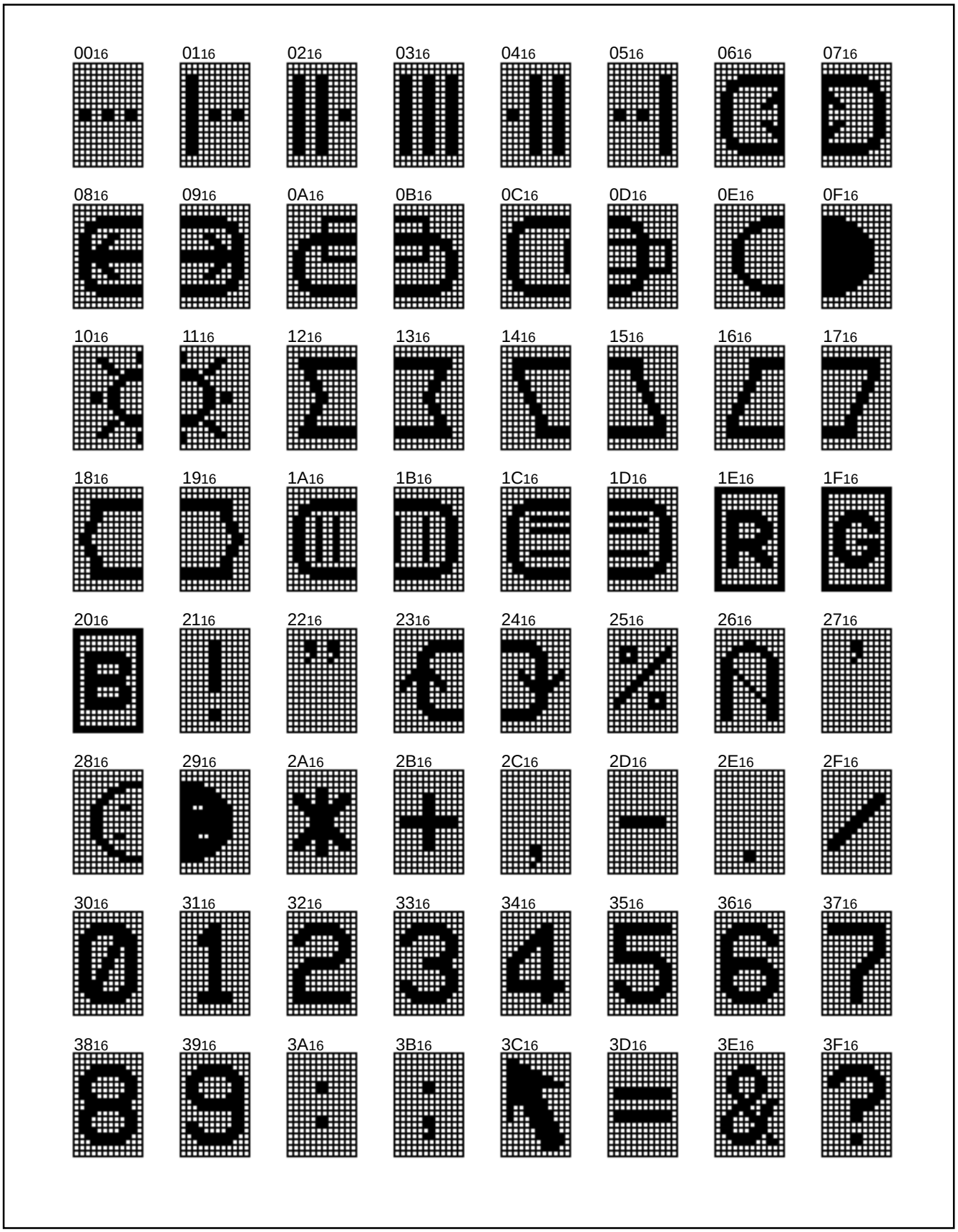


Fig. 20 M35076-001SP character pattern for page 0 (1)

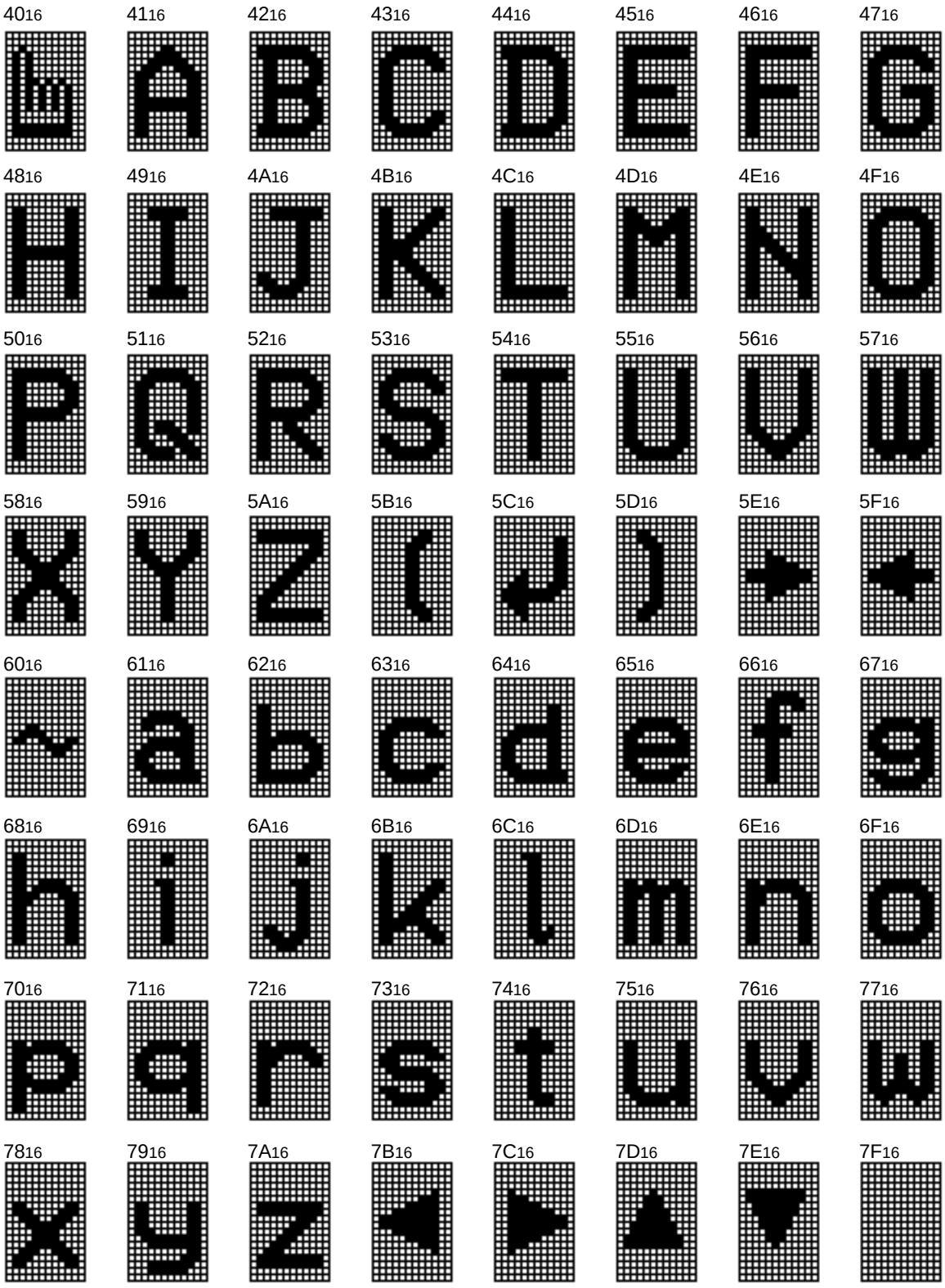


Fig. 21 M35076-001SP character pattern for page 0 (2)

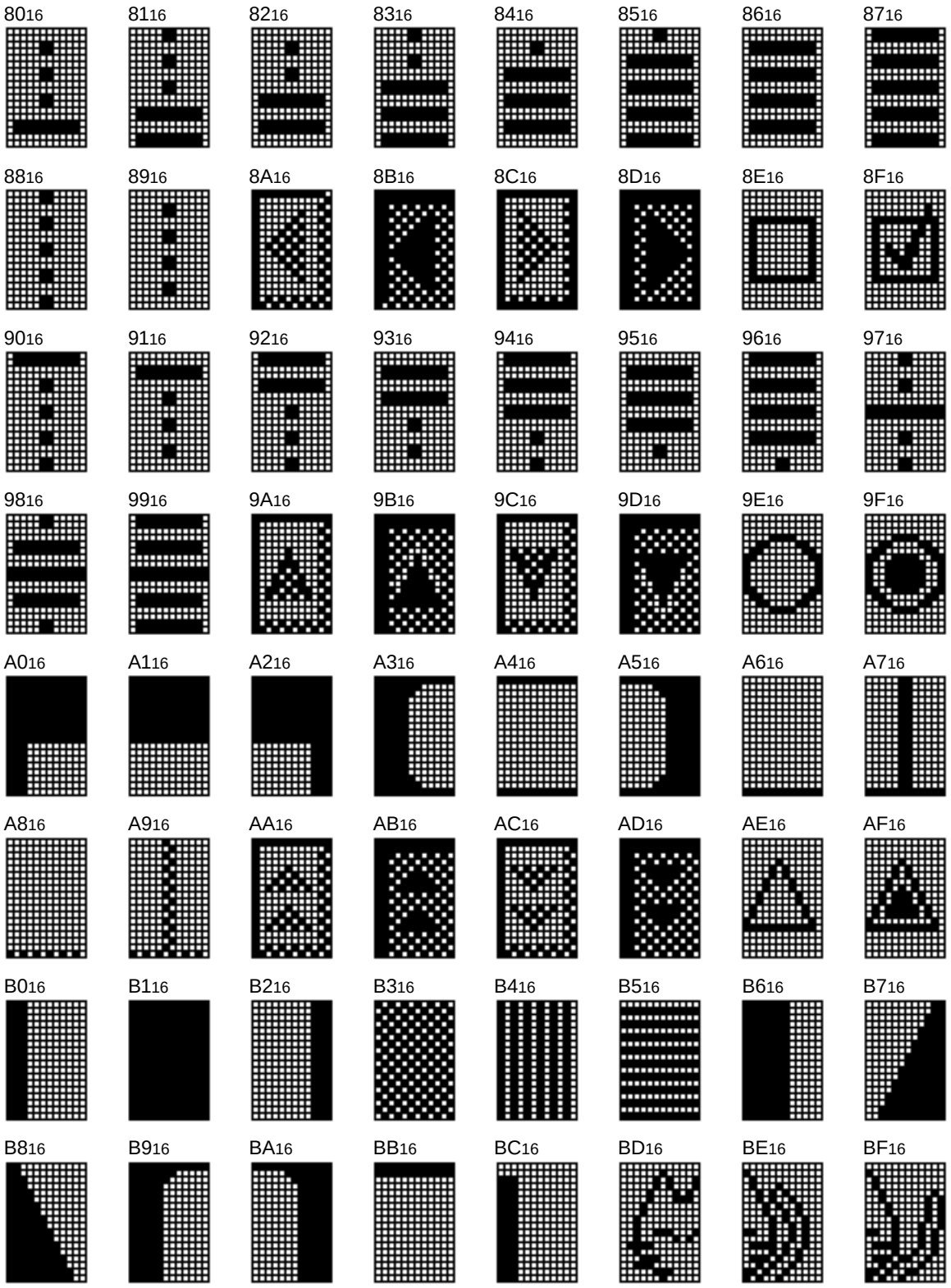


Fig. 22 M35076-001SP character pattern for page 0 (3)

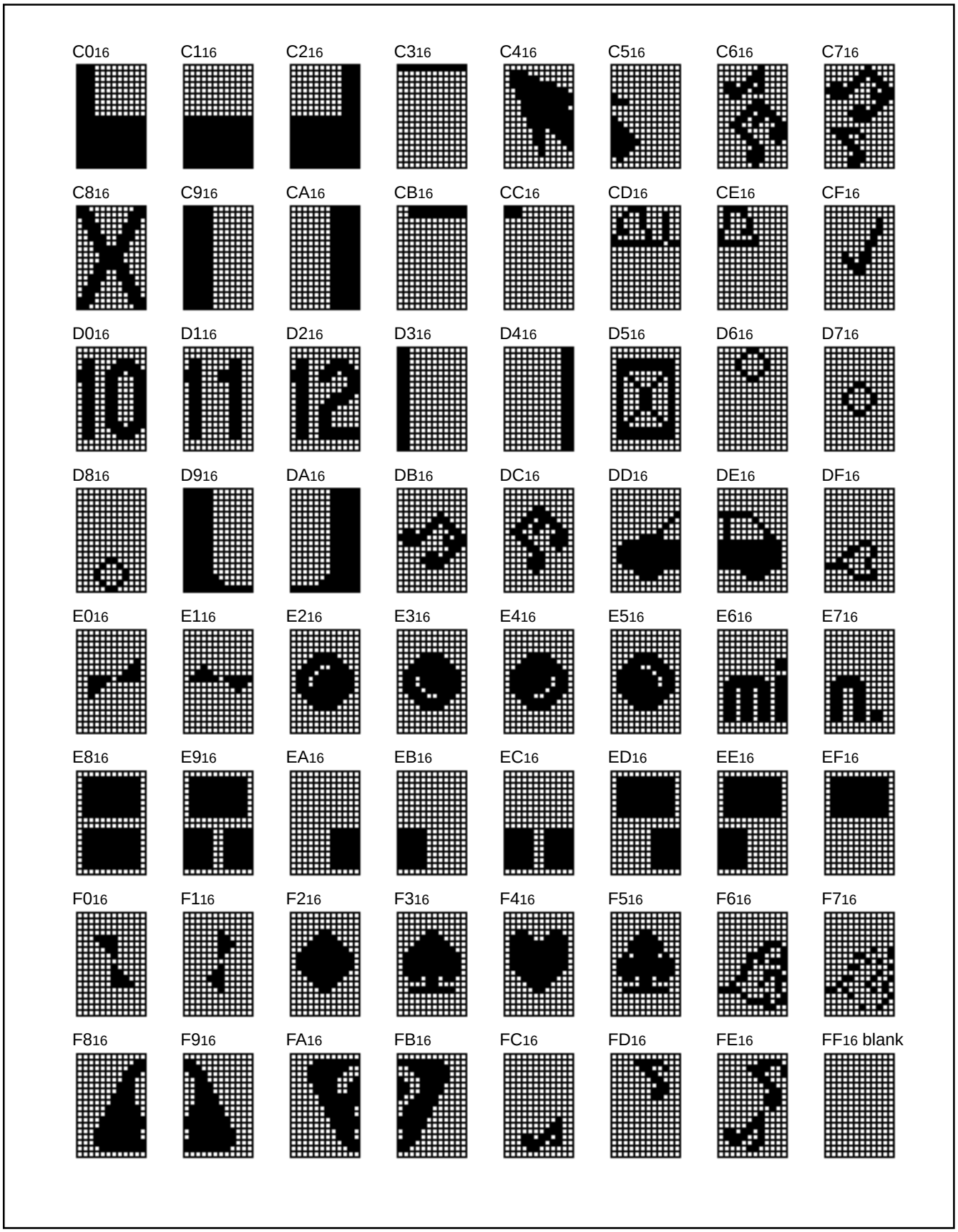


Fig. 23 M35076-001SP character pattern for page 0 (4)

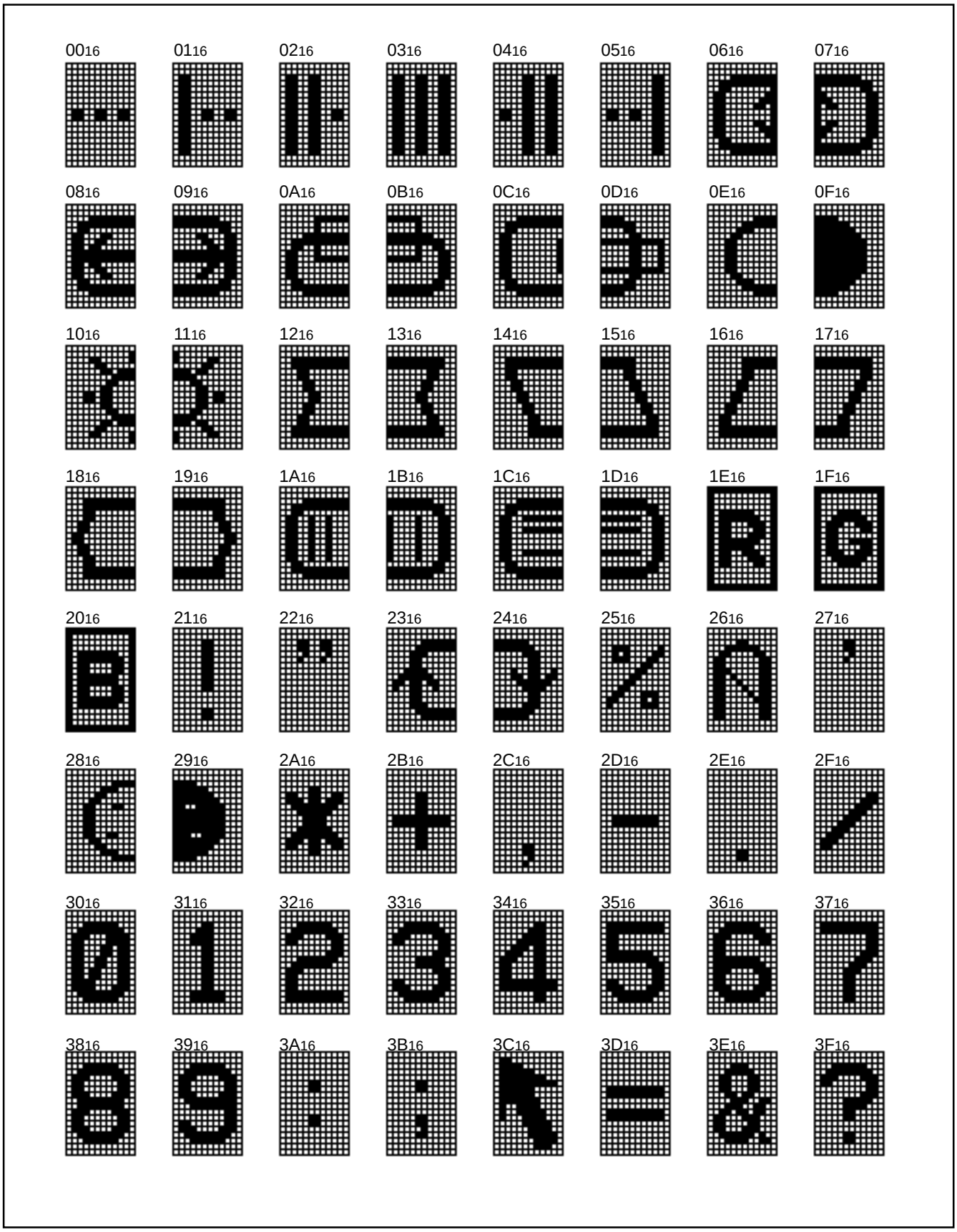


Fig. 24 M35076-001SP character pattern for page 1 (1)

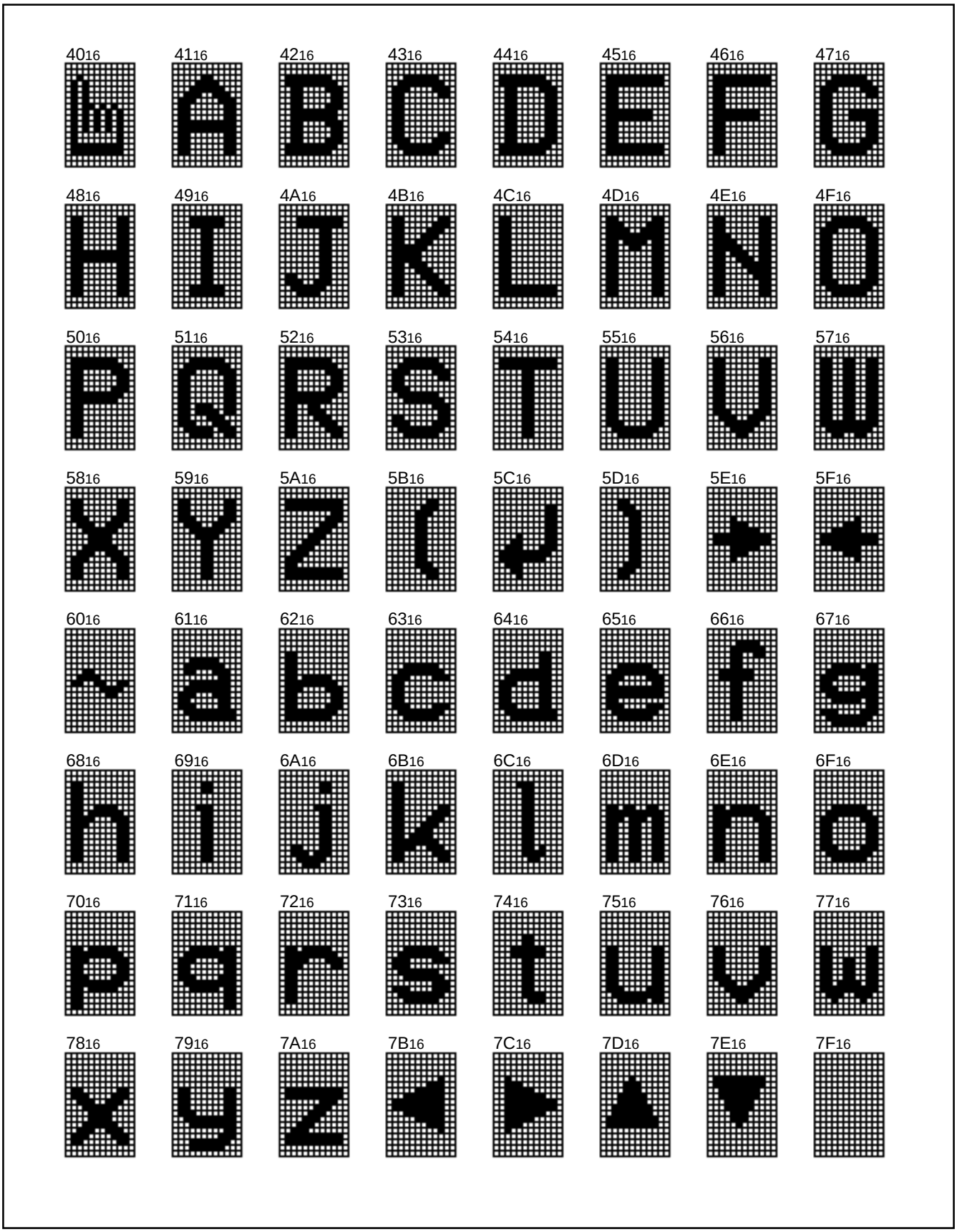


Fig. 25 M35076-001SP character pattern for page 1 (2)

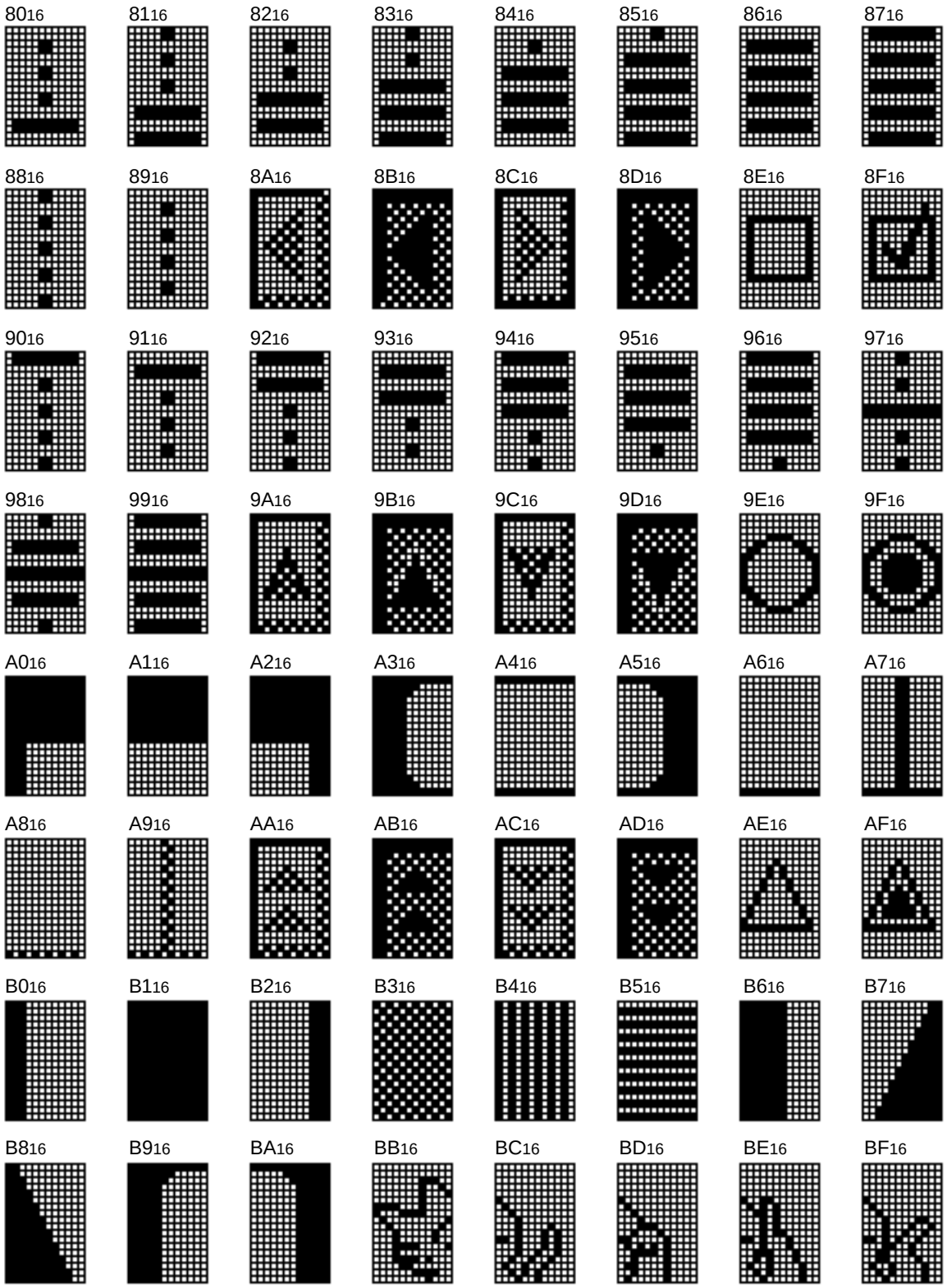


Fig. 26 M35076-001SP character pattern for page 1 (3)

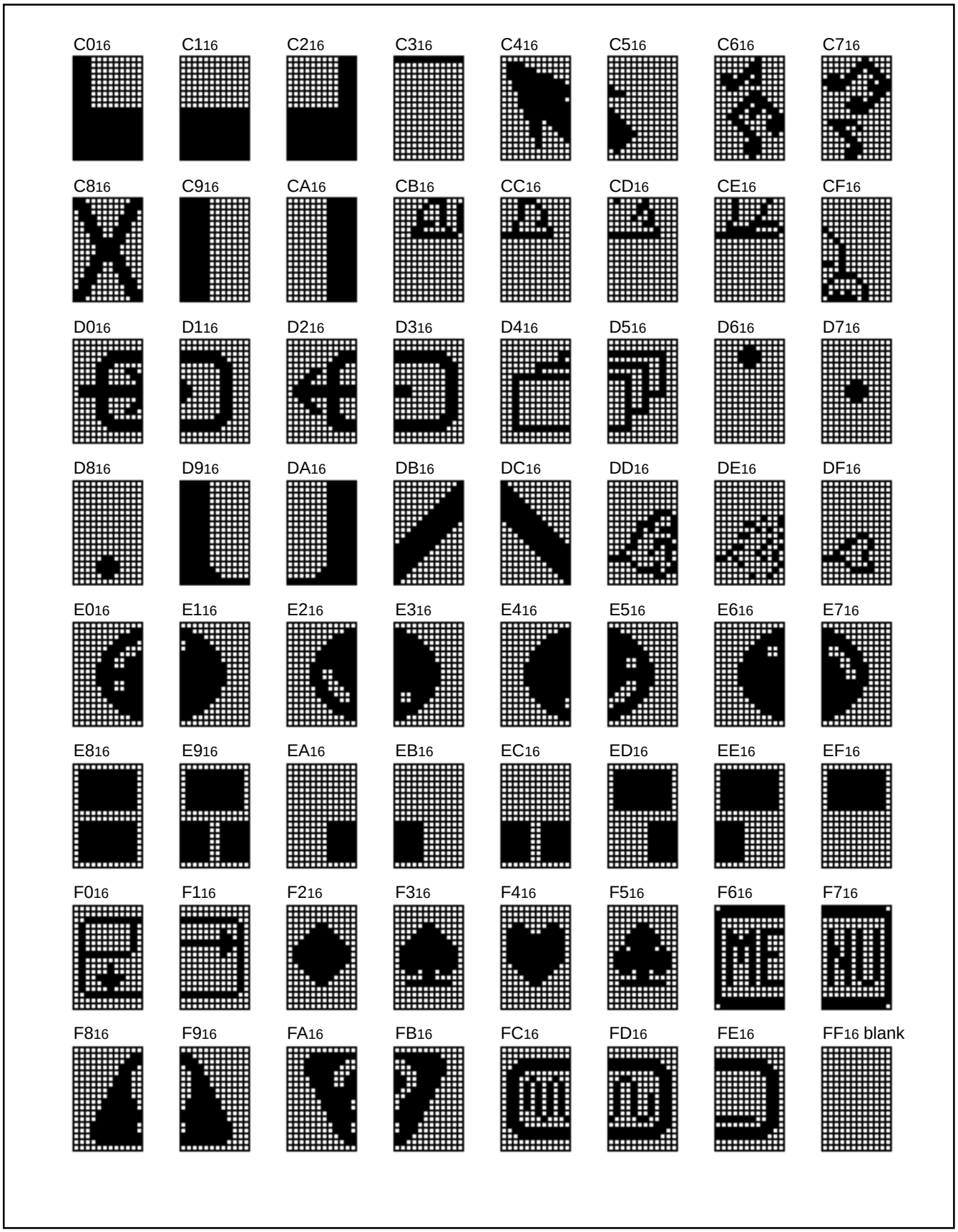


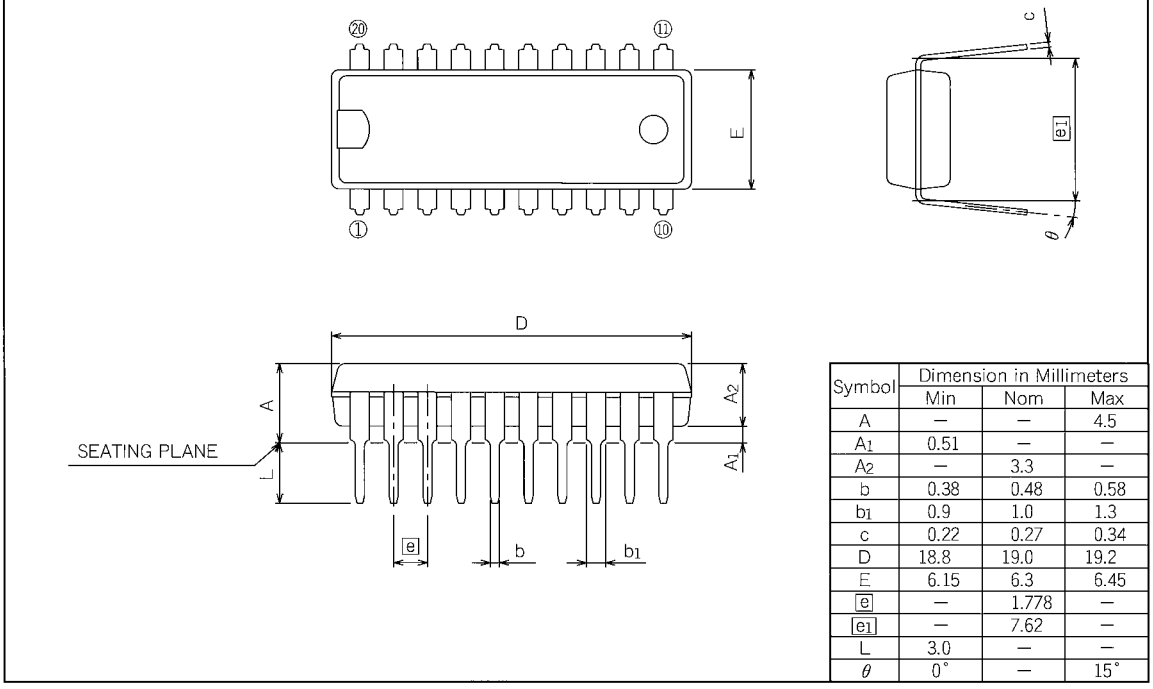
Fig. 27 M35076-001SP character pattern for page 1 (4)

PACKAGE OUTLINE

20P4B — Plastic 20pin 300mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP20-P-300-1.78	—	1.0	

Scale : 2.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.38	0.48	0.58
b_1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	1.778	—
e_1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

MITSUBISHI MICROCOMPUTERS

M35076-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

New publication, effective MAR. 2002.
Specifications subject to change without notice.

MITSUBISHI ELECTRIC

REVISION DESCRIPTION LIST	M35076-XXXSP Data Sheet

Rev. No.	Revision Description	Rev. date
1.0	First Edition	0203