National Semiconductor

29F68
Dynamic RAM Controller

General Description

The 29F68 is a high-performance memory controller, replacing many SSI and MSI devices by grouping several unique functions. It provides two 9-bit address latches and two 9-bit counters for row and column address generation during refresh. A 2-bit bank select latch for row and column address generation during refresh, and a 2-bit bank select latch for the two high order address bits are provided to select one of the four RAS and CAS outputs.

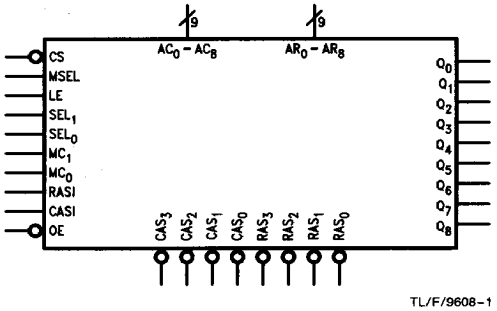
The 29F68 is functionally equivalent to AMD's Am2968 and Motorola's MC74F2968.

Features

- High-performance memory controller
- Replaces many SSI and MSI devices by grouping several unique functions
- Functionally equivalent to AMD's Am2968 and Motorola's MC74F2968
- Provides control for 16K, 64K, or 256K dynamic RAM systems
- Outputs directly drive up to 88 DRAMs
- Highest order two address bits select one of four banks of RAMs
- Chip Select for easy expansion
- Provides memory refresh with error correction mode

Ordering Code: See Section 5

Logic Symbol



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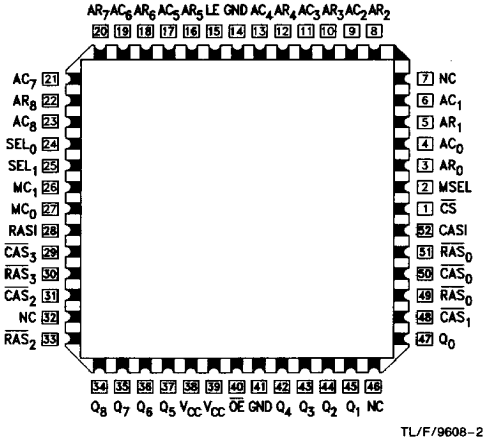
Connection Diagram

Pin Assignment for LCC and PCC



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Pin Description

Name	I/O	Description
AR_0–AR_8 AC_0–AC_8	I	**Address Inputs.** AR_0–AR_8 are latched in as the 9-bit Row Address for the RAM. These inputs drive Q_0–Q_8 when the 29F68 is in the Read/Write mode and MSEL is LOW. AC_0–AC_8 are latched in as the Column Address, and will drive Q_0–Q_8 when MSEL is HIGH and the 29F68 is in the Read/Write mode. The addresses are latched with the Latch Enable (LE) signal.
SEL_0–SEL_1	I	**Bank Select.** These two inputs are normally the two higher order address bits, and are used in the Read/Write mode to select which bank of memory will be receiving the $\overline{RAS}_n$ and $\overline{CAS}_n$ signals after RASI and CASI go HIGH.
LE	I	**Latch Enable.** This active-HIGH input causes the Row, Column and Bank Select latches to become transparent, allowing the latches to accept new input data. A LOW input on LE latches the input data, assuming it meets the setup and hold time requirements.
MSEL	I	**Multiplexer Select.** This input determines whether the Row or Column Address will be sent to the memory address inputs. When MSEL is HIGH the Column Address is selected, while the Row Address is selected when MSEL is LOW. The address may come from either the address latch or refresh address counter depending on MC_0, MC_1.
$\overline{CS}$	I	**Chip Select.** This active-LOW input is used to enable the 29F68. When $\overline{CS}$ is active, the 29F68 operates normally in all four modes. When $\overline{CS}$ goes HIGH, the device will not enter the Read/Write mode. This allows other devices to access the same memory that the 29F68 is controlling (e.g., DMA controller).
$\overline{OE}$	I	**Output Enable.** This active-LOW input enables/disables the output signals. When $\overline{OE}$ is HIGH, the outputs of the 29F68 enter the high impedance state. The $\overline{OE}$ signal allows more than one 29F68 to control the same memory, thus providing an easy method to expand the memory size.
MC_0, MC_1	I	**Mode Control.** These inputs are used to specify which of the four operating modes the 29F68 should be using. The description of the four operating modes is given in the Mode Control Function Table.
Q_0–Q_8	O	**Address Outputs.** These address outputs will feed the DRAM address inputs and provide drive for memory systems up to 500 pF in capacitance.
RASI	I	**Row Address Strobe Input.** During normal memory cycles, the decoded $\overline{RAS}_n$ output ($\overline{RAS}_0$, $\overline{RAS}_1$, $\overline{RAS}_2$ or $\overline{RAS}_3$) is forced LOW after receipt of RASI. In either refresh mode, all four $\overline{RAS}_n$ outputs will go LOW following RASI going HIGH.
$\overline{RAS}_0$–$\overline{RAS}_3$	O	**Row Address Strobe.** Each one of the Row Address Strobe outputs provides a $\overline{RAS}_n$ signal to one of the four banks of dynamic memory. Each will go LOW only when selected by SEL_0 and SEL_1 and only after RASI goes HIGH. All four go LOW in response to RASI in either of the Refresh modes.
CASI	I	**Column Address Strobe Input.** This input going active will cause the selected $\overline{CAS}_n$ output to be forced LOW.
$\overline{CAS}_0$–$\overline{CAS}_3$	O	**Column Address Strobe.** During normal Read/Write cycles the two select bits (SEL_0, SEL_1) determine which $\overline{CAS}_n$ output will go active following CASI going HIGH. When memory error correction is performed, only the $\overline{CAS}_n$ signal selected by $CNTR_0$ and $CNTR_1$ will be active. For non-error correction cycles, all four $\overline{CAS}_n$ outputs remain HIGH.

Functional Description

The 29F68 is designed to be used with 16k, 64k, or 256k dynamic RAMs and is functionally equivalent to AMD's AM2968. The 29F68 provides row/column address multiplexing, refresh address generation and bank selection for up to four banks of RAMs.

Twenty (20) address bits (AR_0–AR_8, AC_0–AC_8, and bank select addresses SEL_0 and SEL_1) are presented to the controller. These addresses are latched by a 20-bit latch. A 20-bit counter generates the refresh address.

A 9-bit multiplexer selects the output address between the input row address, column address, refresh counter row address, column address, or zero (clear). Four RAS and four CAS outputs select the appropriate bank of RAMs and strobe in the row and column addresses.

It should be noted that the counters are cleared (MC_0, MC_1 = 1,1) on the next RASI transition, but the Q outputs are asynchronously cleared through the multiplexer.

Mode Control Function Table

MC_1	MC_0	Operating Mode
0	0	**Refresh without Error Correction.** Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four $\overline{RAS}_n$ outputs are active while the four $\overline{CAS}_n$ signals are kept HIGH.
0	1	**Refresh with Error Correction/Initialize**—During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four $\overline{RAS}_n$ outputs go active in response to RASI, while only one $\overline{CAS}_n$ output goes LOW in response to CASI. The Bank Counter keeps track of which $\overline{CAS}_n$ output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern.
1	0	**Read/Write**— This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL; SEL_0 and SEL_1 are decoded to determine which $\overline{RAS}_n$ and $\overline{CAS}_n$ will be active.
1	1	**Clear Refresh Counter**—This mode will clear the three refresh counters (Row, Column, and Bank) on the HIGH-to-LOW transition of RASI, putting them at the start of the refresh sequence. In this mode, all four $\overline{RAS}_n$ are driven LOW upon receipt of RASI so that DRAM wake-up cycles may be performed. This mode also asynchronously clears the Q_n outputs.

Address Output Function Table

$\overline{CS}$	MC_1	MC_0	MSEL	Mode	MUX Output
L	L	L	X	Refresh without Error Correction	Row Counter Address
	L	H	H	Refresh with Error Correction	Column Counter Address
			L		Row Counter Address
	H	L	H	Read/Write	Column Address Latch
			L		Row Address Latch
	H	H	X	Clear Refresh Counter	Zero
H	L	L	X	Refresh without Error Correction	Row Counter Address
	L	H	H	Refresh with Error Correction	Column Counter Address
			L		Row Counter Address
	H	L	X	Read/Write	Zero
	H	H	X	Clear Refresh Counter	Zero

$\overline{RAS}$ Output Function Table

RASI	$\overline{CS}$	MC_1	MC_0	SEL_1	SEL_0	Mode	$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$
L	X	X	X	X	X	Non-refresh	H	H	H	H
H	L	L	L	X	X	Refresh without Scrubbing	L	L	L	L
		L	H	X	X	Refresh with Scrubbing	L	L	L	L
		H	L	L	L	Read/Write	L	H	H	H
				L	H		H	L	H	H
				H	L		H	H	L	H
				H	H		H	H	H	L
		H	H	X	X	Clear Refresh Counter	L	L	L	L
	H	L	L	X	X	Refresh without Error Correction	L	L	L	L
		L	H			Refresh with Error Correction	L	L	L	L
		H	L			Read/Write	H	H	H	H
		H	H			Clear Refresh Counter	L	L	L	L

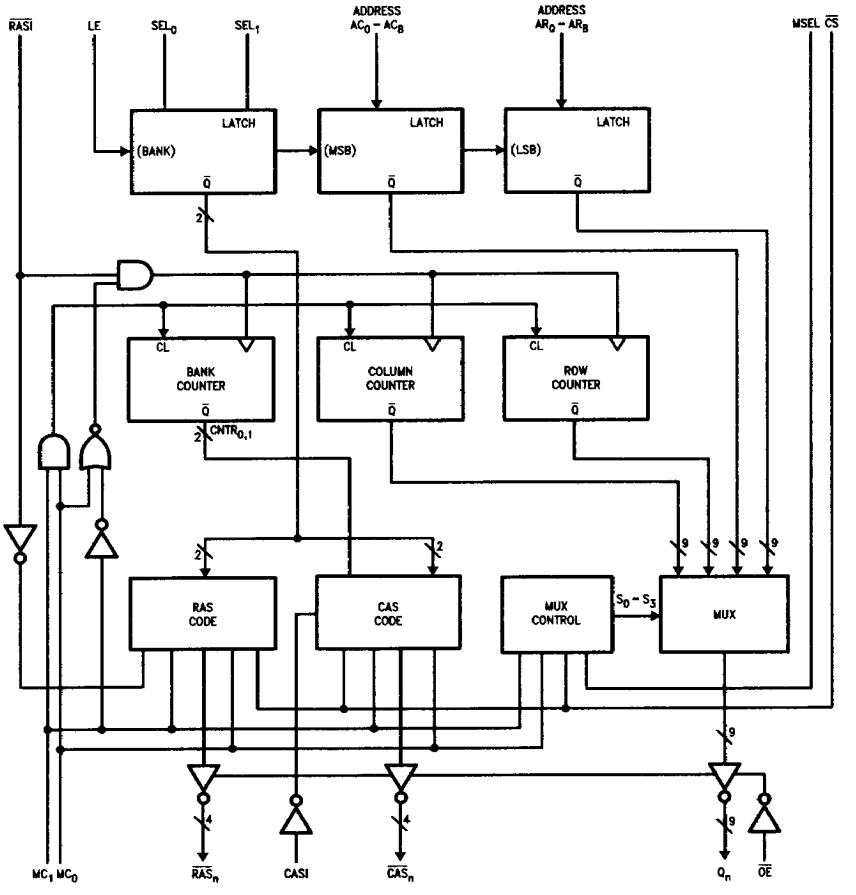
$\overline{CAS}$ Output Function Table

Inputs				Internal Counter		Inputs		Outputs			
CASI	$\overline{CS}$	MC_1	MC_0	$CNTR_1$	$CNTR_0$	SEL_1	SEL_0	$\overline{CAS}_0$	$\overline{CAS}_1$	$\overline{CAS}_2$	$\overline{CAS}_3$
H	L	L	L	X	X	X	X	H	H	H	H
		L	H	L	L	X	X	L	H	H	H
				L	H			H	L	H	H
				H	L			H	H	L	H
				H	H			H	H	H	L
		H	L	X	X	L	L	L	H	H	H
						L	H	H	L	H	H
						H	L	H	H	L	H
						H	H	H	H	H	L
	H	H	H	X	X	X	X	H	H	H	H
		L	L	X	X	X	X	H	H	H	H
		L	H	L	L	X	X	L	H	H	H
				L	H			H	L	H	H
				H	L			H	H	L	H
				H	H			H	H	H	L
		H	L	X	X	X	X	H	H	H	H
		H	H								
L	X	X	X	X	X	X	X	H	H	H	H

Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
AC_0–AC_8	Column Address	1.0/1.0	20 μA/−0.6 mA
AR_0–AR_8	Row Address	1.0/1.0	20 μA/−0.6 mA
Q_0–Q_8	Address Outputs	50/33.3	−1 mA/20 mA
MC_0, MC_1	Memory Cycle	1.0/1.0	20 μA/−0.6 mA
$\overline{CS}$	Chip Select Input	1.0/1.0	20 μA/−0.6 mA
MSEL	Multiplexer Select Input	1.0/1.0	20 μA/−0.6 mA
LE	Latch Enable Input	1.0/1.0	20 μA/−0.6 mA
SEL_0, SEL_1	Select Inputs	1.0/1.0	20 μA/−0.6 mA
RASI	Row Address Strobe In	1.0/1.0	20 μA/−0.6 mA
CASI	Column Address Strobe In	1.0/1.0	20 μA/−0.6 mA
$\overline{RAS}_0$–$\overline{RAS}_3$	Row Address Stobe Outputs	50/33.3	−1 mA/20 mA
$\overline{CAS}_0$–$\overline{CAS}_3$	Column Address Strobe Outputs	50/33.3	−1 mA/20 mA
$\overline{OE}$	Output Enable	1.0/1.0	20 μA/−0.6 mA

Block Diagram



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Timing Waveforms

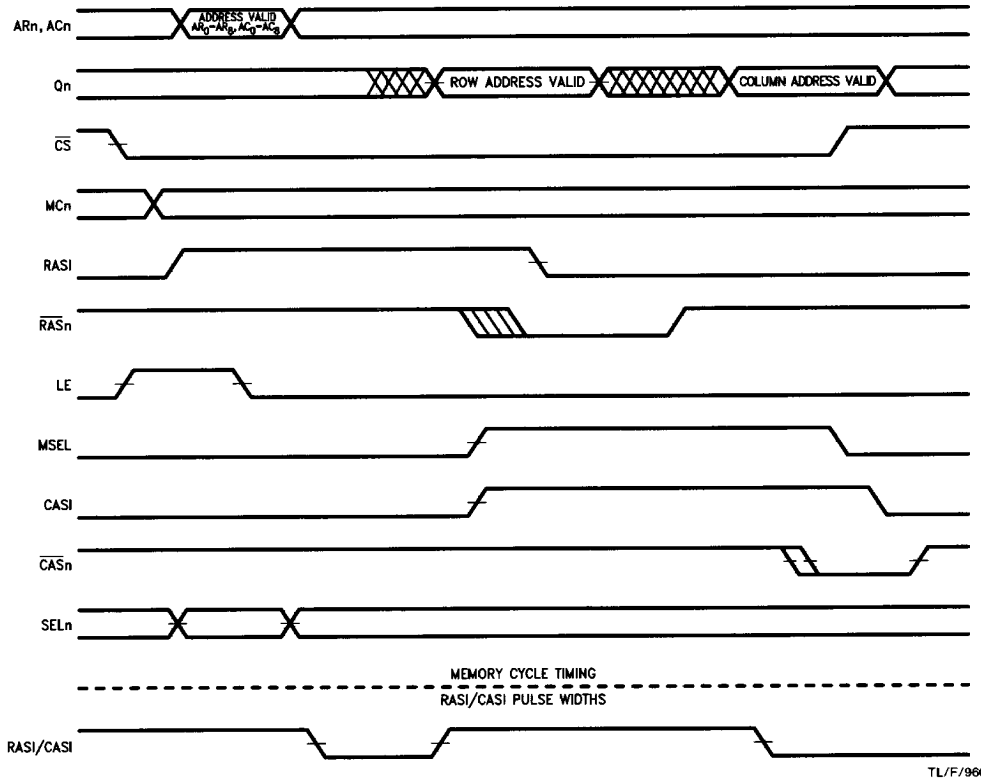
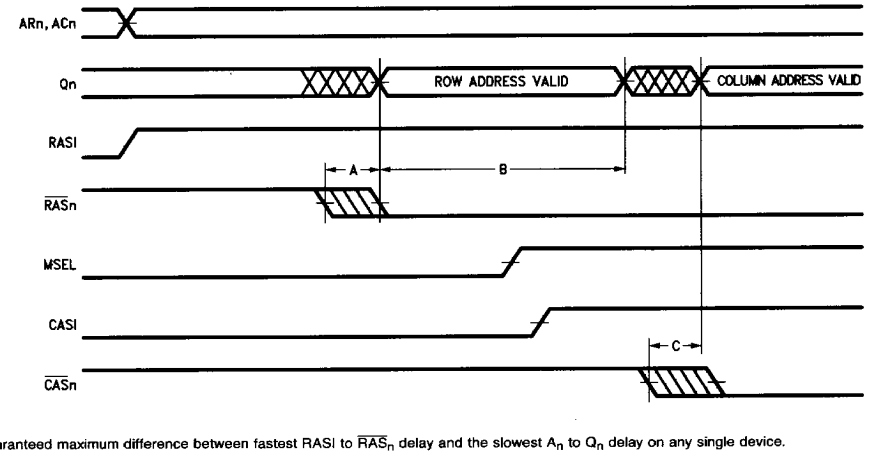


FIGURE 1. Dynamic Memory Controller Timing



Note A: Guaranteed maximum difference between fastest RASI to $\overline{RAS}_n$ delay and the slowest A_n to Q_n delay on any single device.
Note B: Guaranteed maximum difference between fastest MSEL to Q_n delay and the slowest RASI to $\overline{RAS}_n$ delay on any single device.
Note C: Guaranteed maximum difference between fastest CASI to $\overline{CAS}_n$ delay and the slowest MSEL to Q_n delay on any single device.

FIGURE 2. Specifications Applicable to Memory Cycle Timing (MC_n = 1,0)

Timing Waveforms (Continued)

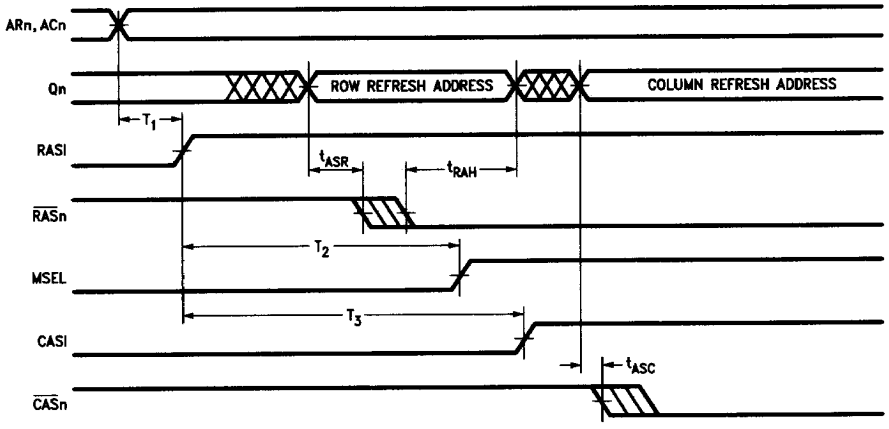


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FIGURE 3. Desired System Timing

Refresh Cycle Timing

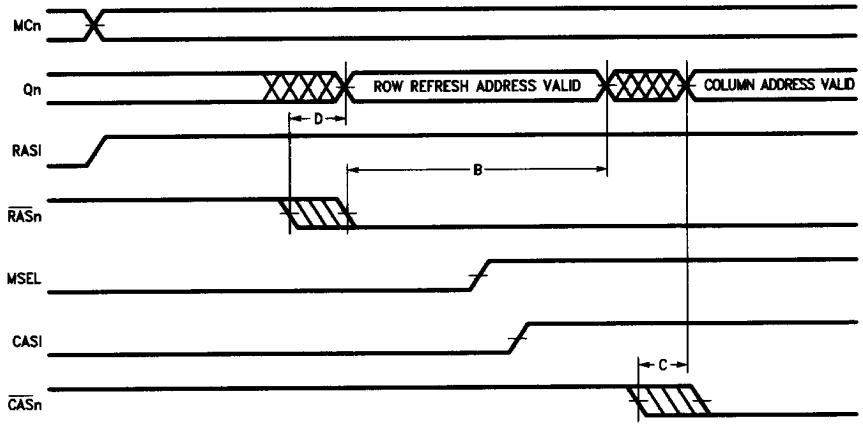

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FIGURE 4. Specifications Applicable to Refresh Cycle Timing (MC_n = 00,01)

Note B: Guaranteed maximum difference between fastest MSEL to Q_n delay and the slowest RASI to $\overline{RAS}_n$ delay on any single device.
Note C: Guaranteed maximum difference between fastest CASI to $\overline{CAS}_n$ delay and the slowest MSEL to Q_n delay on any single device.
Note D: Guaranteed maximum difference between fastest RASI to $\overline{RAS}_n$ delay and the slowest MC_n to Q_n delay on any single device.

Refresh Cycle Timing (Continued)

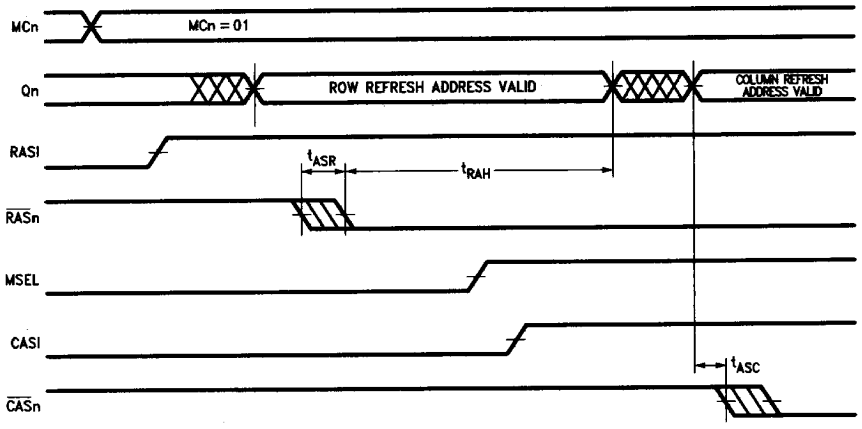

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FIGURE 5. Designed Timing—Refresh with Error Correction

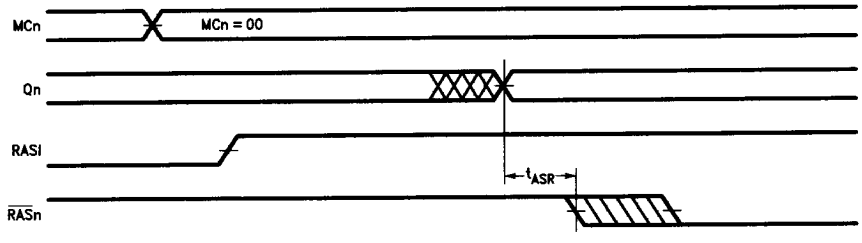

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FIGURE 6. Desired Timing—Refresh without Error Correction

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 1.0 mA
		54F 10% V_{CC}			0.8			I_{OL} = 12.0 mA
		74F 10% V_{CC}			0.5			I_{OL} = 1.0 mA
		74F 10% V_{CC}			0.8			I_{OL} = 12.0 mA
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current				300	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current				300	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current				300	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	29F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$		Military 29F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		Commercial 29F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Commercial 29F $T_A, V_{CC} = Com$ $C_L = 500\ pF$			Units	Fig. No.
		Min	Max	Min	Max	Min	Max	Min	Typ	Max		
t_{PLH}	Propagation Delay	3.0	11.0			2.5	12.0		19.0		ns	2–3
t_{PHL}	AR to Q_n	3.0	11.0			2.5	12.0		22.0			
t_{PLH}	Propagation Delay	3.0	11.0			2.5	12.0		19.0		ns	2–3
t_{PHL}	AC to Q_n	3.0	11.0			2.5	12.0		22.0			
t_{PLH}	Propagation Delay	3.5	12.0			3.0	13.0		23.0		ns	2–3
t_{PHL}	RASI to RAS_i	3.5	12.0			3.0	13.0		20.0			
t_{PLH}	Propagation Delay	1.0	8.0			1.0	8.5		19.0		ns	2–3
t_{PHL}	CASI to CAS_i	1.0	8.0			1.0	8.5		17.0			
t_{PLH}	Propagation Delay	3.0	13.0			2.5	14.0		24.0		ns	2–3
t_{PHL}	MSEL to Q_n	3.0	13.0			2.5	14.0		21.0			
t_{PLH}	Propagation Delay	4.0	15.0			3.5	16.0		25.0		ns	2–3
t_{PHL}	MC_n to Q_n	4.0	15.0			3.5	16.0		22.0			
t_{PLH}	Propagation Delay	3.5	17.5			3.0	18.5		24.0		ns	2–3
t_{PHL}	MC_n to RAS_n	3.5	17.5			3.0	18.5		22.0			
t_{PLH}	Propagation Delay	4.0	12.5			3.5	13.5		23.0		ns	2–3
t_{PHL}	MC_n to CAS_n	4.0	12.5			3.5	13.5		21.0			
t_{PLH}	Propagation Delay	4.0	15.0			3.5	16.0		25.0		ns	2–3
t_{PHL}	LE to RAS_n	4.0	15.0			3.5	16.0		24.0			
t_{PLH}	Propagation Delay	5.0	13.5			4.5	14.5		24.0		ns	2–3
t_{PHL}	LE to CAS_n	5.0	13.5			4.5	14.5		24.0			
t_{PLH}	Propagation Delay	3.5	12.0			3.0	13.0		23.0		ns	2–3
t_{PHL}	LE to Q_n	3.5	12.0			3.0	13.0		22.0			

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	29F T_A = +25°C V_{CC} = +5.0V C_L = 50 pF		Military 29F T_A, V_{CC} = Mil C_L = 50 pF		Commercial 29F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
t_{PZH} t_{PZL}	Output Disable Time OE to Q_n	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2–5
t_{PZH} t_{PZL}	Output Disable Time OE to Q_n	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time OE to RAS_n	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2–5
t_{PZH} t_{PZL}	Output Disable Time OE to RAS_n	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time OE to CAS_n	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2–5
t_{PZH} t_{PZL}	Output Enable Time OE to CAS_n	1.0 1.0	9.5 9.5			1.0 1.0	10.0 10.0	ns	2–5
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CAS_n, RAS_n	15.0 15.0				15.0 15.0		ns	2–4
t_{skew}	Q_n to CAS_n, RAS_n		10.0				10.0	ns	

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	29F T_A = +25°C V_{CC} = +5.0V		Military 29F T_A, V_{CC} = Mil		Commercial 29F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to LE	5.0 5.0				5.0 5.0		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to LE	5.0 5.0				5.0 5.0		ns	2–6
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SEL to LE	5.0 5.0				5.0 5.0		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SEL to LE	5.0 5.0				5.0 5.0		ns	2–6