NATIONAL SEMICOND {LOGIC} 02E D 6501122 0062419 4

54AC/74AC168 • 54AC/74AC169

T-45-23-09

4-Stage Synchronous Bidirectional Counters

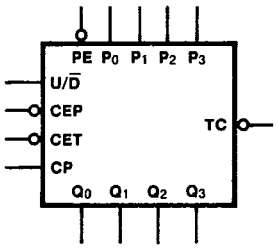
Description

The 'AC168 and 'AC169 are fully synchronous 4-stage up/down counters. The 'AC168 is a BCD decade counter; the 'AC169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

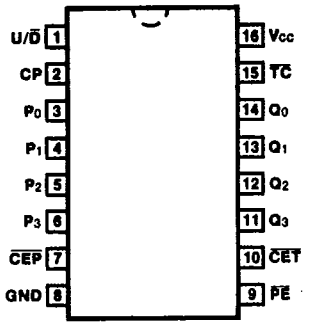
- **Synchronous Counting and Loading**
- **Built-in Lookahead Carry Capability**
- **Presettable for Programmable Operation**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

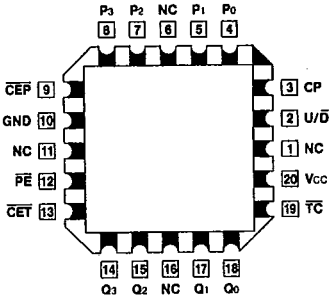
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Pin Names

$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
P_0 - P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up-Down Count Control Input
Q_0 - Q_3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output

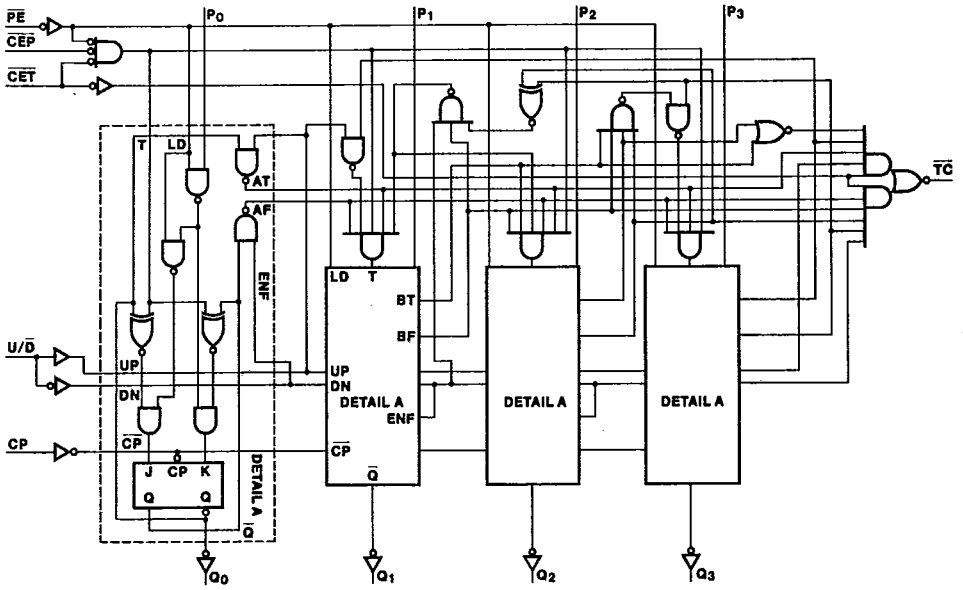
5

NATIONAL SEMICOND {LOGIC} 02E D 6501122 0062420 0

T-45-23-09

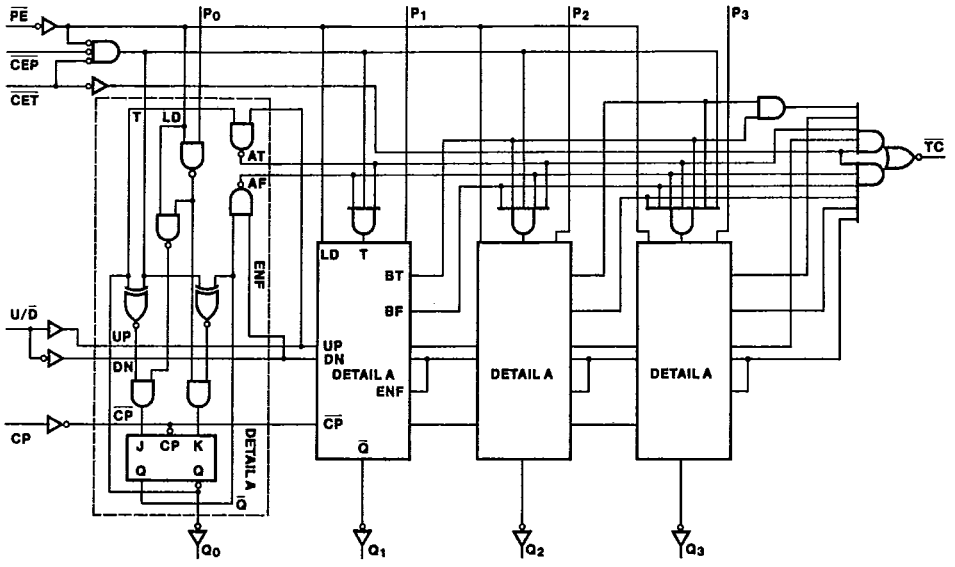
Logic Diagrams

'AC168



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

'AC169



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

NATIONAL SEMICOND {LOGIC} 02E D 6501122 0062421 2

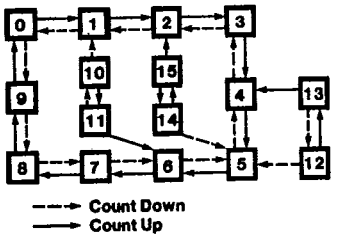
Functional Description

The 'AC168 and 'AC169 use edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the 'AC169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'AC168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

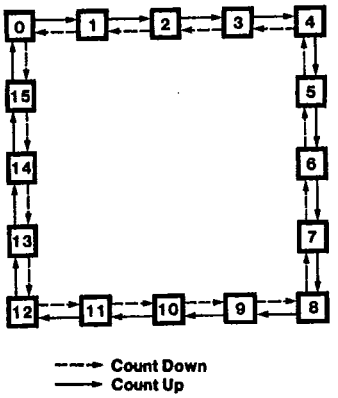
1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
2) Up: ('AC168): $\overline{TC} = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (Up) \cdot \overline{CET}$
   ('AC169): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
3) Down (both): $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (Down) \cdot \overline{CET}$

State Diagrams T-45-23-09

'AC168



'AC169



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Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (P_n to Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC168 $T_A = +25°C$, $C_L = 50$ pF			54AC168 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC168 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		118 154						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		10.5 7.5						ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		13.5 9.5						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		13.5 9.5						ns	3-6
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		11.0 8.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0		10.5 7.5						ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0		9.0 6.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC168 $T_A = +25°C$ $C_L = 50$ pF	54AC168 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC168 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	1.5 0.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5			ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	12.5 9.0			ns	3-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0			ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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5

AC Characteristics

T-45-23-09

Symbol	Parameter	Vcc* (V)	74AC169 $T_A = +25°C$, $C_L = 50$ pF			54AC169 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC169 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	75 100	118 154		55 75		65 90		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.0	9.5 7.0	13.0 10.0	1.0 1.0	16.0 12.0	1.0 1.0	14.5 11.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.0	10.5 7.5	14.5 11.0	1.0 1.0	17.5 13.0	1.0 1.0	16.0 12.0	ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	1.0 1.0	13.5 9.5	18.0 13.0	1.0 1.0	22.5 16.0	1.0 1.0	22.0 14.0	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	1.0 1.0	13.5 9.5	18.0 13.0	1.0 1.0	23.0 16.0	1.0 1.0	20.5 14.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	11.0 8.0	15.0 10.5	1.0 1.0	18.5 13.0	1.0 1.0	16.5 12.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	9.5 7.0	12.5 9.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 10.0	ns	3-6
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	11.0 8.0	15.0 10.5	1.0 1.0	19.0 13.5	1.0 1.0	17.0 12.0	ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	10.0 7.0	13.5 9.5	1.0 1.0	17.0 12.0	1.0 1.0	15.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC169 $T_A = +25°C$ $C_L = 50$ pF		54AC169 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC169 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5	4.5 2.5	6.0 3.0	5.0 2.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	1.5 0.5	0.5 1.5	0.5 1.5	0.5 1.5	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5	10.5 7.0	14.0 9.0	12.5 8.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0	0 0.5	0.5 1.0	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0	10.0 6.5	13.5 9.0	12.0 8.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0	0 0.5	0.5 1.0	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0	5.5 3.5	7.0 4.5	6.5 4.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5	0 0.5	0 0.5	0 0.5	ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	7.0 4.5	10.0 6.5	13.0 8.5	11.5 7.5	ns	3-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0	0 0.5	0 0.5	0 0.5	ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	3.0 3.0	5.0 5.0	4.0 3.0	ns	3-6

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Capacitance

Symbol	Parameter	54/74AC	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5 V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.5 V