| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Technical and editorial changes throughout. | 92-04-17 | M. L. Poelking |
| B | Change boilerplate to add QML class V criteria. Add ground bounce immunity characterization. Editorial changes throughout. | 97-05-15 | T.M. Hess |
| C | Add RHA limits - jak. | 98-05-29 | Monica L. Poelking |

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | C | C | C | C | C | C | C | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | 20 | 21 | | | | | | | | | | | | |
| REV STATUS OF SHEETS | REV | | | C | C | C | C | C | C | C | C | C | C | C | C | C | C | C | |
| | SHEET | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | |

PMIC N/A

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DRAWING APPROVAL DATE
90-10-02

REVISION LEVEL
C

**DEFENSE SUPPLY CENTER COLUMBUS**

**COLUMBUS, OHIO 43216**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

# MICROCIRCUITS, DIGITAL, ADVANCED CMOS, OCTAL D-TYPE FLIP-FLOP WITH RESET, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | 67268 | **5962-89735** |

SHEET 1 OF 21

DSCC FORM 2233
APR 97

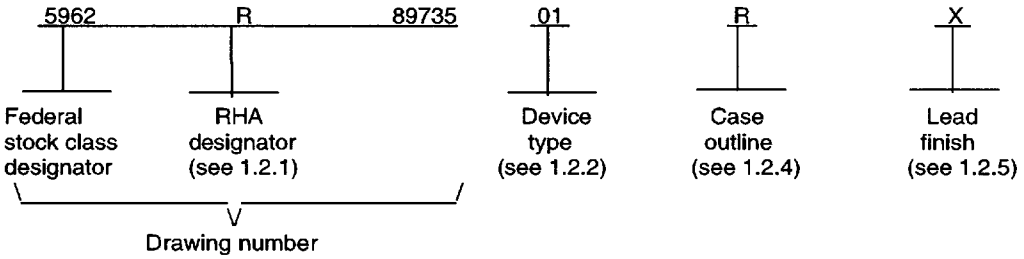
5962-E342-98

1. SCOPE

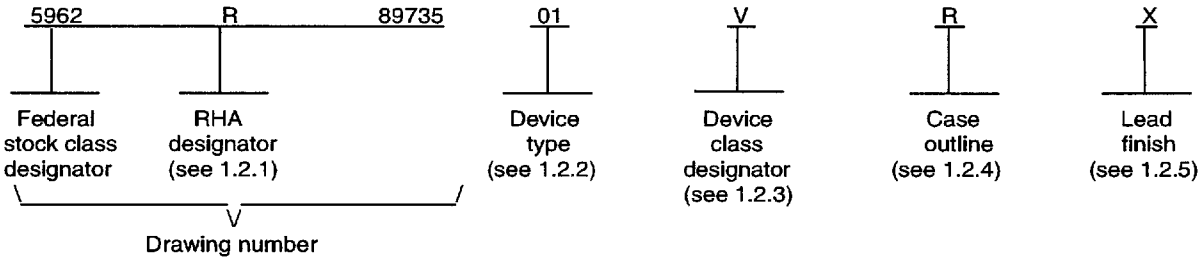
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples:

For device classes M and Q:




For device class V:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54ACTQ273 | Octal D type flip-flop with reset, TTL compatible inputs |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| R | GDIP1-T20 or CDIP2-T20 | 20 | Dual-in-line |
| S | GDFP2-F20 or CDFP3-F20 | 20 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range ($V_{CC}$) ..... -0.5 V dc to +6.0 V dc
DC input voltage range ($V_{IN}$) ..... -0.5 V dc to $V_{CC}$ + 0.5 V dc
DC output voltage range ($V_{OUT}$) ..... -0.5 V dc to $V_{CC}$ + 0.5 V dc
DC input diode current ..... ±20 mA
DC output diode current (per output pin) ..... ±50 mA
DC output source or sink current (per output pin) ..... ±50 mA
DC $V_{CC}$ or GND current ..... ±100 mA
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation ($P_D$) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case ($\Theta_{JC}$) ..... See MIL-STD-1835
Junction temperature ($T_J$) ..... +175°C 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range ($V_{CC}$) ..... +4.5 V dc to +5.5 V dc
Input voltage range ($V_{IN}$) ..... +0.0 V dc to $V_{CC}$
Output voltage range ($V_{OUT}$) ..... +0.0 V dc to $V_{CC}$
Case operating temperature range ($T_C$) ..... -55°C to +125°C
Maximum Input rise and fall rate ($\Delta t/\Delta v$) ..... 8 ns/V
Minimum high level input voltage ($I_{OH}$) ..... -24 mA
Maximum low level output current ($I_{OL}$) ..... +24 mA
Maximum frequency, ($f_{max}$):
  $T_C$ = +25°C:
    $V_{CC}$ = 4.5 V to 5.5 V ..... 95 MHz
  $T_C$ = -55°C, +125°C:
    $V_{CC}$ = 4.5 V to 5.5 V ..... 85 MHz
Minimum setup time,Dn to CP ($t_s$):
  $T_C$ = +25°C:
    $V_{CC}$ = 4.5 V to 5.5 V ..... 5.0 ns
  $T_C$ = -55°C, +125°C:
    $V_{CC}$ = 4.5 V to 5.5 V ..... 5.0 ns

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55°C to +125°C.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

Maximum hold time, Dn to CP ($t_h$):
$T_C$ = +25°:
$V_{CC}$ = 4.5 V to 5.5 V ..... 2.0 ns
$T_C$ = -55°C, +125°C:
$V_{CC}$ = 4.5 V to 5.5 V ..... 2.0 ns
Maximum clock high, low pulse width ($t_{w1}$):
$T_C$ = +25°C:
$V_{CC}$ = 4.5 V to 5.5 V ..... 5.0 ns
$T_C$ = -55°C, +125°C:
$V_{CC}$ = 4.5 V to 5.5 V ..... 5.0 ns
Maximum pulse width, MR low ($t_{w2}$):
$T_C$ = +25°:
$V_{CC}$ = 4.5 V to 5.5 V ..... 5.0 ns
$T_C$ = -55°C, +125°C:
$V_{CC}$ = 4.5 V to 5.5 V ..... 5.0 ns
Maximum removal time, MR to clock ($t_{rem}$):
$T_C$ = +25°:
$V_{CC}$ = 4.5 V to 5.5 V ..... 4.0 ns
$T_C$ = -55°C, +125°C:
$V_{CC}$ = 4.5 V to 5.5 V ..... 4.0 ns

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) ..... XX percent 1/

1/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

Table I. Electrical performance characteristics.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | | Device type and Device class | $V_{CC}$ | Group A subgroups | Limits 3/ Min | Limits 3/ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| High level output voltage 3006 | $V_{OH}$ 4/ 5/ | For all inputs affecting output under test, $V_{IN}$ = 2.0 V or 0.8 V | | All<br>All | 4.5 V | 1, 2, 3 | 4.4 | | V |
| | | For all other inputs, $V_{IN} = V_{CC}$ or GND | | All<br>All | 5.5 V | 1, 2, 3 | 5.4 | | |
| | | $I_{OH}$ = -50 µA | M, D, L, R | All<br>All | 5.5 V | 1 | 5.4 | | |
| | | For all inputs affecting output under test, $V_{IN}$ = 2.0 V or 0.8 V | | All<br>All | 4.5 V | 1 | 3.86 | | |
| | | For all other inputs, $V_{IN} = V_{CC}$ or GND | M, D, L, R | All<br>All | 4.5 V | 1 | 3.86 | | |
| | | $I_{OH}$ = -24 mA | | All<br>All | 4.5 V | 2, 3 | 3.7 | | |
| | | | | All<br>All | 5.5 V | 1 | 4.86 | | |
| | | | | All<br>All | 5.5 V | 2, 3 | 4.7 | | |
| | | For all inputs affecting output under test, $V_{IN}$ = 2.0 V or 0.8 V | | All<br>All | 5.5 V | 1, 2, 3 | 3.85 | | |
| | | For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH}$ = -50 mA 6/ | M, D, L, R | All<br>All | 5.5 V | 1 | 3.85 | | |
| Low level output voltage 3007 | $V_{OL}$ 4/ 5/ | For all inputs affecting output under test, $V_{IN}$ = 2.0 V or 0.8 V | | All<br>All | 4.5 V | 1, 2, 3 | | 0.1 | V |
| | | For all other inputs, $V_{IN} = V_{CC}$ or GND | | All<br>All | 5.5 V | 1, 2, 3 | | 0.1 | |
| | | $I_{OL}$ = 50 µA | M, D, L, R | All<br>All | 5.5 V | 1 | | 0.1 | |
| | | For all inputs affecting output under test, $V_{IN}$ = 2.0 V or 0.8 V | | All<br>All | 4.5 V | 1 | | 0.36 | |
| | | For all other inputs, $V_{IN} = V_{CC}$ or GND | M, D, L, R | All<br>All | 4.5 V | 1 | | 0.36 | |
| | | $I_{OL}$ = 24 mA | | All<br>All | 4.5 V | 2, 3 | | 0.5 | |
| | | | | All<br>All | 5.5 V | 1 | | 0.36 | |
| | | | | All<br>All | 5.5 V | 2, 3 | | 0.5 | |
| | | For all inputs affecting output under test, $V_{IN}$ = 2.0 V or 0.8 V | | All<br>All | 5.5 V | 1, 2, 3 | | 1.65 | |
| | | For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL}$ = 50 mA 6/ | M, D, L, R | All<br>All | 5.5 V | 1 | | 1.65 | |

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | Device type and Device class | $V_{CC}$ | Group A subgroups | Limits 3/ Min | Limits 3/ Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Positive input clamp voltage 3022 | $V_{IC+}$ 4/ 5/ | For input under test, $I_{IN} = 18$ mA | All V | 4.5 V | 1, 2, 3 | | 5.7 | V |
| | | M, D, L, R | All V | 4.5 V | 1 | | 5.7 | |
| Negative input clamp voltage 3022 | $V_{IC-}$ 4/ 5/ | For input under test, $I_{IN} = -18$ mA | All V | 4.5 V | 1, 2, 3 | | -1.2 | V |
| | | M, D, L, R | All V | 4.5 V | 1 | | -1.2 | |
| Input leakage current high 3010 | $I_{IH}$ 4/ 5/ | For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND | All All | 5.5 V | 1 | | 0.1 | µA |
| | | M, D, L, R | All All | 5.5 V | 1 | | 0.1 | |
| | | | All All | 5.5 V | 2, 3 | | 1.0 | |
| Input leakage current low 3009 | $I_{IL}$ 4/ 5/ | For input under test, $V_{IN} = GND$ For all other inputs, $V_{IN} = V_{CC}$ or GND | All All | 5.5 V | 1 | | -0.1 | µA |
| | | M, D, L, R | All All | 5.5 V | 1 | | -0.1 | |
| | | | All All | 5.5 V | 2, 3 | | 1.0 | |
| Input capacitance 3012 | $C_{IN}$ | See 4.4.1c $T_C = +25°C$ | All All | GND | 4 | | 10 | pF |
| Power dissipation capacitance | $C_{PD}$ 7/ | See 4.4.1c $T_C = +25°C$ | All All | 5.0 V | 4 | | 55 | pF |
| Quiescent supply current delta, TTL input level 3005 | $\Delta I_{CC}$ 4/ 5/ 8/ | For input under test, $V_{IN} = V_{CC} - 2.1$ V For all other inputs, $V_{IN} = V_{CC}$ or GND | All All | 5.5 V | 1 | | 1.0 | mA |
| | | | | | 2, 3 | | 1.6 | |
| | | M, D | All | 5.5 V | 1 | | 1.6 | |
| | | L, R | All | | | | 3.5 | |
| Quiescent supply current, output high 3005 | $I_{CCH}$ 4/ 5/ | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0.0$ A | All All | 5.5 V | 1 | | 4.0 | µA |
| | | | | | 2, 3 | | 80.0 | |
| | | M | All All | 5.5 V | 1 | | 100 | |
| | | D | | | | | 1.0 | mA |
| | | L, R | | | | | 3.5 | |
| Quiescent supply current, output low 3005 | $I_{CCL}$ 4/ 5/ | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0.0$ A | All All | 5.5 V | 1 | | 4.0 | µA |
| | | | | | 2, 3 | | 80.0 | |
| | | M | All All | 5.5 V | 1 | | 100.0 | |
| | | D | | | | | 1.0 | mA |
| | | L, R | | | | | 3.5 | |

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | Device type and Device class | $V_{CC}$ | Group A subgroups | Limits 3/ Min | Limits 3/ Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Low level ground bounce noise | $V_{OLP}$ 9/ | $V_{IH} = 3.0\ V$, $V_{IL} = 0.0\ V$<br>$T_A = +25°C$<br>See 4.4.1d<br>See figure 4 | All<br>All | 5.0 V | 4 | | 1500 | mV |
| | $V_{OLV}$ 9/ | | | | 4 | | -1200 | |
| High level $V_{CC}$ bounce noise | $V_{OHP}$ 9/ | | | 5.0 V | 4 | | $V_{OH}$ +1200 | mV |
| | $V_{OHV}$ 9/ | | | | 4 | | $V_{OH}$ -2200 | |
| Functional tests 3014 | 4/ 5/ 10/ | $V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$<br>See 4.4.1b | All<br>All | 4.5 V | 7, 8 | L | H | |
| | | Verify output $V_{OUT}$ M, D, L, R | All<br>All | | 7 | L | H | |
| | | | All<br>All | 5.5 V | 7, 8 | L | H | |
| Latch-up input/output over-voltage | $I_{CC}$ (O/V1) 11/ | $t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$<br>$5\ \mu s \le t_r \le 5\ ms$<br>$5\ \mu s \le t_f \le 5\ ms$<br>$V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$<br>$V_{over} = 10.5\ V$<br>See 4.4.1e | All<br>V | 5.5 V | 2 | | 200 | mA |
| Latch-up input/output positive over-current | $I_{CC}$ (O/I1+) 11/ | $t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$<br>$5\ \mu s \le t_r \le 5\ ms$<br>$5\ \mu s \le t_f \le 5\ ms$<br>$V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$<br>$I_{trigger} = +120\ mA$<br>See 4.4.1e | All<br>V | 5.5 V | 2 | | 200 | mA |
| Latch-up input/output negative over-current | $I_{CC}$ (O/I1-) 11/ | $t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$<br>$5\ \mu s \le t_r \le 5\ ms$<br>$5\ \mu s \le t_f \le 5\ ms$<br>$V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$<br>$I_{trigger} = -120\ mA$<br>See 4.4.1e | All<br>V | 5.5 V | 2 | | 200 | mA |
| Latch-up supply over-voltage | $I_{CC}$ (O/V2) 11/ | $t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$<br>$5\ \mu s \le t_r \le 5\ ms$<br>$5\ \mu s \le t_f \le 5\ ms$<br>$V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$<br>$V_{over} = 9.0\ V$<br>See 4.4.1e | All<br>V | 5.5 V | 2 | | 100 | mA |
| Propagation delay time, CP to Qn 3003 | $t_{PHL1}$ 4/ 5/ 12/ | $C_L = 50\ pF$ minimum<br>$R_L = 500\Omega$<br>See figure 5 | All<br>All | 4.5 V | 9 | 1.0 | 9.0 | ns |
| | | M, D, L, R | All<br>All | | 9 | 1.0 | 9.0 | |
| | | | All<br>All | | 10, 11 | 1.0 | 10.0 | |

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | | Device type and Device class | $V_{CC}$ | Group A subgroups | Limits 3/ Min | Limits 3/ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time, CP to Qn 3003 | $t_{PLH1}$ 4/ 5/ 12/ | $C_L$ = 50 pF minimum<br>$R_L$ = 500Ω<br>See figure 5 | M, D, L, R | All<br>All | 4.5 V | 9 | 1.0 | 9.0 | ns |
| | | | | All<br>All | | 9 | 1.0 | 9.0 | |
| | | | | All<br>All | | 10, 11 | 1.0 | 10.0 | |
| Propagation delay time, MR to Qn 3003 | $t_{PHL2}$ 4/ 5/ 12/ | $C_L$ = 50 pF minimum<br>$R_L$ = 500Ω<br>See figure 5 | M, D, L, R | All<br>All | 4.5 V | 9 | 1.0 | 9.5 | ns |
| | | | | All<br>All | | 9 | 1.0 | 9.5 | |
| | | | | All<br>All | | 10, 11 | 1.0 | 11.0 | |

1/ For tests not listed in the referenced MIL-STD-883, (e.g. ΔICC), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except for the $I_{CC}$ and $\Delta I_{CC}$ tests, the output terminal shall be open. When performing the $I_{CC}$ and $\Delta I_{CC}$ tests, the current meter shall be placed in the circuit such that all current flows through the meter.

Additional detailed information on qualified devices (i.e. pin for pin conditions and testing sequence) is available from the qualifying activity (DCSS-VQC) upon request.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at $+4.5\ V \le V_{CC} \le +5.5\ V$.

4/ RHA samples do not have to be tested at -55°C and +125°C prior to irradiation.

5/ When performing post irradiation electrical measurements for RHA level, $T_A$ = +25°C. Limits shown are guaranteed at $T_A$ = +25°C ±5°C.

6/ Transmission driving tests are performed at $V_{CC}$ = 5.5 V with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN}$ = 2.0 V or 0.8 V.

7/ Power dissipation capacitance ($C_{PD}$) determines the no load power consumption, $P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})\ f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$. The dynamic current consumption, $I_S = (C_{PD} + C_L)\ V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$. For both $P_D$ and $I_S$, n is the number of device inputs at TTL levels, f is the frequency of the input signal, d is the duty cycle of the input signal, and $C_L$ is the output load capacitance.

8/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.

Table I. Electrical performance characteristics - Continued.

9/ This test is for qualification only. Ground and $V_{CC}$ bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested that, whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from $V_{CC}$ to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and $V_{CC}$ bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal $V_{OH}$ level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at $V_{OH}$ as all other outputs possible are switched from $V_{OH}$ to $V_{OL}$. $V_{OHV}$ and $V_{OHP}$ are then measured from the nominal $V_{OH}$ level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from $V_{OL}$ to $V_{OH}$.

The device inputs shall be conditioned such that all outputs are at a low nominal $V_{OL}$ level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at $V_{OL}$ as all other outputs possible are switched from $V_{OL}$ to $V_{OH}$. $V_{OLP}$ and $V_{OLV}$ are then measured from the nominal $V_{OL}$ level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from $V_{OH}$ to $V_{OL}$.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, $V_{IL} = 0.4$ V and $V_{IH} = 2.4$ V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

11/ See JEDEC STD. 17 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$ and $V_{over}$, are to be accurate within ±5 percent.

12/ AC limits at $V_{CC} = 5.5$ V are equal to limits at $V_{CC} = 4.5$ V and guaranteed by testing at $V_{CC} = 4.5$ V. Minimum AC limits for $V_{CC} = 5.5$ V are 1.0 ns and guaranteed by guardbanding the $V_{CC} = 4.5$ V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

| Device type | 01 |
|---|---|
| Case outlines | R, S, and 2 |
| Terminal number | Terminal symbol |
| 1 | $\overline{MR}$ |
| 2 | Q0 |
| 3 | D0 |
| 4 | D1 |
| 5 | Q1 |
| 6 | Q2 |
| 7 | D2 |
| 8 | D3 |
| 9 | Q3 |
| 10 | GND |
| 11 | CP |
| 12 | Q4 |
| 13 | D4 |
| 14 | D5 |
| 15 | Q5 |
| 16 | Q6 |
| 17 | D6 |
| 18 | D7 |
| 19 | Q7 |
| 20 | $V_{CC}$ |

| Pin description | |
|---|---|
| Terminal symbol | Description |
| Dn (n = 0 to 7) | Data inputs |
| Qn (n = 0 to 7) | Data outputs |
| $\overline{MR}$ | Master reset input (active low) |
| CP | Clock pulse input |

FIGURE 1. Terminal connections.

| Device type 01 | | | |
|---|---|---|---|
| Inputs | | | Outputs |
| $\overline{MR}$ | CP | Dn | Qn |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | Q0 |

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Transition from low to high level
Q0 = The level of Q before the indicated steady-state input conditions were established

FIGURE 2. Truth table.

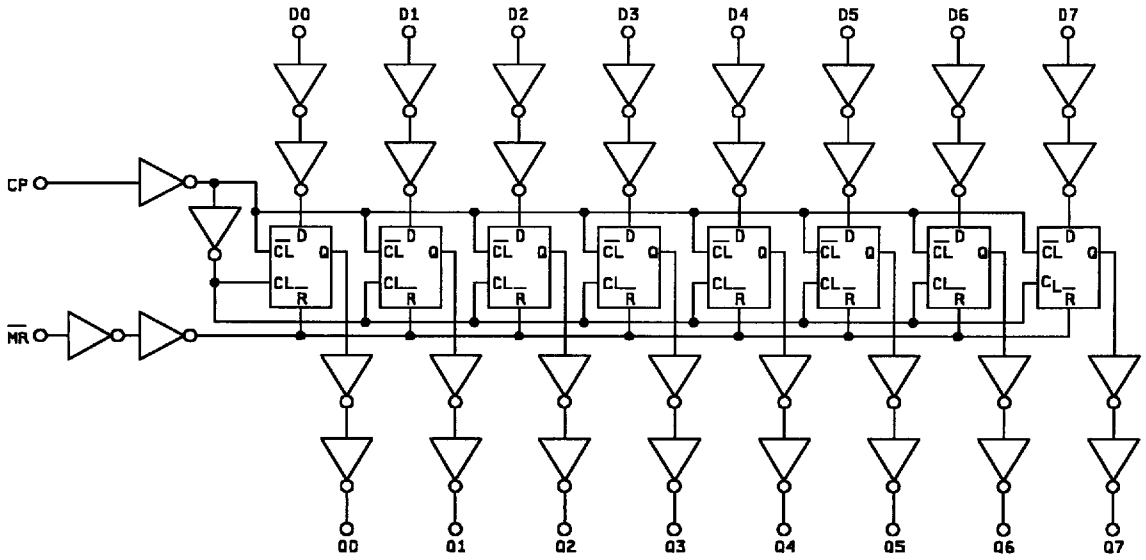
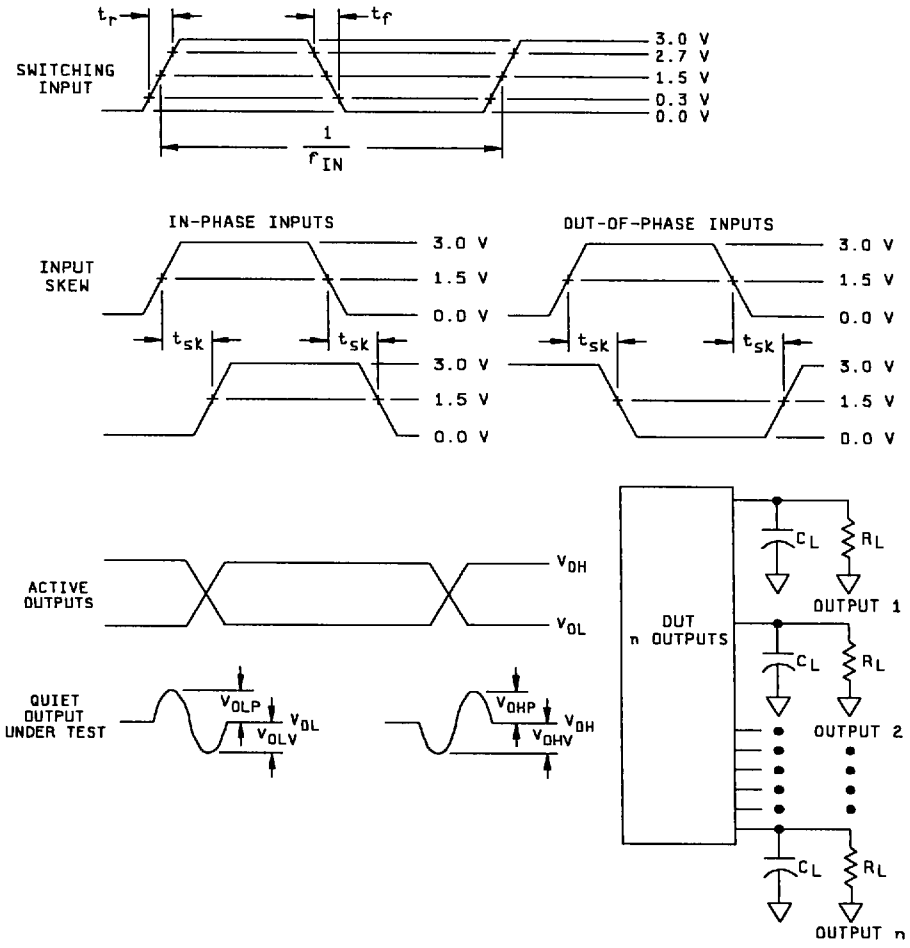



FIGURE 3. Logic diagram.




NOTES:

1. $C_L$= includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. $R_L$= 450Ω ± 1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. $V_{IN}$ = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. $t_r$, $t_f$ = 3 ns ±1.0 ns. For input signal generators incapable of maintaining these values of $t_r$ and $t_f$, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching input signals ($t_{sk}$): ≤ 250ps.

FIGURE 4. Ground bounce load circuit and waveforms.

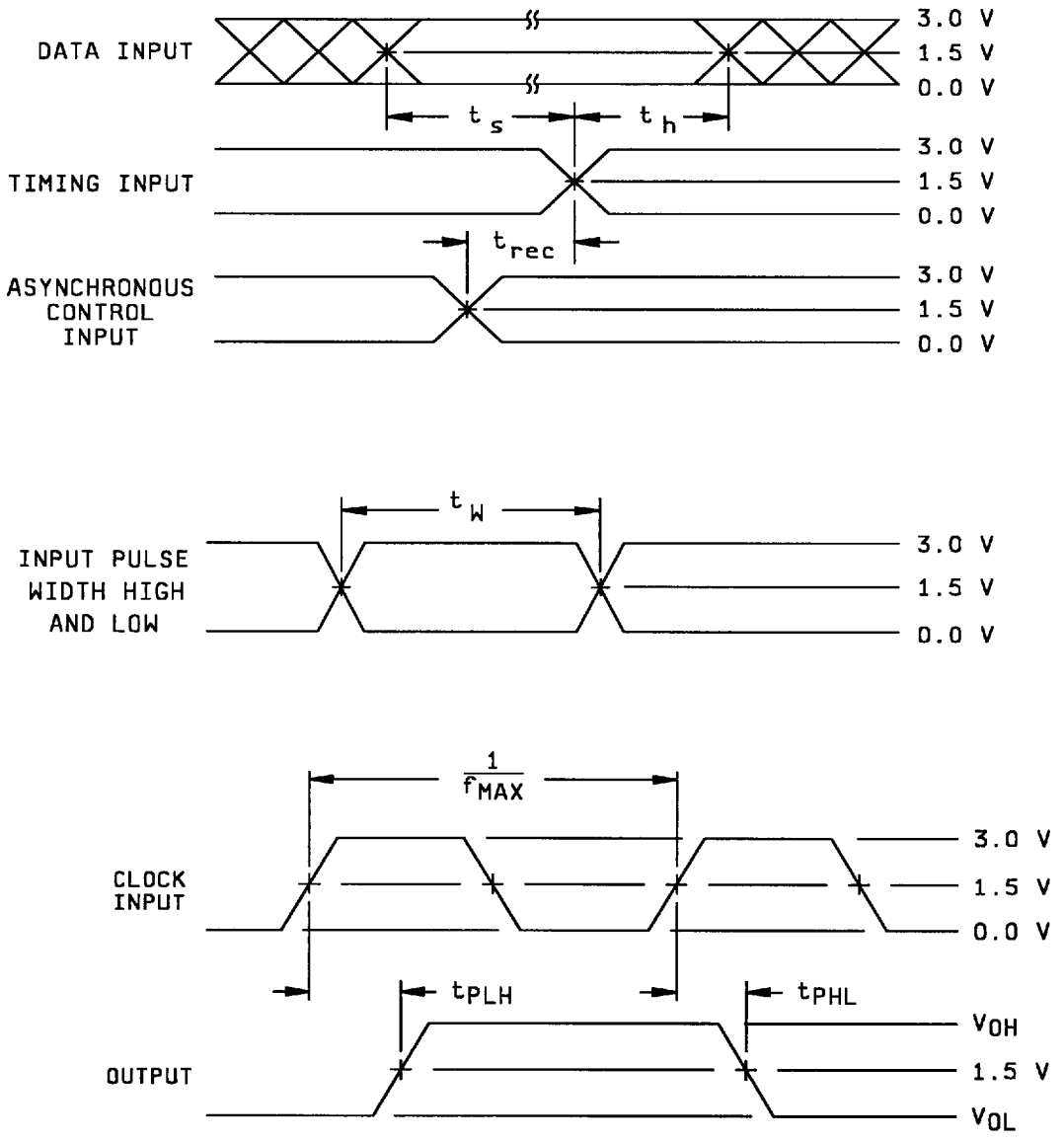
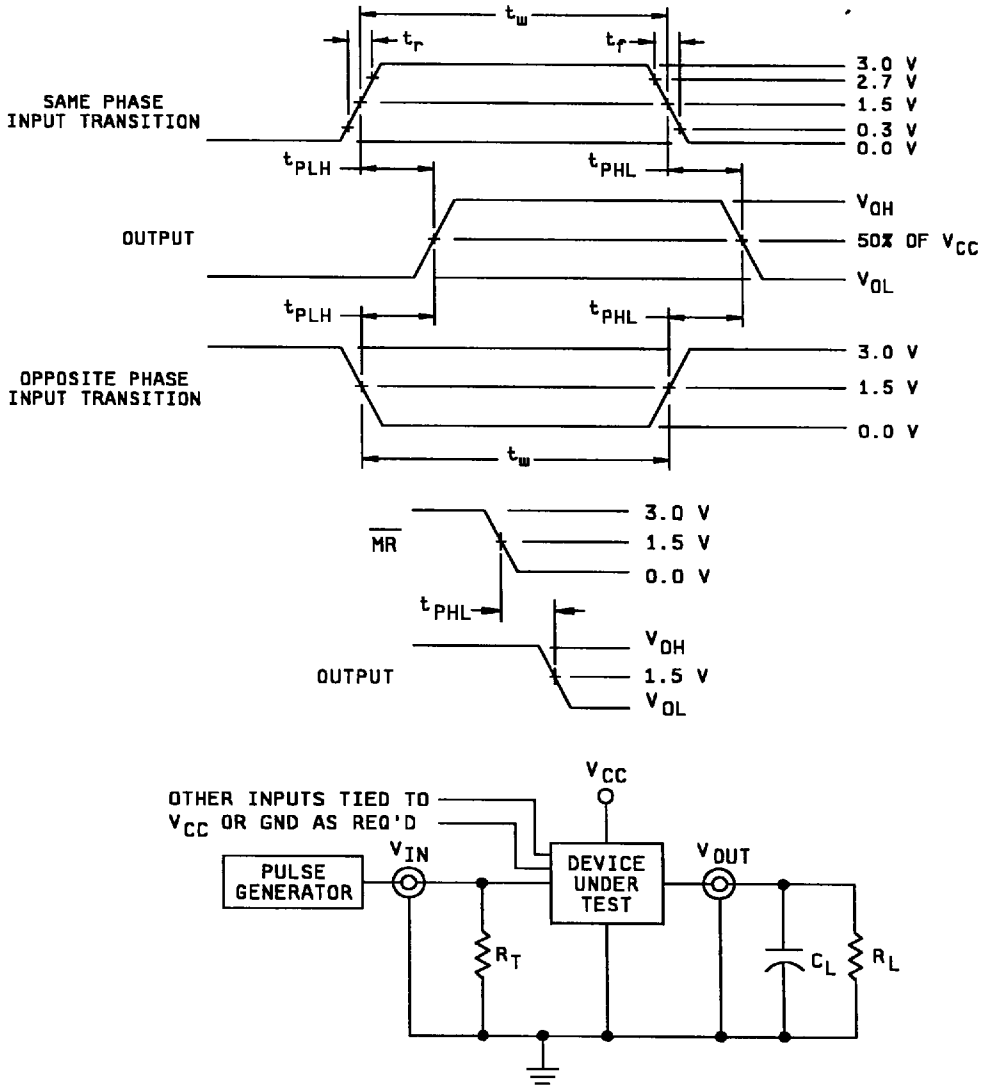



FIGURE 5. Switching waveforms and test circuit.




NOTES:

1. $C_L$ = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. $R_T$ = 50Ω or equivalent, $R_L$ = 500Ω or equivalent.
3. Input signal from pulse generator: $V_{IN}$ = 0.0 V to 3.0 V; PRR ≤ 10 MHz; $t_r$ ≤ 3.0 ns; $t_f$ ≤ 3.0ns; $t_r$ and $t_f$ shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 Mhz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit - Continued.

4.3.1 Electrostatic discharge sensitivity qualification inspection . Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | 1 | 1 |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 7, 8, 9 | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 2/ 1, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3, 7, 8 | 1, 2, 3, 7, 8 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3, 7, 8 | 1, 2, 3, 7, 8 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein.

c. $C_{IN}$ and $C_{PD}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. For $C_{IN}$ and $C_{PD}$, test all applicable pins on five devices with zero failures.

d. Ground and $V_{CC}$ bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DSCC-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DSCC-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DSCC-VA data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

e. Latch-up tests are required for device class V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. Test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

d. RHA tests for device class M for levels M, D, L, R, F, G, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

e. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, and as specified herein:

Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

1. Inputs tested high, $V_{CC}$ = 5.5 V dc +5%, $R_{CC}$ = 10Ω ±20%, $V_{IN}$ = 5.0 V dc +5%, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

2. Inputs tested low, $V_{CC}$ = 5.5 V dc +5%, $R_{CC}$ = 10Ω ±20%, $V_{IN}$ = 0.0 V dc, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on class M, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end point electrical parameter limits shall be as specified in table I herein and shall be the preirradiation end point electrical parameter limit at 25°C ± 5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-05-29

Approved sources of supply for SMD 5962-89735 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8973501RA | 27014 | 54ACTQ273DMQB |
| 5962-8973501SA | 27014 | 54ACTQ273FMQB |
| 5962-89735012A | 27014 | 54ACTQ273LMQB |
| 5962R8973501RA | 27014 | 54ACTQ273DMQB-R |
| 5962R8973501SA | 27014 | 54ACTQ273FMQB-R |
| 5962R89735012A | 27014 | 54ACTQ273LMQB-R |
| 5962-8973501VRA | 27014 | 54ACTQ273J-QMLV |
| 5962-8973501VSA | 27014 | 54ACTQ273W-QMLV |
| 5962-8973501V2A | 27014 | 54ACTQ273E-QMLV |
| 5962R8973501VRA | 27014 | 54ACTQ273JRQMLV |
| 5962R8973501VSA | 27014 | 54ACTQ273WRQMLV |
| 5962R8973501V2A | 27014 | 54ACTQ273ERQMLV |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 27014 | National Semiconductor<br>2900 Semiconductor Drive<br>P.O. Box 58090<br>Santa Clara, CA 95052-8090<br>Point of contact: 5 Foden Road<br>South Portland, ME 04106 |

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