REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: [signature]

DRAWING APPROVAL DATE: 91-10-03

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, LINEAR, 4TH ORDER ELLIPTIC NOTCH FILTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90968

SHEET 1 OF 17

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

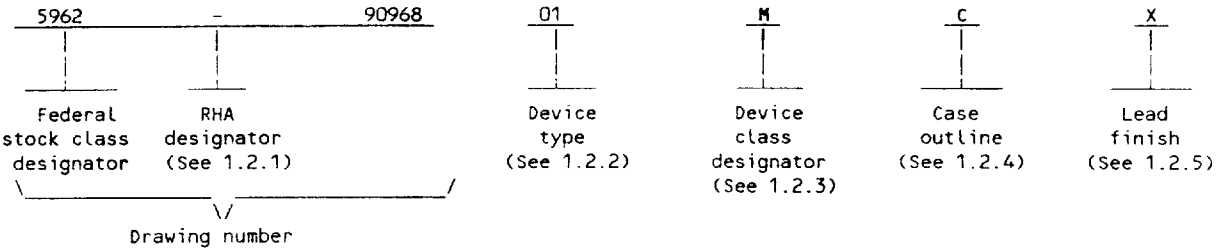
5962-E024

9004708 0007486 257

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LMF90	4th-order elliptic notch filter

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
C	D-1 (14-lead, .785" x .310" x .200"), dual-in-line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage (V^+ to V^-) 2/	-0.3 V to +16 V
Voltage at any input or output 2/	V^- -0.3 V to V^+ +0.3 V
Input current at any pin 3/	5 mA
Package input current (I_{IN}) 3/	20 mA
Power dissipation (P_D)	500 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (Θ_{JA})	59°C/W board mounted

1.4 Recommended operating conditions.

Supply voltage (V^+ to V^-)	4.0 V to 15.0 V
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise specified, all voltages are measured with respect to GND.
3/ When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < V^-$ or $V_{IN} > V^+$), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, $V^+ = +5$ V, $V^- = -5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output offset voltage	V_{OO}	W = D = V^-, R = V^+, f_{CLK} = 167 kHz	1, 2, 3	01	-120	120	mV
		W = D = R = GND, f_{CLK} = 250 kHz			-140	140	
		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz			-170	170	
Supply current	$\pm I_S$	$V_{IN1} = V_{IN2}$ = GND, f_{CLK} = 500 kHz	1, 2, 3		-5	5	mA
Output voltage swing	$+V_{OUT}$	R_L = 5 kΩ	1, 2, 3		4		V
	$-V_{OUT}$					-4	
Logical low input voltage	V_{IN1}	Pins 1, 2, 3, 7, and 10	1, 2, 3			-4.0	
Logical GND input voltage	V_{IN2}	Pins 1, 2, 3, 7, and 10	1, 2, 3		-1.0	1.0	
Logical high input voltage	V_{IN3}	Pins 1, 2, 3, and 7	1, 2, 3		4.0		
Input current	I_{IN}	Pins 1, 2, 3, 7, and 10	1, 2, 3		-10	10	μA
Logical 0 input voltage, pins 5 and 6	V_{IL}	Pin 5, XLS = V^+, or pin 6, XLS = GND 1/	1, 2, 3			-4.0	V
Logical 1 input voltage, pins 5 and 6	V_{IH}	Pin 5, XLS = V^+, or pin 6, XLS = GND 1/	1, 2, 3		4.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions $-55°C \le T_A \le +125°C$, $V^+ = +5$ V, $V^- = -5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
						Min	Max	
Logical 0 input voltage, pin 6		V_{IL}	$V^+ - V^- = 10$ V, XLS = V^- or $V^+ = +5$ V, $V^- = 0$ V, XLS = +2.5 V 1/	1, 2, 3	01		0.8	V
Logical 1 input voltage, pin 6		V_{IH}	$V^+ - V^- = 10$ V, XLS = V^- or $V^+ = +5$ V, $V^- = 0$ V, XLS = +2.5 V 1/	1, 2, 3		2.0		
Logical 0 output voltage, pin 6		V_{OL}	XLS = V^+, $\lvert I_{OUT} \rvert = 4$ mA	1, 2, 3			-4.0	
Logical 1 output voltage, pin 6		V_{OH}	XLS = V^+, $\lvert I_{OUT} \rvert = 4$ mA	1, 2, 3		4.0		
Center frequency range		f_O	2/	4, 5, 6			30	kHz
Clock frequency	Pin 6	f_{CLK}	3/	4, 5, 6			1.5	MHz
	Pins 4 and 5						4.0	
Clock to center frequency ratio		f_{CLK}/f_{O1}	W = D = V^-, R = V^+, f_{CLK} = 167 kHz	4		33.17	33.84	
				5, 6		33	34	
		f_{CLK}/f_{O2}	W = D = R = GND, f_{CLK} = 250 kHz	4		49.75	50.75	
				5, 6		49.5	51	
		f_{CLK}/f_{O3}	W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz	4		99.50	101.51	
				5, 6		99	102	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, $V^+ = +5$ V, $V^- = -5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Passband gain	H_{ON}	DC and 20 kHz, W = D = V^-, R = V^+, f_{CLK} = 167 kHz	4, 5, 6	01	-0.2	0.2	dB
		W = D = R = GND, f_{CLK} = 250 kHz					
		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz					
Ratio of passband width to center frequency	P_{BW}	W = D = V^-, R = V^+, f_{CLK} = 167 kHz	4, 5, 6		0.11	0.145	
		W = D = R = GND, f_{CLK} = 250 kHz			0.24	0.290	
		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz			0.50	0.600	
Gain at center frequency	A_{Min} at f_{01}	W = D = V^-, R = V^+, f_{CLK} = 167 kHz	4, 5, 6			-30	
	A_{Min} at f_{02}	W = D = R = GND, f_{CLK} = 250 kHz				-36.5	
	A_{Min} at f_{03}	W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz				-36.5	
Additional center frequency gain tests at f_{01}		W = GND, R = V^+, f_{CLK} = 167 kHz, D = V^-	4, 5, 6			-30	
		W = V^+, D = V^-, f_{CLK} = 167 kHz, R = V^+					
		W = V^-, D = GND, R = V^+, f_{CLK} = 167 kHz					
		W = D = GND, R = V^+, f_{CLK} = 167 kHz				-35	
		W = V^+, D = GND, R = V^+, f_{CLK} = 167 kHz					

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, $V^+ = +5$ V, $V^- = -5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Additional center frequency gain tests at f_{02}		W = V^-, D = V^-, f_{CLK} = 250 kHz, R = GND	4, 5, 6	01		-30	dB
		W = GND, D = V^-, f_{CLK} = 250 kHz R = GND					
		W = V^+, D = V^-, R = GND, f_{CLK} = 250 kHz					
		W = V^-, D = R = GND, f_{CLK} = 250 kHz					
		W = V^+, D = R = GND, f_{CLK} = 250 kHz				-35	
Additional center frequency gain tests at f_{03}		W = D = R = V^-, f_{CLK} = 500 kHz	4, 5, 6			-30	
		W = GND, D = V^-, f_{CLK} = 500 kHz, R = V^-					
		W = V^+, D = V^-, R = V^-, f_{CLK} = 500 kHz					
		W = V^-, D = GND, R = V^-, f_{CLK} = 500 kHz					
		W = D = GND, R = V^-, f_{CLK} = 500 kHz				-35	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, $V^+ = +5$ V, $V^- = -5$ V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Gain at $f_3 = 0.995f_{01}$ Gain at $f_4 = 1.005f_{01}$	A_{3a} A_{4a}	W = D = V^-, R = V^+, f_{CLK} = 167 kHz	4, 5, 6	01		-30	dB
Gain at $f_3 = 0.992f_{02}$ Gain at $f_4 = 1.008f_{02}$	A_{3b} A_{4b}	W = D = R = GND, f_{CLK} = 250 kHz				-35	
Gain at $f_3 = 0.982f_{03}$ Gain at $f_4 = 1.018f_{03}$	A_{3c} A_{4c}	W = V^+, D = GND, f_{CLK} = 500 kHz, R = V^-				-35	
Passband ripple	A_{max1}	W = D = V^-, R = V^+, f_{CLK} = 167 kHz, $f_5 = 0.914f_{01}$			0	0.9	
		W = D = V^-, R = V^+, f_{CLK} = 167 kHz, $f_6 = 1.094f_{01}$					
	A_{max2}	W = D = R = GND, f_{CLK} = 250 kHz, $f_5 = 0.830f_{02}$					
		W = D = R = GND, f_{CLK} = 250 kHz, $f_6 = 1.205f_{02}$					
	A_{max3}	W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz, $f_5 = 0.700f_{03}$					
		W = V^+, D = GND, R = V^-, f_{CLK} = 500 kHz, $f_6 = 1.428f_{03}$					

1/ Tested indirectly.

2/ Tested inversely.

3/ Maximum clock frequency at pin 6 when testing center frequency range.

Device type	01
Case outline	C
Terminal number	Terminal symbol
1	W
2	R
3	LD
4	XTAL2
5	XTAL1
6	CLK
7	XLS
8	V^-
9	V_{OUT}
10	D
11	V_{IN2}
12	V_{IN1}
13	GND
14	V^+

FIGURE 1. Terminal connections.

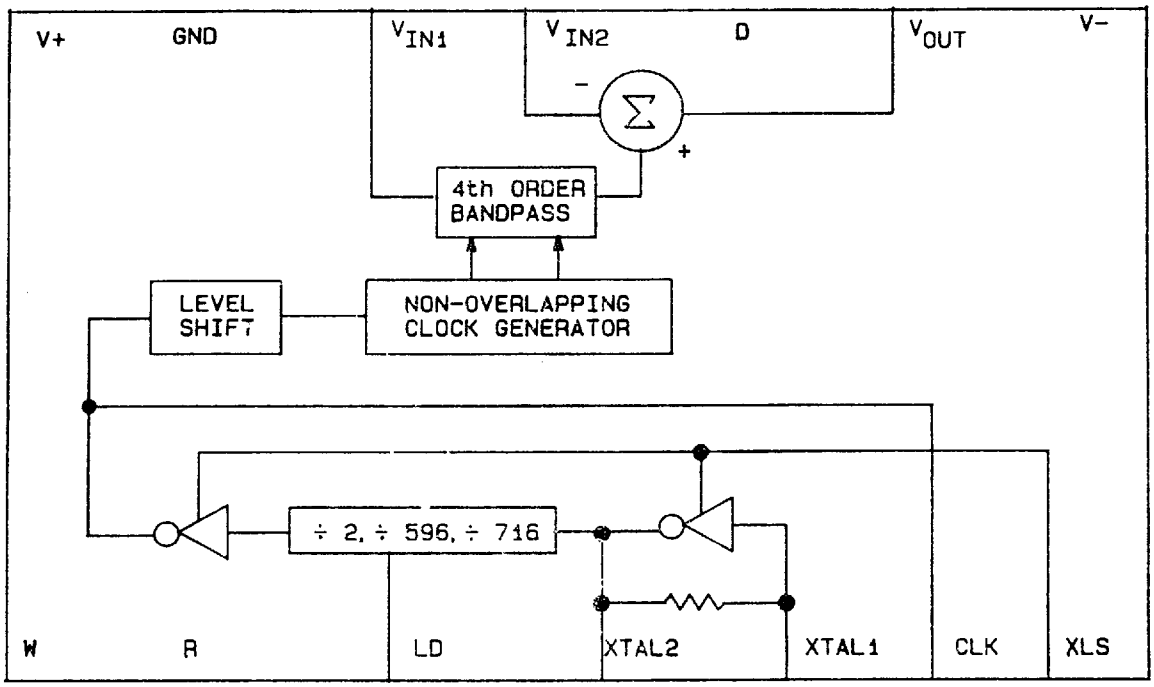


FIGURE 2. Block diagram.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 118 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1				
Final electrical parameters (see 4.2)	1/ 1,2,3,4, 5,6	1/ 1,2,3,4, 5,6	1/ 1,2,3,4, 5,6	1/ 1,2,3,4, 5,6	1/ 1,2,3,4, 5,6
Group A test requirements (see 4.4)	1,2,3,4, 5,6	1,2,3,4, 5,6	1,2,3,4, 5,6	1,2,3,4, 5,6	1,2,3,4, 5,6
Group B end-point electrical parameters (see 4.4)	---	---	1,2,3,4, 5,6	---	1,2,3,4, 5,6
Group C end-point electrical parameters (see 4.4)	1,2,3	1 2/	1	1	1
Group D end-point electrical parameters (see 4.4)	1,2,3	1	1	1	1
Group E end-point electrical parameters (see 4.4)	1,4	1,4	1,4	1,4	1,4

1/ PDA applies to subgroup 1.
2/ Delta limits in accordance with table IIC shall be computed with reference to the previous electrical parameters.

4.4.1 Group A inspection. Tests shall be as specified in table IIA herein.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125° C	100%
Radiographic	2012	100%

TABLE IIC. Delta limits at +25°C.

Parameters 1/	Device types
	All
V_{OO}	±10 percent of specified value in table I
$\pm I_S$	±10 percent of specified value in table I

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.5 Symbols, definitions and functional descriptions.

W (pin 1) — This three-level logic input sets the width of the notch. Notch width is $f_{c2} - f_{c1}$. When W is tied to V^+ (pin 14), GND (pin 13), or V^- (pin 8), the notch width is $0.55f_O$, $0.26f_O$, or $0.127f_O$, respectively.

R (pin 2) — This three-level logic input sets the ratio of the clock frequency (f_{CLK}) to the center frequency (f_O). When R is tied to V^+, GND, or V^-, the clock-to-center-frequency ratio is 33.33:1, 50:1, or 100:1, respectively.

LD (pin 3) — Three three-level logic input sets the division factor of the clock frequency divider. When LD is tied to V^+, GND, or V^-, the division factor is 716, 596, or 2, respectively.

XTAL2 (pin 4) — This is the output of the internal crystal oscillator. When using the internal oscillator, the crystal should be tied between XTAL2 and XTAL1. (The capacitors are internal - no external capacitors are needed for the oscillator to operate.) When not using the internal oscillator this pin should be left open.

XTAL1 (pin 5) — This is the crystal oscillator input. When using the internal oscillator, the crystal should be tied between XTAL1 and XTAL2. XTAL1 can also be used as an input for an external clock signal swinging from V^+ to V^-. The frequency of the crystal or the external clock will be divided internally by the clock divider as determined by the programming voltage on pin 3.

CLK (pin 6) — This the filter clock pin. The clock signal appearing on this pin is the filter clock (f_{CLK}). When using the internal crystal oscillator or an external clock signal applied to pin 5 while pin 7 is tied to V^+, the CLK pin is the output of the divider and can be used to drive other LMF90s with its rail-to-rail output swing. When not using the internal crystal oscillator or an external clock on pin 5, the CLK pin can be used as a CMOS or TTL clock input provided that pin 7 is tied to GND or V^-. For best performance, the duty cycle of a clock signal applied to this pin should be near 50 percent, especially at higher clock frequencies.

XLS (pin 7) — This is a three-level logic pin. When XLS is tied to V^+, the crystal oscillator and frequency divider are enabled and CLK (pin 6) is an output. When XLS is tied to GND (pin 13), the crystal oscillator and frequency divider are disabled and pin 6 is an input for a clock swinging between V^- and V^+. When XLS is tied to V^-, the crystal oscillator and frequency divider are disabled and pin 6 is a TTL level clock input for a clock signal swinging between GND and V^+ or between V^- and GND.

V^- (pin 8) — This the negative power supply pin. It should be bypassed with at least a 0.1 µF capacitor. For single-supply operation, connect this pin to system ground.

V_{OUT} (pin 9) — This is the filter output.

D (pin 10) — This two-level logic input is used to set the depth of the notch (the attenuation at f_0). When D is tied to GND or V^-, the typical notch depth is 48 dB or 39 dB, respectively. Note, however, that the notch depth is also dependent on the width setting (pin 1). See the electrical characteristics for tested limits.

V_{IN2} (pin 11) — This is the input to the difference amplifier section of the notch filter.

V_{IN1} (pin 12) — This is the input to the internal bandpass filter. This pin is normally connected to pin 11. For wide bandwidth applications, an anti-aliasing filter can be inserted between pin 11 and pin 12.

GND (pin 13) — This is the analog ground reference for the LMF90. In split supply applications, GND should be connected to the system ground. When operating the LMF90 from a single positive power supply voltage, pin 13 should be connected to a "clean" reference voltage midway between V^+ and V^-.

V^+ (pin 14) — This is the positive power supply pin. It should be bypassed with at least a 0.1 µF capacitor.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.