Features

- Paged Configurations with Page Reset on Power-Up or $\overline{RST}$ Signal
  - 8 Pages, 16K x 8
- Low Power CMOS Operation
  - 100 μA max. Standby
  - 25 mA max. Active at 5 MHz
- Fast Read Access Time - 150ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP
  - 32-Pad LCC and OTP PLCC
- 5V± 10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100μs/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with 27128, 27513, 27011

1 MEGABIT (8 x 16K [illegible] 8) UV E[illegible]ble [illegible]Page CMOS EP[illegible]OM

Preliminary

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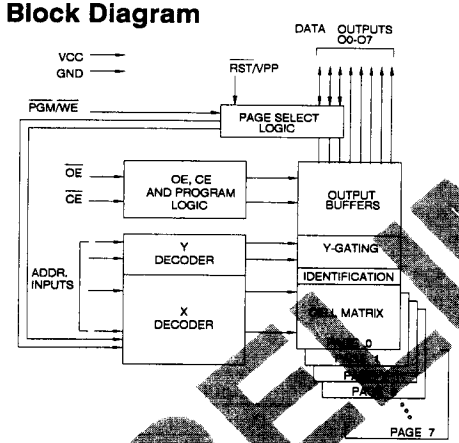
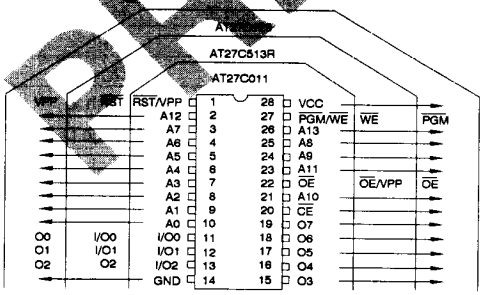
Block Diagram



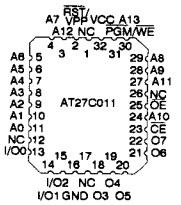
Address Locations	Number of Pages	Bits per Page
[illegible]	[illegible]	131,072

Pin Name	Function
A0-A13	Addresses
O0-O7	Outputs
I/O0-I/O1	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}/\overline{WE}$	Page Write Enable
$\overline{RST}/V_{PP}$	Page Reset
NC	No Connect

Pin Configurations



Note: JEDEC standard pinouts for AT27C513R and AT27C128 are shown for comparison only.



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

Description

The AT27C011 is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). This device requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 150ns, making this part compatible with high performance microprocessor systems by eliminating the need for speed-reducing WAIT states.

The AT27C011 features page mode addressing. Atmel's 27C011 has 8 pages, each organized 16K x 8, and provides a compatible upgrade for existing 128K EPROM based designs. Increased memory capacity and improved system performance can now be easily retrofitted without using costly additional board space.

The AT27C011 has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latches are automatically reset to page 0 upon power-up (resets typically for $V_{CC} \leq 3.8V$) or when $\overline{RST}$/Vpp is brought low (V_{IL}).

Atmel's 1.2 micron scaled CMOS technology provides significantly lower active power consumption than similar NMOS designs. Power consumption is typically only 8mA in Active Mode and less than 20μA in Standby.

The AT27C011 is available in a choice of industry standard JEDEC-approved packages including; 28-pin DIP in ceramic or one time programmable (OTP) plastic, and 32-pad ceramic leadless chip carrier (LCC) or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$,$\overline{OE}$) to give designers the flexibility to prevent bus contention.

With a high density 128K byte storage capability, the AT27C011 allows firmware to be stored reliably and to be quickly accessed by the system without the delays of mass storage media.

The AT27C011 has additional features to ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. Programming time is typically 100μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Page Selection Data [1]

	Page D_{IN}				Page D_{IN}		
Page Selection	**I/O2**	**I/O1**	**I/O0**	**Page Selection**	**I/O2**	**I/O1**	**I/O0**
Select Page 0	V_{IL}	V_{IL}	V_{IL}	Select Page 4	V_{IH}	V_{IL}	V_{IL}
Select Page 1	V_{IL}	V_{IL}	V_{IH}	Select Page 5	V_{IH}	V_{IL}	V_{IH}
Select Page 2	V_{IL}	V_{IH}	V_{IL}	Select Page 6	V_{IH}	V_{IH}	V_{IL}
Select Page 3	V_{IL}	V_{IH}	V_{IH}	Select Page 7	V_{IH}	V_{IH}	V_{IH}

Note: 1. The AT27C011 automatically resets to page 0 whenever $V_{CC} \leq 3.8V$ (typical conditions).

Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$/$\overline{WE}$	$\overline{RST}$/V_{PP}	Ai	V_{CC} [3]	**Outputs**	**I/Oi**
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	V_{CC}	D_{OUT}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X[1]	V_{CC}	High Z	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	High Z	High Z
Rapid Program[2]	V_{IL}	V_{IH}	V_{IL}	V_{PP}	Ai	V_{CC}	D_{IN}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	Ai	V_{CC}	D_{OUT}	D_{OUT}
PGM Inhibit	V_{IH}	X	V_{IH}	V_{PP}	X	V_{CC}	High Z	High Z
Page Select	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{CC} [3]	High Z	Page D_{IN}
Page Reset	X	X	X	V_{IL}	X	V_{CC} [3]	High Z	High Z
Product Identification[5]	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A9=V_H [4] A0=V_{IH} or V_{IL} A1-A13=V_{IL}	V_{CC}	Identification Code	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. Page 0 is automatically selected at power up ($V_{CC} < 3.8V$).
4. $V_H = 12.0 \pm 0.5V$.
5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 w•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

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D.C. and A.C. Operating Conditions for Read and Page Select Operations

		AT27C011			
		-15	-17	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

D.C. and Operating Characteristics for Read and Page Select Operations

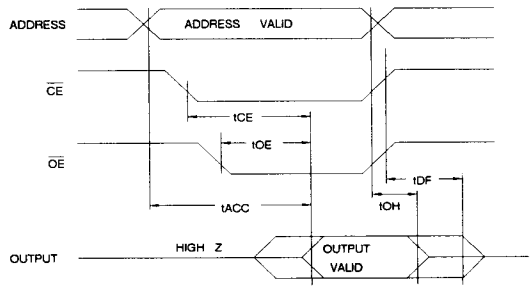
Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V			10	µA
I_{PP1}	$\overline{RST}/V_{PP}$ (1) Read/Standby Current	$\overline{RST}/V_{PP}$ = 3.8 to V_{CC} + 0.3V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC} + 1.0V			100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC} + 1.0V			1	mA
I_{CC}	V_{CC} Active Current	f = 5MHz, I_{OUT} = 0mA, $\overline{CE}$ = V_{IL}	Com.		25	mA
			Ind.,Mil.		30	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100µA		V_{CC}-0.3		V
		I_{OH} = -2.5mA		3.5		V
		I_{OH} = -400µA		2.4		V
V_{CLR}	Page Latch Clear V_{CC} Supply Voltage				4.0	V

Notes: 1. V_{CC} must be applied simultaneously or before $\overline{RST}/V_{PP}$, and removed simultaneously or after $\overline{RST}/V_{PP}$.

A.C. Characteristics for Read Operation

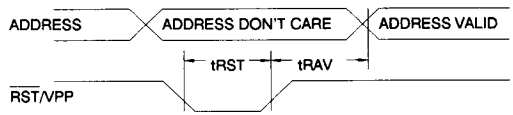
Symbol	Parameter	Condition		AT27C011 -15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{ACC} (4)	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Com.		150		170		200		250	ns
			Ind., Mil.				170		200		250	ns
t_{CE} (3)	$\overline{CE}$ to Output Delay, $\overline{OE} = V_{IL}$				150		170		200		250	ns
t_{OE} (3,4)	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$			65		70		75		100	ns
t_{DF} (2,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Float	$\overline{CE} = V_{IL}$			50		55		55		60	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE} = \overline{OE} = V_{IL}$			0		0		0		0	ns

A.C. Waveforms for Read Operation (1)



Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

A.C. Waveforms for Page Reset Operation



Pin Capacitance (f = 1MHz T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

A.C. Characteristics for Page Select and Page Reset Operations

Symbol	Parameter	Condition	AT27C011 -15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Units
t_{CW} (1)	$\overline{CE}$ to End of Write	$\overline{OE} = V_{IH}$	110		125		145		180		ns
t_{WP} (1)	Write Pulse Width	$\overline{OE} = V_{IH}$	60		70		80		100		ns
t_{WR} (3)	Write Recovery Time		20		20		20		20		ns
t_{DS}	Data Setup Time	$\overline{OE} = V_{IH}$	35		40		45		50		ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	20		20		20		20		ns
t_{CS}	$\overline{CE}$ to Write Setup Time	$\overline{OE} = V_{IH}$	0		0		0		0		ns
t_{WH} (2,3)	$\overline{PGM/WE}$ Low from $\overline{OE}$ High Delay Time		50		50		50		55		ns
t_{RST}	Reset Low Time		150		170		200		250		ns
t_{RAV}	Reset to Address Valid		150		170		200		250		ns

Notes: 1. Writing can be terminated by either $\overline{CE}$ or $\overline{PGM/WE}$ going high after the minimum t_{CW} or t_{WP} requirements have been met.
2. $\overline{OE}$ must be at V_{IH} during a Page Select.
3. This parameter is only sampled and is not 100% tested.

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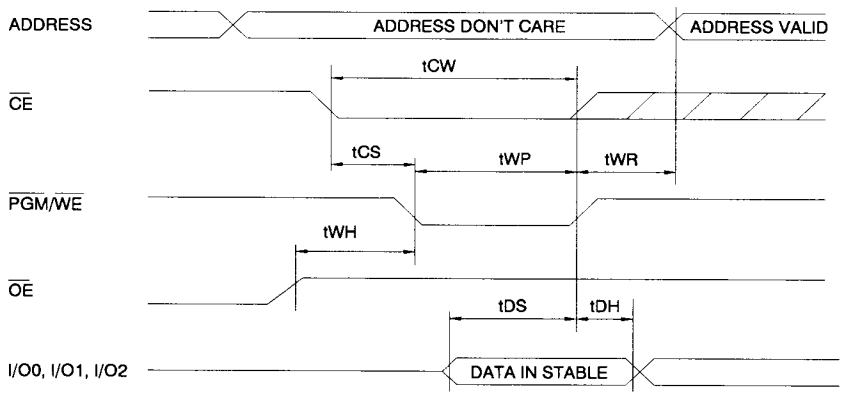
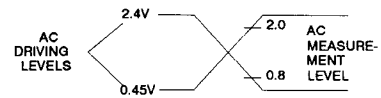
A.C. Waveforms for Page Select Operation

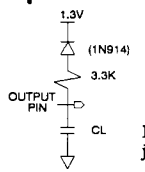


Input Test Waveforms and Measurement Levels



t_R, t_F < 20ns (10% to 90%)

Output Test Load



Note: C_L = 100pF including jig capacitance.

D.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{RST}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions	Limits Min	Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+1$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1mA$		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400\mu A$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	$\overline{RST}/V_{PP}$ Current	$\overline{CE}=\overline{PGM/WE}=V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 0.8V to 2.0V
Output Timing Reference Level ..... 0.8V to 2.0V

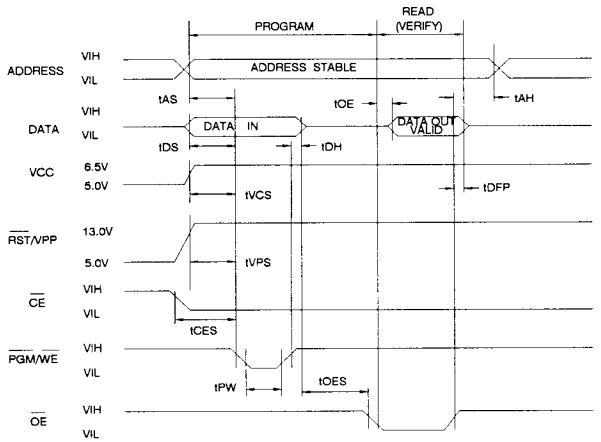
A.C. Programming Characteristics

T_A=25±5°C, V_{CC}=6.5±0.25V, $\overline{RST}/V_{PP}$=13.0±0.25V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Hold Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	$\overline{RST}/V_{PP}$ Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM/WE}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{RST}/V_{PP}$ and removed simultaneously or after $\overline{RST}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100µsec±5%.

Programming Waveforms [1]

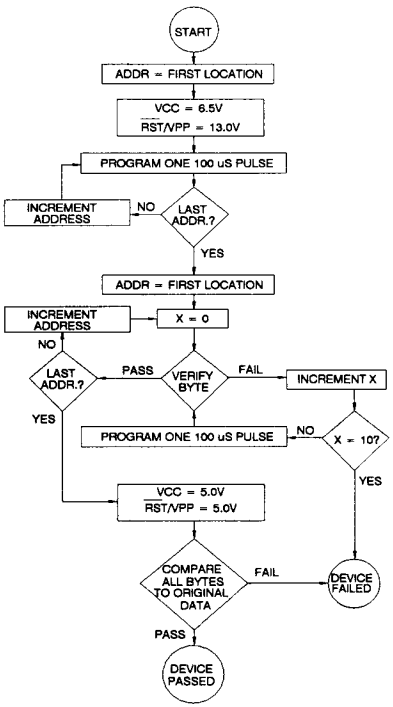


Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{DV} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. The proper page to be programmed must be selected by a page select operation prior to programming the AT27C011.

Rapid Programming Algorithm [1]

A 100μs $\overline{PGM}/\overline{WE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{RST}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 100μs $\overline{PGM}/\overline{WE}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{RST}/V_{PP}$ is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Note: 1. The proper page to be programmed must be selected by a page select operation prior to programming the AT27C011.



Erasure Characteristics

The entire memory array of the AT27C011 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000μW/cm^2 intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W•sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

4

Identification Code:

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	0	1	0	1	85

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	25	0.1	AT27C011-15DC AT27C011-15LC	28DW6 32LW	Commercial (0°C to 70°C)
170	25	0.1	AT27C011-17DC AT27C011-17LC AT27C011-17PC AT27C011-17JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
170	30	0.1	AT27C011-17DI AT27C011-17LI AT27C011-17PI AT27C011-17JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C011-17DM AT27C011-17LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C011-17DM/883 AT27C011-17LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	25	0.1	AT27C011-20DC AT27C011-20LC AT27C011-20PC AT27C011-20JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
200	30	0.1	AT27C011-20DI AT27C011-20LI AT27C011-20PI AT27C011-20JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C011-20DM AT27C011-20LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C011-20DM/883 AT27C011-20LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	25	0.1	AT27C011-25DC AT27C011-25LC AT27C011-25PC AT27C011-25JC	28DW6 32LW 28P6 32J	Commercial (0°C to 70°C)
250	30	0.1	AT27C011-25DI AT27C011-25LI AT27C011-25PI AT27C011-25JI	28DW6 32LW 28P6 32J	Industrial (-40°C to 85°C)
			AT27C011-25DM AT27C011-25LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C011-25DM/883 AT27C011-25LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

	Package Type
28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)