Semiconductor Corporation

CS5481

10-Bit, 20 MHz A/D Converter

Features

- Monolithic 20 MSPS CMOS ADC
  - On-chip Track/Hold
  - On-chip Voltage Reference
  - +5V Power Supply Only
- Dynamic Performance (f_{in}= 1.24 MHz):
  - SNR: 58 dB
  - THD: 63 dB
  - SINAD: 57 dB
- CMOS Outputs
- Analog Input Range:
  - Single-ended Input: $1.2V_{p-p}$
  - Differential Input: $2.4V_{p-p}$
- Low Power: 200 mW

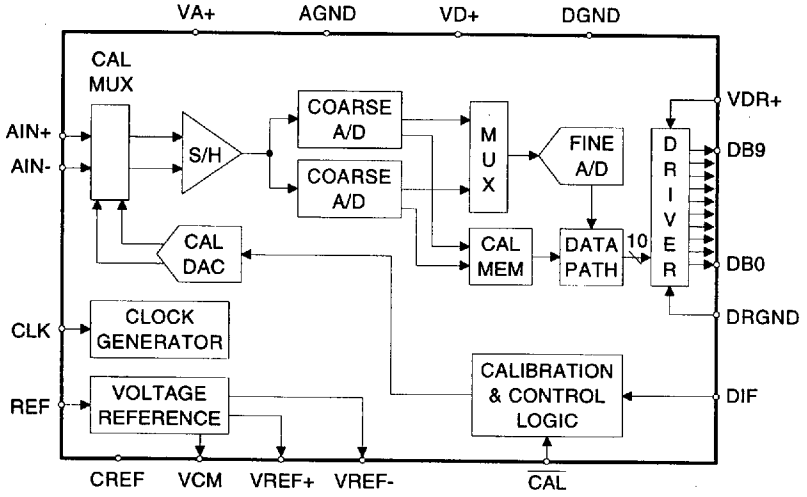
General Description

The CS5481 is a monolithic 10-bit sampling analog-to-digital converter capable of 20 MSPS conversion rate. To achieve high throughput, the CS5481 uses a fully pipelined architecture. Unique self-calibration circuitry ensures excellent linearity with no missing codes over the entire operating temperature range.

Digital inputs are CMOS and TTL compatible. Digital outputs are CMOS compatible. The analog input can be driven by either a differential 2.4 Vp-p signal, or a 1.2 Vp-p single-ended signal. Output data is available in offset binary format.

The CS5481 advanced CMOS construction provides low power consumption and the inherent reliability of monolithic devices.

For more information contact Crystal Semiconductor



Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A=T_{MIN} to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5.0V; AGND=DGND=DRGND1=DRGND2=0V; CLK=20MHz; DIF=VD+; REF=+1.2V; C_L < 10pF)

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-40	-	+85	°C
Resolution		RES	10	-	-	Bits
Accuracy						
Linearity Error	(Note 1)	INL	-	± 1	-	LSB
Differential Linearity	(Note 1)	DNL	-	± 1/2	-	LSB
No Missing Codes	(Note 1)	NMC	10	-	-	Bits
Offset Error	(Note 1)	Vos	-	± 5	-	LSB
Full Scale Error	(Note 1)	FSE	-	± 1	-	% FS
Power Supplies						
DC Power Supply Currents	(Note 2)	IA+ ID+ IDR+	- - -	TBD TBD TBD	TBD TBD TBD	mA mA mA
Power Dissipation	(Note 2)	P_D	-	TBD	200	mW
Power Supply Rejection Ratio	(Note 3)	PSRR	-	70	-	dB
Analog Input						
Input Voltage Range	Single-ended Input Differential Input	AIN	- -	- -	1.2 2.4	V_{p-p} V_{p-p}
Input Capacitance		C_{IN}	-	10	-	pF
Analog Bandwidth		BW	-	200	-	MHz
Common Mode Rejection		CMR	-	40	-	dB
Reference Input						
Input Range		REF	0.6	1.2	1.3	V
Input Impedance		R_L	-	1	-	kΩ

Notes: 1. Applies after calibration at the temperature of interest
2. C_L=10pF typical.
3. f_{in}=1kHz

* Refer to the Specification Definitions immediately following the Pin Description section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*		Symbol	Min	Typ	Max	Units
Dynamic Performance						
Signal-to-(Noise plus Distortion)	(Note 1)	SINAD				
f_{in} = 1.24 MHz			-	57	-	dB
f_{in} = 3.58 MHz			-	56	-	dB
Harmonic Distortion	(Note 1)	THD				
f_{in} = 1.24 MHz			-	63	-	dB
f_{in} = 3.58 MHz			-	63	-	dB
Effective Number of Bits	(Note 1)	ENOB				
f_{in} = 1.24 MHz			-	9.2	-	Bits
f_{in} = 3.58 MHz			-	9.0	-	Bits
Signal-to-Noise	(Note 1)	SNR				
f_{in} = 1.24 MHz			-	58	-	dB
f_{in} = 3.58 MHz			-	56	-	dB
Spurious Free Dynamic Range	(Note 1)	SFDR	-	68	-	dBc
Differential Phase	(Note 1)	DP	-	1	-	°
Differential Gain	(Note 1)	DG	-	1	-	%
Intermodulation Distortion	(Notes 1, 4)	IMD	-	60	-	dB
Overvoltage Recovery Time		t_{ovr}	-	100	-	ns

Note: 4. Tested with input signals of 1MHz and 1.05MHz.

* Refer to the Specitication Definitions immediately following the Pin Description section.

Specitfications are subject to change without notice.

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5V± 5%; AGND=DGND=DRGND1=DRGND2=0V, Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage	V_{OH}	(VD+)-0.3	-	-	V
Low-Level Output Voltage	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{LKG}	-	-	± 10	µA
Digital Input Capacitance	C_{IN}	-	10	-	pF
Digital Output Capacitance	C_{OUT}	-	10	-	pF

RECOMMENDED OPERATING CONDITIONS (AGND, DGND, DRGND1, DRGND2 = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies	Positive Analog	VA+	4.75	5.0	5.25	V
	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Driver	VDR+	4.75	5.0	5.25	V
Analog Input Voltage	Single-ended	AIN	-	-	1.2	V_{p-p}
	Differential		-	-	2.4	V_{p-p}
Reference Voltage		REF	0.6	1.2	1.3	V

ABSOLUTE MAXIMUM RATINGS (AGND, DGND,DRGND1,DRGND2 = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies	Positive Digital	VD+	-0.3	-	6.0	V
	Positive Driver	VDR+	-0.3	-	6.0	V
	Positive Analog	VA+	-0.3	-	6.0	V
Input Current, Any Pin Except Supplies	(Note 5)	I_{in}	-	-	±10	mA
Output Current		I_{out}	-	-	±25	mA
Power Dissipation (Total)	(Note 6)		-	-	500	mW
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage		V_{INL}	-0.3	-	(VL+)+0.3	V
Ambient Operating Temperature		T_A	-55	-	125	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Note: 5. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50mA
6. Total power dissipation, including all input currents and output curents.

WARNING:Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5V± 5%; Input Levels: Logic 0 = 0V, Logic 1 = VL+; C_L <10pF)

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	$1/t_{conv}$	2	-	20	MHz
Clock Duty Cycle		40	-	60	%
Acquisition Time	t_{acq}	-	1	-	CLK
Pipeline Delay	t_{pd}	-	11	-	CLKs
Aperture Delay	t_{apd}	-	3	-	ns
Aperture Jitter	t_{apj}	-	5	-	ps_{rms}
Output Delay	t_{od}	-	10	-	ns
CLK falling to $\overline{CAL}$ falling	t_{sc}	2	-	-	CLKs
Start of Calibration to end of calibration	t_{cal}	-	800,000	-	CLKs

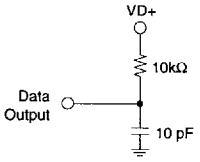


Figure 1. Load Circuit for timing tests

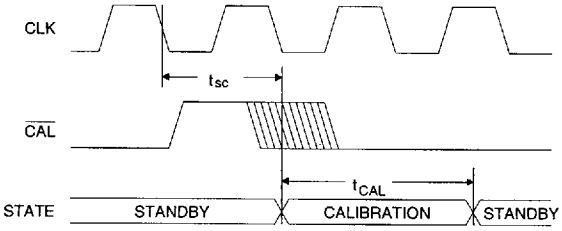


Figure 2. Calibration Timing

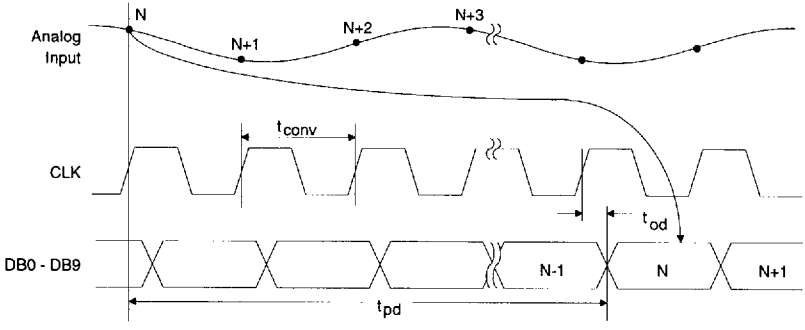
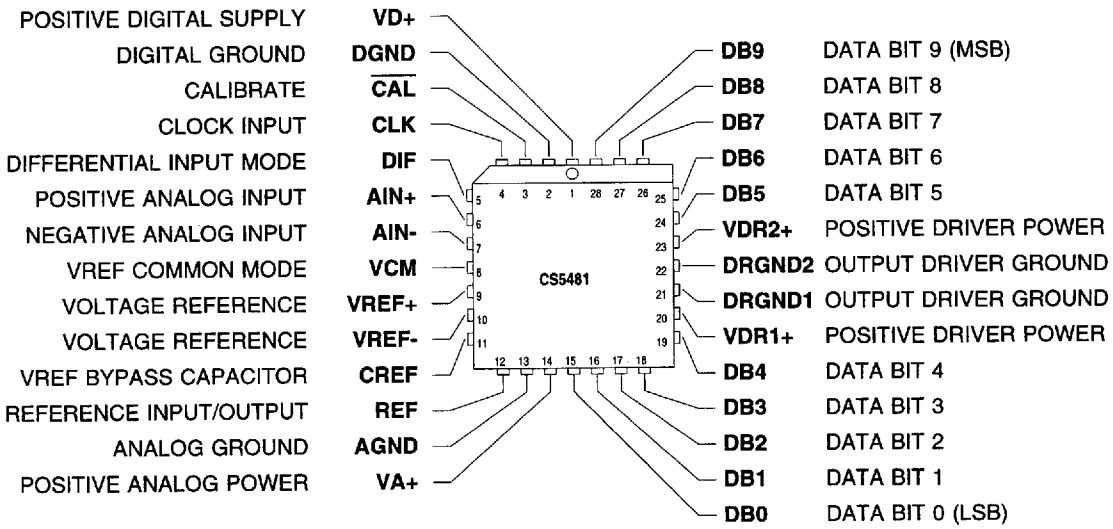


Figure 3. Timing Diagram

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 14
Positive analog supply voltage. Nominally +5 volts.

VD+ - Positive Digital Power, PIN 1
Positive digital supply voltage. Nominally +5 volts.

VDR1+, VDR2+ - Positive Output Driver Power, PINS 20, 23
Positive output driver supply voltage. Nominally +5 volts.

AGND - Analog Ground, PIN 13
Analog ground reference.

DGND - Digital Ground, PIN 2
Digital ground reference.

DRGND1, DRGND2 - Output Driver Ground, PINS 21, 22
Output Driver ground reference.

Analog Inputs

AIN+, AIN- - Analog Input, PINS 6, 7
AIN+ is the positive analog input signal to the differential input of the T/H amplifier. AIN- is the negative analog input signal to the differential input of the T/H amplifier. AIN- is normally tied to VCM for single-ended operation.

Reference Connections

VCM - Voltage Reference Common Mode, PIN 8
Signal common, nominally 2.5 volts.

VREF+ - Positive Voltage Reference, PIN 9
Positive full-scale voltage, nominally 3.1 volts.

VREF- - Negative Voltage Reference, PIN 10
Negative full-scale voltage, nominally 1.9 volts.

CREF - Voltage Reference Bypass Capacitor, PIN 11
Internal voltage reference must be bypassed with a 0.1µF capacitor in parallel with a 1000pF ceramic chip capacitor to analog ground. No other external connections allowed.

REF - Reference Input/Output, PIN 12
Internal voltage reference output, or optional external voltage reference input. Taken with respect to AGND represents the full-scale input range. Nominally 1.2 volts.

Digital Inputs

$\overline{\text{CAL}}$ - Calibrate, PIN 3
Calibration command. If brought low for 1 clock cycle or more, the CS5481 will reset and initiate an internal calibration. Calibrates for differential input signal (DIF=1) or single-ended input (DIF=0). Any spurious glitch on this pin may inadvertently place the chip in the calibration mode.

DIF - Differential Input Mode, PIN 5
With the DIF pin low, the device is configured for single-ended operation. With the DIF pin high, the device is configured for differential input operation.

Digital Outputs

DB0 through DB9 - Data Bus Outputs, PINS 15-19, 24-28
Data Bit 0 (LSB) through Data Bit 9 (MSB).

Clock Generator

CLK - Clock Input, PIN 4
A CMOS compatible clock must be input to the CLK pin to serve as the master clock for the device. A master clock must be present at all times to insure proper operation of the device.

DEFINITIONS

Linearity Error - INL

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero and gain errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in LSB's.

Differential Nonlinearity - DNL

The minimum resolution for which no missing codes is guaranteed. Units in LSB's.

Offset Error - V_{OS}

The deviation of the first code transition from the ideal (VREF- + 1LSB). Units in LSB's.

Full Scale Error - FSE

The deviation of the last code transition from the ideal (VREF- - 1LSB). Units in LSB's.

Signal-to-Noise - SNR

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc and distortion terms). Expressed in decibels (dB).

Signal-to- (Noise plus Distortion) - SINAD

The ratio of the rms value of the signal, to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels (dB).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant (2^{nd} through 5^{th}) harmonics to the rms value of the signal. Expressed in decibels (dB) or percent (%).

Intermodulation Distortion - IMD

The ratio of the rms value of the larger of the two test frequencies, which are 6dB down from full-scale, to the rms value of the largest 2^{nd} order and 3^{rd} order intermodulation components. Expressed in decibels (dB).

Effective Number of Bits - ENOB

A measure of ac linearity and is calculated from: ENOB = [(SNR - 1.76)/6.02]

Spurious-Free-Dynamic-Range - SFDR

The ratio of the rms value of the signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic. Units in percent (%) and decibels relative to the carrier (dBc).

Differential Phase - DP

The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed. Units in degrees.

Differential Gain - DG

The difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed. Units in percent (%).

Over voltage Recovery Time - t_{ovr}

The time required for the ADC to recover to full accuracy after an analog signal 150% of full scale is reduced to 50% of the full-scale value. Units in nanoseconds.

Aperture Delay - t_{apd}

The time delay between the falling edge and the actual start of the HOLD mode in a Track and Hold function. Units in nanoseconds.

Aperture Jitter - t_{apj}

The range of variation in the aperture time. Effectively a "sampling window" which ultimately dictates the maximum input slew rate acceptable for a given accuracy. Units in picoseconds.

Pipeline Delay - t_{pd}

The number of clock cycles between the initiation of the conversion process and the associated output data bit being available. Expressed in clock cycles.

Full Power Bandwidth

The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.