T-46-23-10

CY7C164A
CY7C166A

CYPRESS SEMICONDUCTOR

16,384 x 4 Static R/W RAM

Features

- Automatic power-down when deselected
- Output Enable ($\overline{OE}$) feature (7C166A)
- CMOS for optimum speed/power
- High speed
  - t_{AA} = 15 ns
- Low active power
  - 550 mW
- Low standby power
  - 220 mW
- TTL-compatible imputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C164A and CY7C166A are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C166A has an active low output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

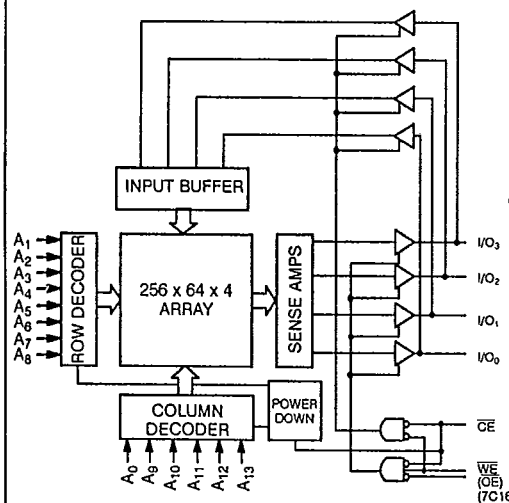
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW (and the output enable ($\overline{OE}$) is LOW for the 7C166A). Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166A), while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{OE}$) is HIGH for 7C166A).

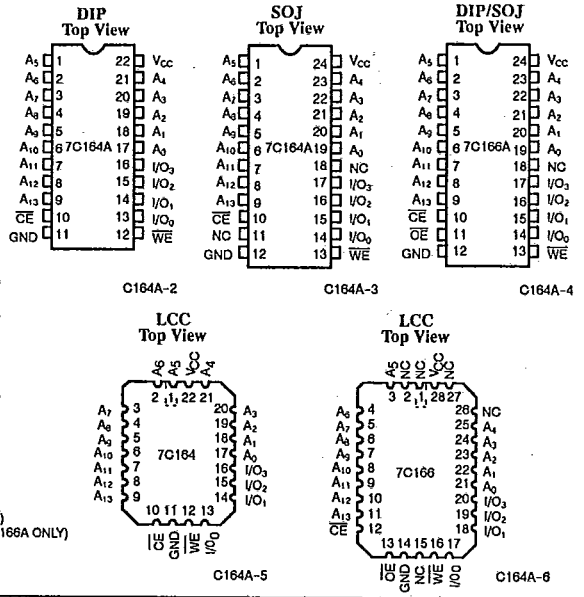
A die coat is used to insure alpha immunity.

Logic Block Diagram



C164A-1

Pin Configurations



Selection Guide

		7C164A-15 7C166A-15	7C164A-20 7C166A-20	7C164A-25 7C166A-25	7C164A-35 7C166A-35	7C164A-45 7C166A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	100	100	100	100
	Military		100	100	100	100
Maximum Standby Current (mA)	Commercial	40/20	40/20	30	30	30
	Military		40/20	40/20	30	30

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CY7C164A
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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage to Ground Potential ..... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to + 7.0V

DC Input Voltage ..... – 3.0V to + 7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C164A–15 7C166A–15 Min.	7C164A–15 7C166A–15 Max.	7C164A–20 7C166A–20 Min.	7C164A–20 7C166A–20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			–3.0	0.8	–3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		115		100	mA
			Mil				100	
I_{SB1}	Automatic $\overline{CE}$[5] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Com'l		40		40	mA
			Mil				40	
I_{SB2}	Automatic $\overline{CE}$[5] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V	Com'l		20		20	mA
			Mil				20	

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = –3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
6. Tested initially and after any design or process changes that may affect these parameters.

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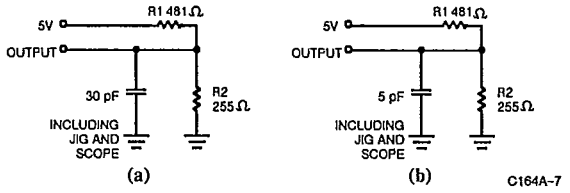
Electrical Characteristics Over the Operating Range [2] (continued)

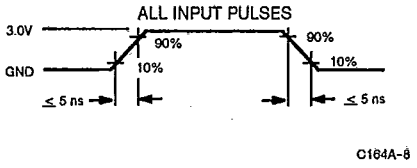
Parameters	Description	Test Conditions		7C164A-25 7C166A-25 Min.	7C164A-25 7C166A-25 Max.	7C164A-35,45 7C166A-35,45 Min.	7C164A-35,45 7C166A-35,45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		-10	+10	-10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		-10	+10	-10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		100		100	mA
			Mil		100		100	
I_{SB1}	Automatic $\overline{CE}$[5] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Com'l		30		30	mA
			Mil		40		30	
I_{SB2}	Automatic $\overline{CE}$[5] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} - 0.3V V_{IN} ≥ V_{CC} - 0.3V or V_{IN} ≤ 0.3V	Com'l		20		20	mA
			Mil		20		20	

Capacitance[6]

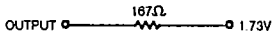
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





Equivalent to: THEVENIN EQUIVALENT



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Switching Characteristics Over the Operating Range[2,7]

Parameters	Description		7C164A-15 7C166A-15 Min.	7C164A-15 7C166A-15 Max.	7C164A-20 7C166A-20 Min.	7C164A-20 7C166A-20 Max.	7C164A-25 7C166A-25 Min.	7C164A-25 7C166A-25 Max.	7C164A-35 7C166A-35 Min.	7C164A-35 7C166A-35 Max.	7C164A-45 7C166A-45 Min.	7C164A-45 7C166A-45 Max.	Units
READ CYCLE													
t_{RC}	Read Cycle Time		15		20		25		35		45		ns
t_{AA}	Address to Data Valid			15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change		3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7C166A		10		10		12		15		20	ns
t_{LHZOE}	$\overline{OE}$ LOW to LOW Z	7C166A	3		3		3		3		3		ns
t_{LZOE}	$\overline{OE}$ HIGH to HIGH Z	7C166A		8		8		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]		3		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]			8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			15		20		20		20		25	ns
WRITE CYCLE[10]													
t_{WC}	Write Cycle Time		15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End		12		15		20		25		30		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End		10		10		10		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]		5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]			7		7		7		10		15	ns

Notes:
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
9. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL}. (7C166: $\overline{OE}$ = V_{IL} also).
13. Address valid prior to or coincident with $\overline{CE}$ transition low.
14. 7C166 only: Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

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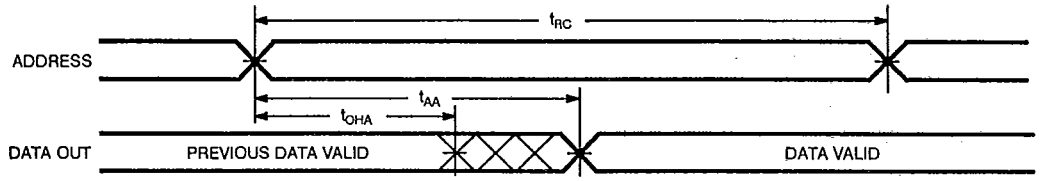
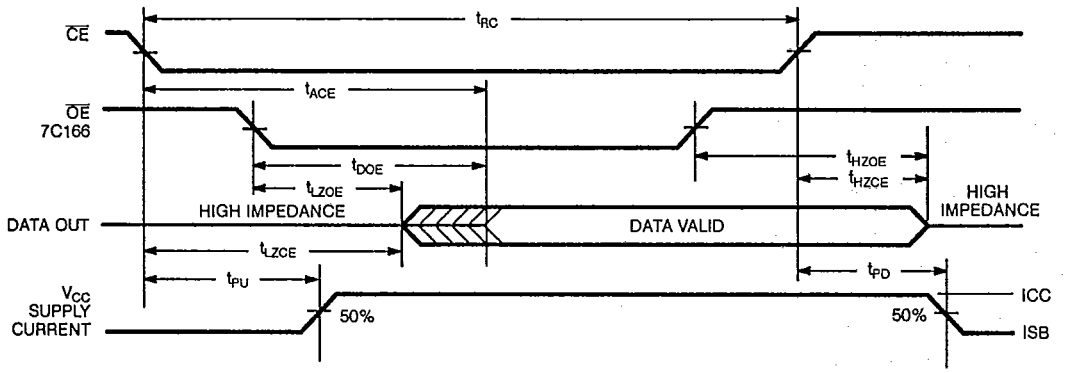
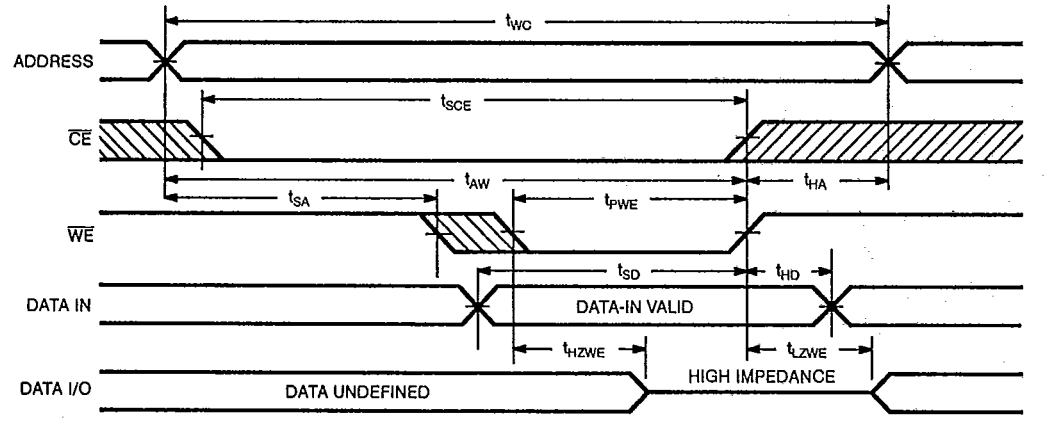
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [10, 14]



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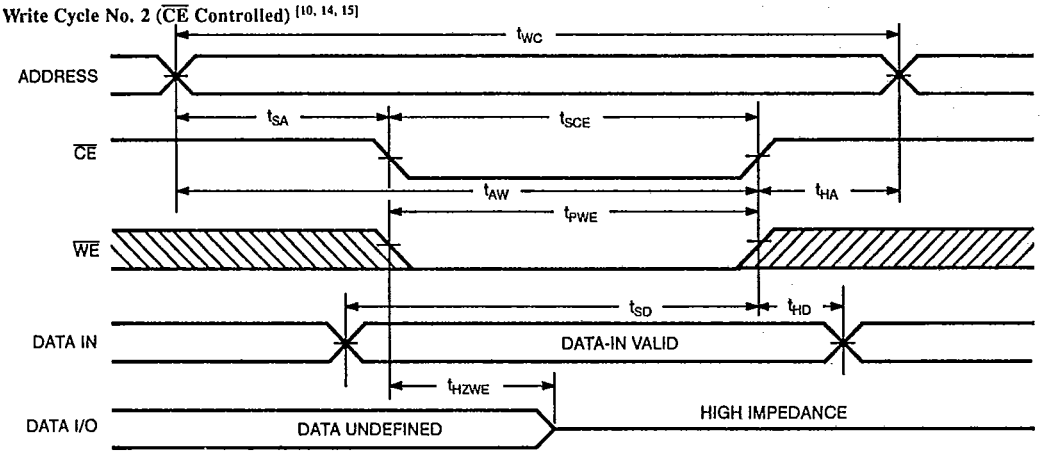
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [10, 14, 15]



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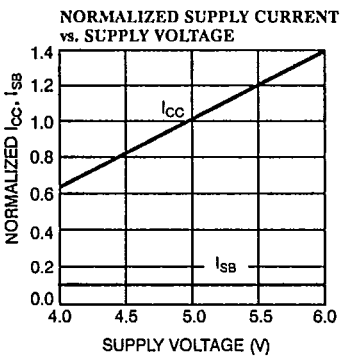
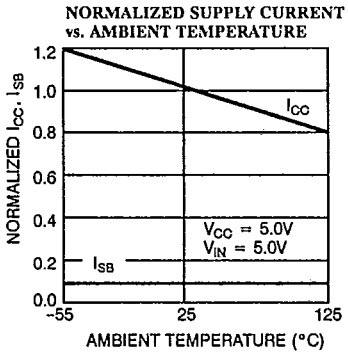
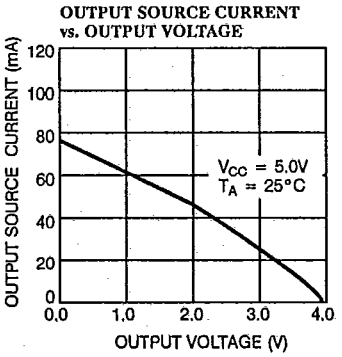
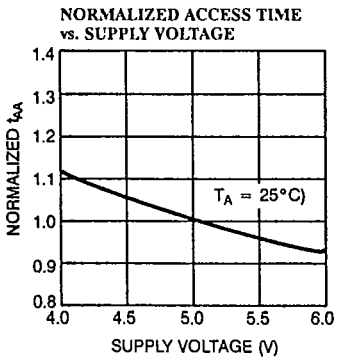
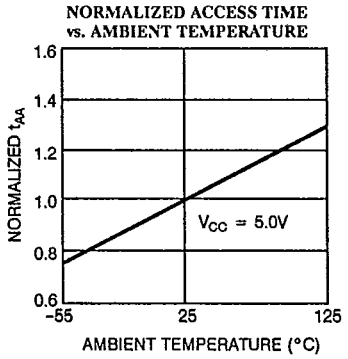
Typical DC and AC Characteristics

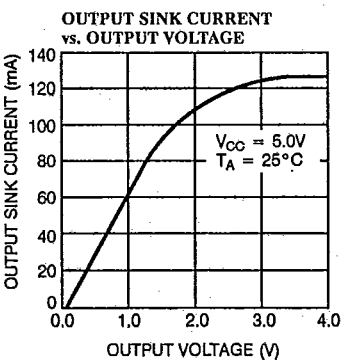












Typical DC and AC Characteristics (continued)

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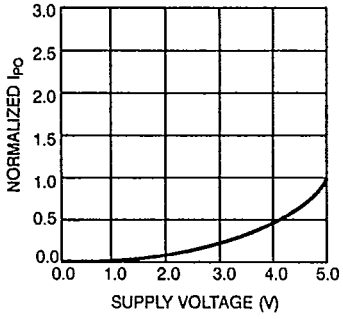
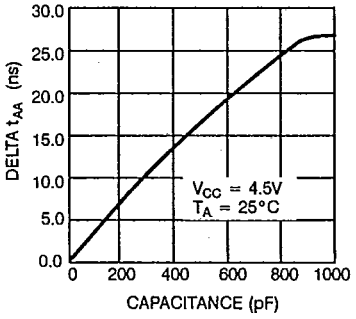
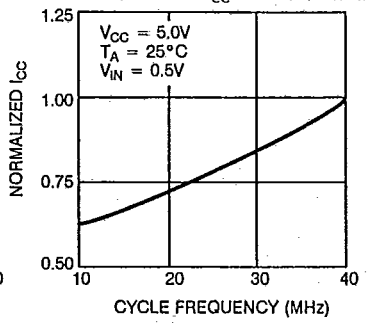
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



7C164A Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7C166A Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

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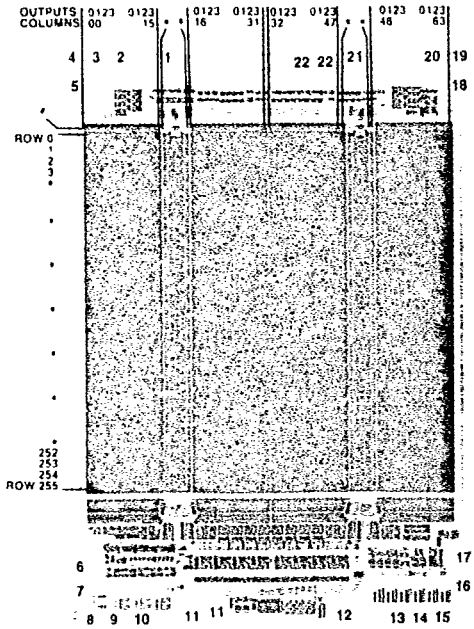
Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C164A-15PC	P9	Commercial
	CY7C164A-15VC	V13	
	CY7C164A-15DC	D10	
	CY7C164A-15LC	L52	
20	CY7C164A-20PC	P9	Commercial
	CY7C164A-20VC	V13	
	CY7C164A-20DC	D10	
	CY7C164A-20LC	L52	
	CY7C164A-20DMB	D10	Military
	CY7C164A-20LMB	L52	
	CY7C164A-20KMB	K73	
25	CY7C164A-25PC	P9	Commercial
	CY7C164A-25VC	V13	
	CY7C164A-25DC	D10	
	CY7C164A-25LC	L52	
	CY7C164A-25DMB	D10	Military
	CY7C164A-25LMB	L52	
	CY7C164A-25KMB	K73	
35	CY7C164A-35PC	P9	Commercial
	CY7C164A-35VC	V13	
	CY7C164A-35DC	D10	
	CY7C164A-35LC	L52	
	CY7C164A-35DMB	D10	Military
	CY7C164A-35LMB	L52	
	CY7C164A-35KMB	K73	
45	CY7C164A-45PC	P9	Commercial
	CY7C164A-45VC	V13	
	CY7C164A-45DC	D10	
	CY7C164A-45LC	L52	
	CY7C164A-45DMB	D10	Military
	CY7C164A-45LMB	L52	
	CY7C164A-45KMB	K73	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C166A-15PC	P13	Commercial
	CY7C166A-15VC	V13	
	CY7C166A-15DC	D10	
	CY7C166A-15LC	L52	
20	CY7C166A-20PC	P13	Commercial
	CY7C166A-20VC	V13	
	CY7C166A-20DC	D14	
	CY7C166A-20LC	L54	
	CY7C166A-20DMB	D14	Military
	CY7C166A-20LMB	L54	
	CY7C166A-20KMB	K73	
25	CY7C166A-25PC	P13	Commercial
	CY7C166A-25VC	V13	
	CY7C166A-25DC	D14	
	CY7C166A-25LC	L54	
	CY7C166A-25DMB	D14	Military
	CY7C166A-25LMB	L54	
	CY7C166A-25KMB	K73	
35	CY7C166A-35PC	P13	Commercial
	CY7C166A-35VC	V13	
	CY7C166A-35DC	D14	
	CY7C166A-35LC	L54	
	CY7C166A-35DMB	D14	Military
	CY7C166A-35LMB	L54	
	CY7C166A-35KMB	K73	
45	CY7C166A-45PC	P13	Commercial
	CY7C166A-45VC	V13	
	CY7C166A-45DC	D14	
	CY7C166A-45LC	L54	
	CY7C166A-45DMB	D14	Military
	CY7C166A-45LMB	L54	
	CY7C166A-45KMB	K73	

Bit Map



Address Designators

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Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y5	6
A11	Y4	7
A12	Y0	8
A13	Y1	9
A0	Y2	17
A1	Y3	18
A2	X0	19
A3	X1	20
A4	X2	21

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}[16]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
16. 7C166A only.

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