PDSP16256 / A

PROGRAMMABLE FIR FILTER

(Supersedes version in December 1993 Digital Video & Video Digital Signal Processing IC Handbook, HB3923-1)

The PDSP16256 contains sixteen multiplier - accumulators, which can be multi cycled to provide from 16 to 128 stages of digital filtering. It accepts 16 bit data and coefficients, and accumulates results upto 32 bits.

In 16 tap mode the device samples data at the 25MHz system clock rate. If a lower sample rate is acceptable then the number of stages can be increased in powers of two upto a maximum of 128. Each time the number of stages is doubled, the sample clock rate must be halved with respect to the system clock. With 128 stages the sample clock is therefore one eighth of the system clock.

In all speed modes devices can be cascaded to provide filters of any length, only limited by the possibility of accumulator overflow. The 32 bit results are passed between cascaded devices without any intermediate scaling and subsequent loss of precision.

The device can be configured as either, one long filter, or two separate filters with half the number of taps in each. Both networks can have independent inputs and outputs.

Both single and cascaded devices can be operated in decimate by two mode. The output rate is then half the input rate, but twice the number of stages are possible at a given sample rate. A single device with a 20MHz clock would then, for example, provide a 128 stage low pass filter, with a 5MHz input rate and 2.5MHz output rate.

Coefficients are stored internally and can be down loaded from a host system or an EPROM. The latter requires no additional support, and is used in stand alone applications. A full set of coefficients is then automatically loaded at power on, or at the request of the system. A single EPROM can be used to provide coefficients for upto 16 devices.

FEATURES

- Sixteen MACs in a single device
- Basic mode is 16 tap filter with 25MHz sample rates
- 16 bit data and 32 bit accumulators
- Programmable to give up to 128 taps with sampling rates proportionally reducing to 3.13MHz
- Can be configured as one long filter or two half length filters
- Decimate by two option will double the filter length
- Coefficients supplied from a host system or a local EPROM
- Advanced 144 PGA package with integral ground and supply Splanes

APPLICATIONS

- High Performance Digital Filters
- Pulse Compression for Radar & Sonar
- Matrix Multiplication
- Correlation

ASSOCIATED PRODUCTS

PDSP16350 I/Q Splitter / NCO

PDSP16510 FFT Processor

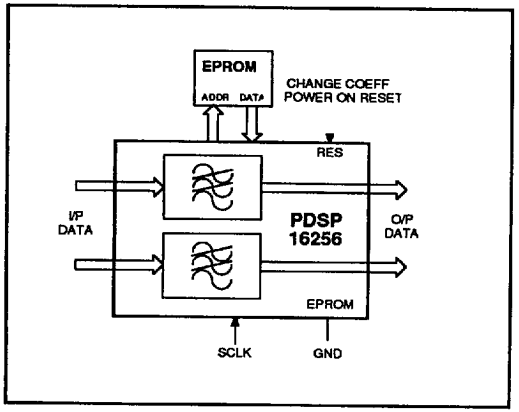

Fig. 1 Dual Filter

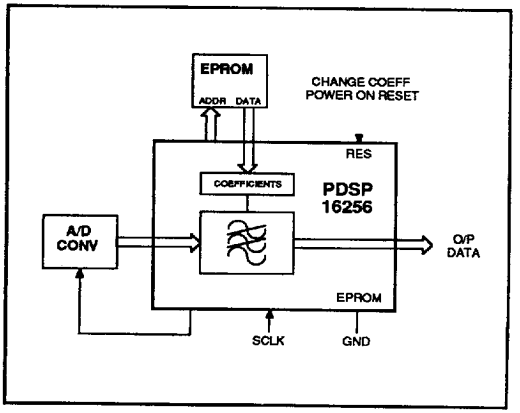

Fig. 2 Typical System Application

SIGNAL	DESCRIPTION
DA15:0	16 bit data input bus to Network A.
DB15:0	Delayed data output bus in the single filter mode. Connected to the data input bus of the next device in a cascaded chain. Input to Network B in the dual filter modes.
X31:0	Expansion input bus in the single filter mode. Connected to the previous filter output in a cascaded chain. The inputs are not used on a single device system or on the Termination device in a cascaded chain. The output from Network B in the dual modes.
F31:0	In single filter mode this bus holds the main device output. In dual mode it holds the output from Network A.
FEN	Filter enable. The first high present on an SCLK rising edge defines the first data sample. The signal must stay active whilst valid data is being received.
DFEN	Delayed filter enable. This output is connected to the Filter Enable input of the next device in a cascaded chain, when moving towards the termination device. It is used to coordinate the control logic within each device.
SWAP	Selects either the upper or lower set of coefficients for Bank Swap. A low selects the lower bank, a high the upper bank.
FRUN	When high this signal allows continuous filter operations to occur without the need for the initial FEN edge. If the device is not a single or interface device then this pin must be tied low.
$\overline{\text{DCLR}}$	A low on this signal on the SCLK rising edge will clear all the internal accumulators. DCLR need only remain low for a single cycle, signal BUSY will indicate when the internal clearing is complete. After a clear the device must be re-synchronised to the data stream using FEN. It is recommended the FEN is taken low at the same time as clear. FEN may then be taken high to synchronise the data stream once BUSY has returned low.
C15:0	16 bit coefficient input bus. In the Byte mode of operation, C15:8 have alternative uses as explained in the text.
A7:0	Coefficient address bus. In the EPROM mode A7:0 are address outputs for an EPROM. In the remote host mode they are inputs from the host. A7 is not used when coefficients are loaded as 16 bit words.
CCS	This pin is similar in operation to A7:0 and provides a higher order address bit. When low the coefficients are loaded, when high the control register is loaded.
$\overline{\text{WEN}}$	In the remote mode this pin is an input which when low enables the load operation. In the EPROM mode it is an output which provides the write enable for other slave devices.
$\overline{\text{CS}}$	This pin is always an input and must also be low for the internal write operation to occur.
$\overline{\text{BYTE}}$	When this pin is tied low, coefficients are loaded as two bytes. When the pin is high they are loaded as 16 bit words. In the EPROM mode this pin is ignored.
$\overline{\text{EPROM}}$	When this pin is tied low coefficients are loaded as bytes from an external EPROM. The device outputs an address on A7:0. When the pin is high coefficients must be loaded from a remote master. They can then be transferred individually rather than as a complete set.
SCLK	The main system clock, all operations are synchronous with this clock. The clock rate must be either 1, 2, 4, or 8 times the required data sampling rate. The factor used depends on the required filter length.
CLKOP	This output when used to enable SCLK can provide a data sampling clock. It has the effect of dividing the SCLK rate by 1, 2, 4 or 8 depending on the filter mode selected.
$\overline{\text{OEN}}$	Tri-state enable for the F bus. When high the outputs will be high impedance. OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge

SIGNAL	DESCRIPTION
BUSY	A high on this signal indicates that the device is completing internal operations and is not yet able to accept new data. The signal is used during automatic EPROM loading, reset and accumulator clearing.
$\overline{RES}$	When this pin is low the control logic and accumulators are reset. In the EPROM mode it will initiate a load sequence when it goes high.

NOTE unused busses (e.g. X31:0 when the device is configured in single or termination mode) can be set to any value. They should however be maintained at a valid logic level to avoid an increase in power consumption.

To ensure correct input voltage thresholds are maintained all the VDD and GND pins must be connected to adequate power and ground planes.

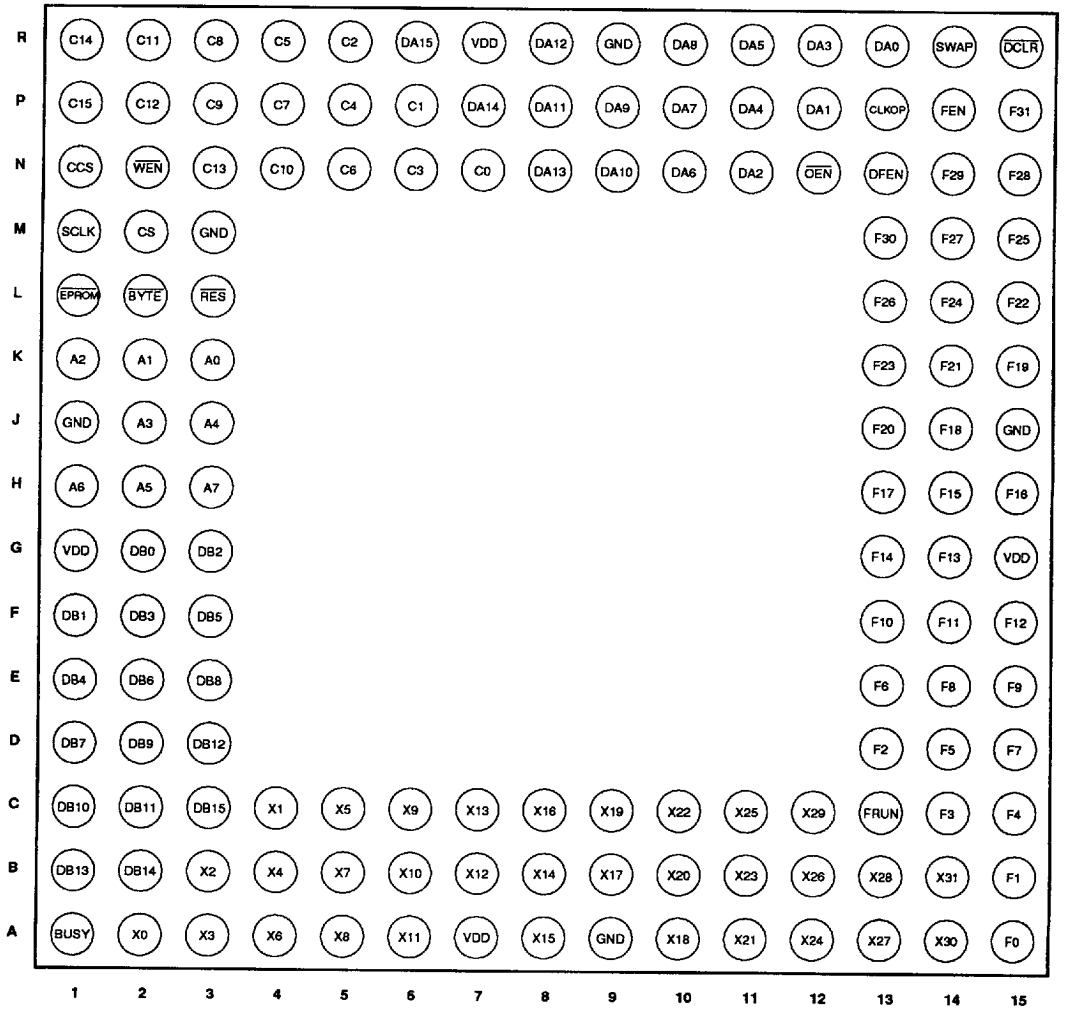

Fig. 3A Device Pinout - Bottom view (144 pin PGA - AC144)

GC	SIG	GC	SIG	GC	SIG	GC	SIG
1	F0	44	SWAP	87	C15	130	GND
2	F1	45	GND	88	GND	131	BUSY
3	F2	46	$\overline{OEN}$	89	GND	132	X0
4	F3	47	CLKOP	90	$\overline{WEN}$	133	VDD
5	VDD	48	VDD	91	CCS	134	X1
6	F4	49	DA0	92	$\overline{CS}$	135	X2
7	F5	50	DA1	93	VDD	136	X3
8	GND	51	DA2	94	$\overline{RES}$	137	X4
9	F6	52	DA3	95	SCLK	138	X5
10	F7	53	DA4	96	GND	139	X6
11	F8	54	DA5	97	VDD	140	GND
12	F9	55	GND	98	$\overline{BYTE}$	141	X7
13	F10	56	DA6	99	$\overline{EPROM}$	142	X8
14	F11	57	DA7	100	A0	143	VDD
15	F12	58	DA8	101	A1	144	X9
16	GND	59	DA9	102	A2	145	X10
17	F13	60	VDD	103	A3	146	X11
18	F14	61	DA10	104	A4	147	X12
19	F15	62	DA11	105	VDD	148	X13
20	VDD	63	DA12	106	A5	149	X14
21	F16	64	DA13	107	A6	150	GND
22	F17	65	DA14	108	GND	151	X15
23	F18	66	DA15	109	A7	152	X16
24	F19	67	GND	110	DB0	153	X17
25	VDD	68	C0	111	DB1	154	X18
26	F20	69	C1	112	DB2	155	X19
27	F21	70	C2	113	GND	156	X20
28	GND	71	C3	114	DB3	157	X21
29	F22	72	C4	115	DB4	158	X22
30	F23	73	C5	116	DB5	159	GND
31	F24	74	VDD	117	DB6	160	X23
32	F25	75	C6	118	DB7	161	X24
33	F26	76	C7	119	VDD	162	X25
34	F27	77	C8	120	DB8	163	VDD
35	F28	78	C9	121	DB9	164	X26
36	GND	79	C10	122	DB10	165	X27
37	F29	80	GND	123	DB11	166	X28
38	F30	81	C11	124	DB12	167	X29
39	F31	82	C12	125	DB13	168	X30
40	VDD	83	C13	126	DB14	169	GND
41	FEN	84	VDD	127	GND	170	X31
42	DFEN	85	GND	128	DB15	171	VDD
43	$\overline{DCLR}$	86	C14	129	VDD	172	FRUN

Fig. 3B Device Pinout (172 pin QFP - GC172)

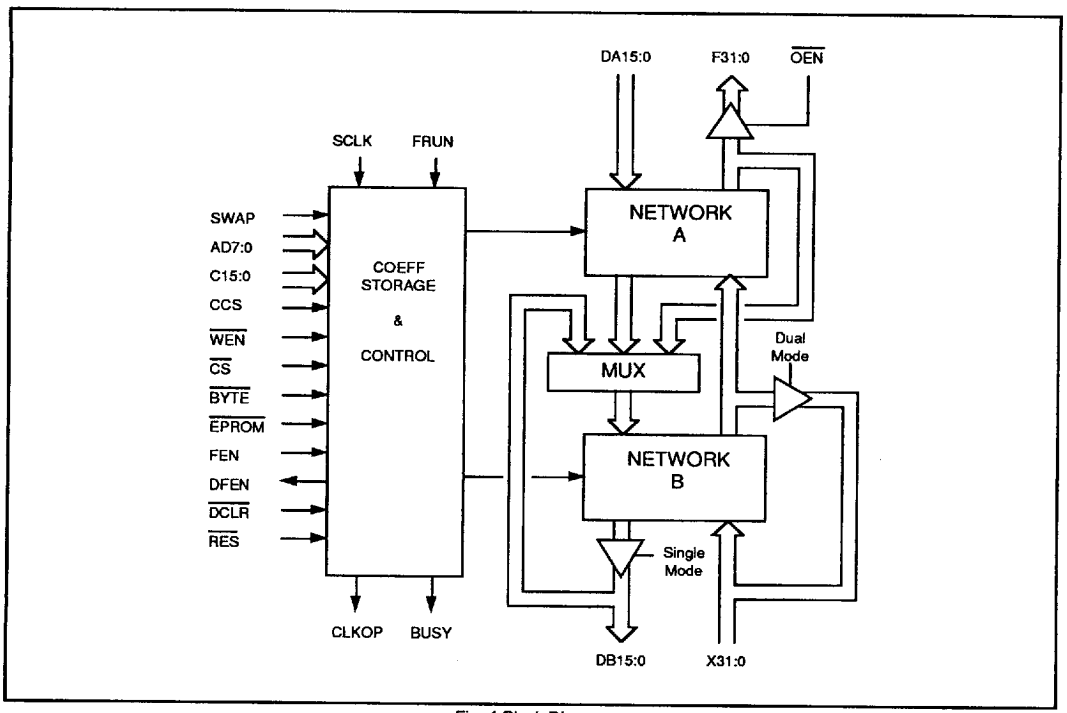

Fig. 4 Block Diagram

OPERATIONAL OVERVIEW

The PDSP16256 is an application specific FIR filter for use in high performance digital signal processing systems. Sampling rates can be upto 25MHz The device provides the filter function without any software development, and the options are simply selected by loading a control register. The device can be user configured as either a single filter, or as two separate filters. The latter can provide two independent filters for the in-phase and quadrature channels after IQ splitting, or can provide two filters in cascade for greater stop band rejection.

The device operates from a system clock, with rates up to 25MHz. This clock must be 1, 2, 4, or 8 times the required sampling frequency, with the higher multiplication rates producing longer filter networks at the expense of lower sampling rates. Devices can be connected in cascade to produce longer filter lengths. This can be accomplished without the need for any additional external data delays, and all the single device options remain available.

Continuous inputs are accepted, and continuous results produced after the internal pipeline delay. Connection can be made directly to an A/D converter. The filter operation can be synchronised to a Filter Enable signal whose active going edge marks the first data sample. The internal multiplier - accumulator array can be cleared with a dedicated input. This is necessary if erroneous results obtained during the normal data 'flush through' are not permissible.

Coefficients can be loaded from a host system using a conventional peripheral interface and separate data bus. Alternatively, they can be loaded as a complete set from a byte wide EPROM. The device produces addresses for the EPROM and a BUSY output indicates that the transfer is occurring. Up to sixteen devices can have their coefficients supplied from a single EPROM. These devices need not necessarily be part of the same filter network.

Each of the filter networks shown in Fig. 4 contains eight systolic multiplier accumulator stages, an example with four stages is shown in Fig. 5. Input data flows through the delay lines and is presented for multiplication with the required coefficient. This is added to either the last result from this accumulator or the result from the previous accumulator. The filter results progress along the adders at the data sample rate. If the sample rate equals SCLK divided by four, for example, then the accumulated result is passed onto the next stage every forth cycle. The structure described is highly efficient when used to calculate filtered results from continuous input data.

A comprehensive digital filter design program is available for PC compatible machines. This will optimise the filter coefficients for the filter type required and number of taps available at the selected sample rate within the PDSP16256 device. An EPROM file can be automatically generated in Motorola S-record format.

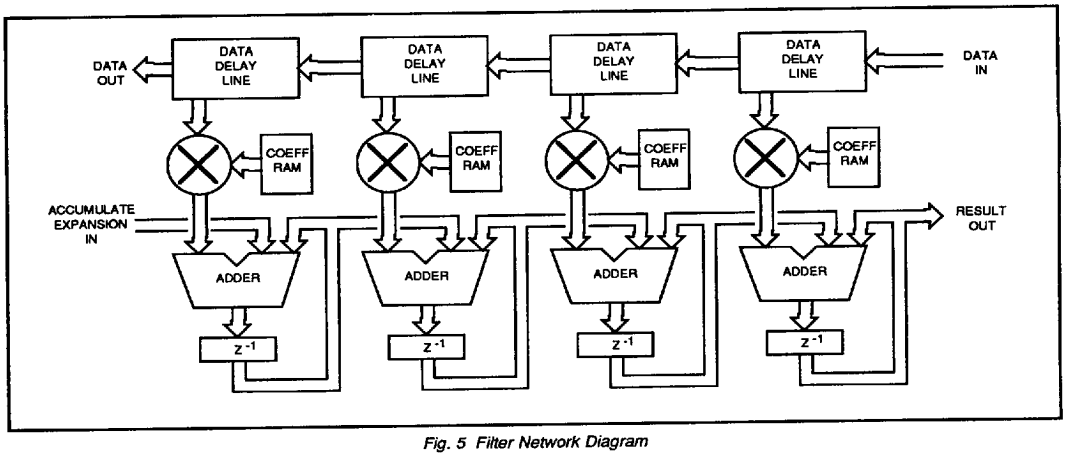

Fig. 5 Filter Network Diagram

SINGLE FILTER OPTIONS

When operating as a single filter the device accepts data on the 16 bit DA bus at the selected sample rate, see Figs 6 and 7. Results are presented on the 32 bit F bus, which may be tristated using the OEN input. Signal OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge. Devices may be cascaded this allows filters with more taps than available from a single device. To accomplish this two further busses are utilised. The DB bus presents the input data to the next device in cascade after the appropriate delay, while, partial results are accepted on the X bus.

Single filter mode is selected by setting control register bit 15 to a one. The required filter length is then selected using control register bits 14 and 13 as summarised in Table 3. The options define the number of times each multiplier - accumulator is used per sample clock period. This can be once, twice, four times, or eight times.

In addition a normal/decimate bit (CR12) allows the filter length to be doubled at any sample rate. This is possible when the filter coefficients are selected to produce a low pass filter, since the filtered output would then not contain the higher frequency components present in the input. The Nyquist criterion, specifying that the sampling rate must be at least double the highest frequency component, can still then be satisfied even though the sampling rate has been halved.

CR 14	CR 13	CR 12	Input Rate	Output Rate	Filter Length	Setup Latency
0	0	0	SCLK	SCLK	16 Taps	16
0	0	1	SCLK	SCLK/2	32 Taps	17
0	1	0	SCLK/2	SCLK/2	32 Taps	16
0	1	1	SCLK/2	SCLK/4	64 Taps	18
1	0	0	SCLK/4	SCLK/4	64 Taps	20
1	0	1	SCLK/4	SCLK/8	128 Taps	24
1	1	0	SCLK/8	SCLK/8	128 Taps	24

Table 3. Single Filter Options

The system clock latency for a single device is shown in Table 3. This is defined as the delay from a particular data sample being available on the input pins to the first result including that input appearing on the output pins. It does not include the delay needed to gather N samples, for an N tap filter, before a mathematically correct result is obtained.

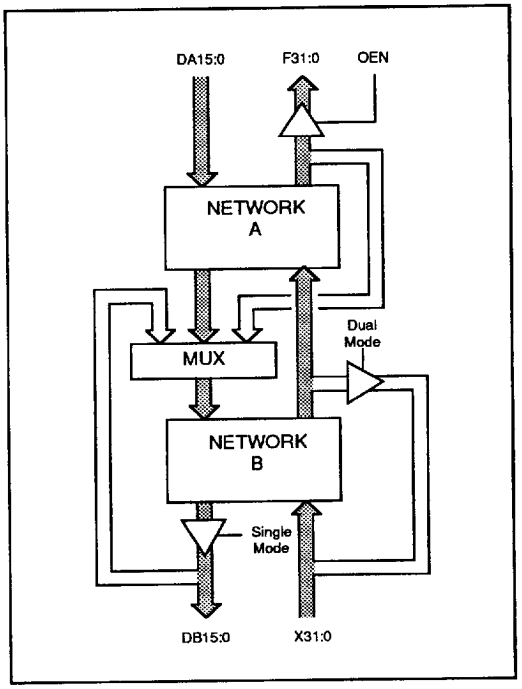

Fig. 6 Single Filter Bus Utilisation

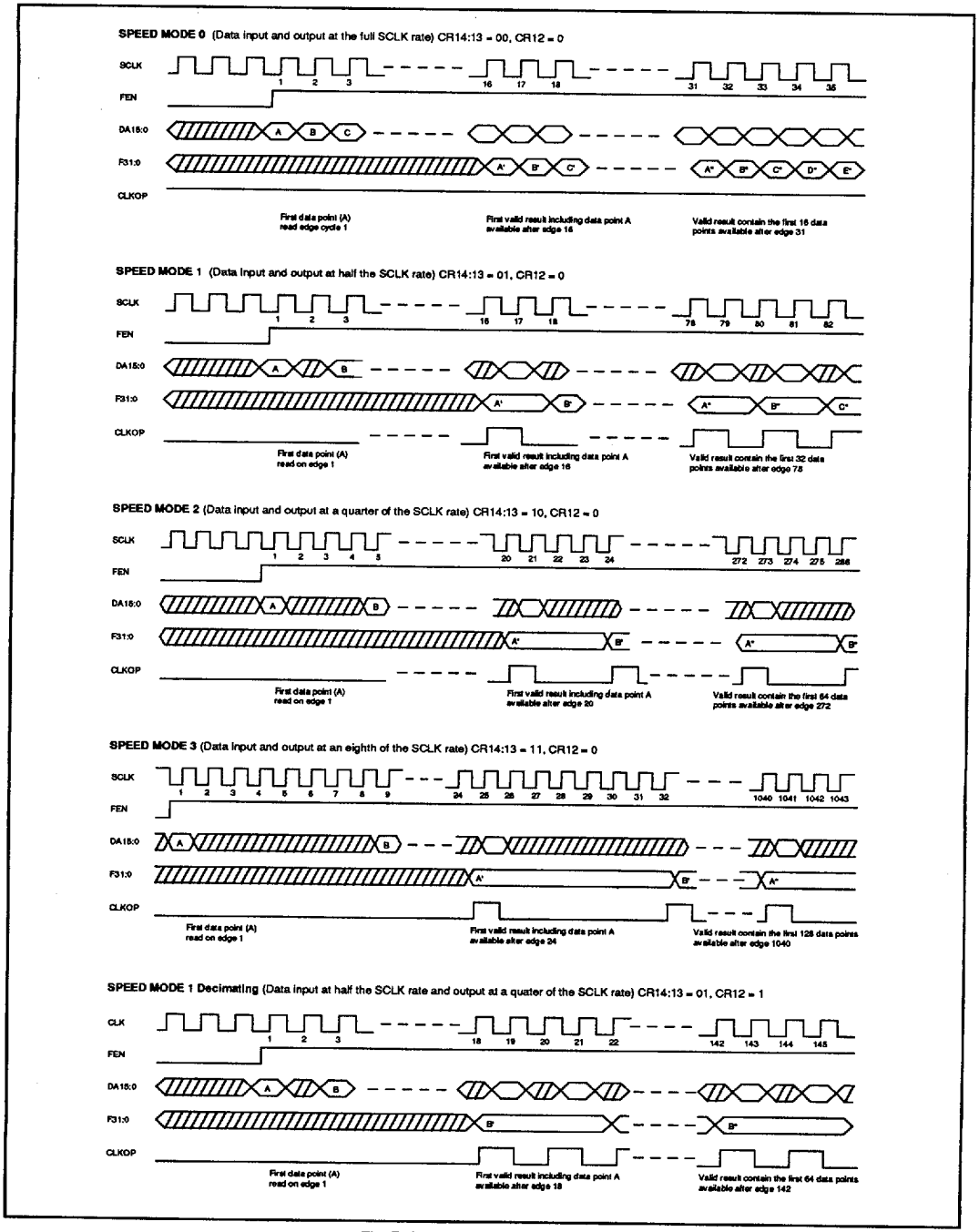

Fig. 7 Single Filter Timing Diagrams

DUAL INDEPENDENT FILTER OPTIONS

When operating as two independent filters the device accepts 16 bit data on both the DA and DB buses at the selected sample rate, see Fig. 8. Results are available from both the F and X buses. The F bus may be tristated using the OEN input. Signal OEN is registered onto the device and does not therefore take effect until the first SCLK rising edge

Each filter must be configured in the same manner, and multiple device expansion is not possible due to the pin reorganization. The latter requirement can, of course, still be satisfied by several devices configured as single filters.

Dual independent filter mode is selected by setting control register bits 15 and 4 to a zero. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. As in single filter mode normal or decimate by two operation can be selected using control register bit 12.

CR 14 13 12	Input Rate	Output Rate	Filter Length	Setup Latency	
				Ind	Cas
0 0 0	SCLK	SCLK	8 Taps	16	27
0 0 1	SCLK	SCLK/2	16 Taps	17	-
0 1 0	SCLK/2	SCLK/2	16 Taps	16	28
0 1 1	SCLK/2	SCLK/4	32 Taps	18	-
1 0 0	SCLK/4	SCLK/4	32 Taps	20	36
1 0 1	SCLK/4	SCLK/8	64 Taps	24	-
1 1 0	SCLK/8	SCLK/8	64 Taps	24	40

Table 4. Dual Filter Options

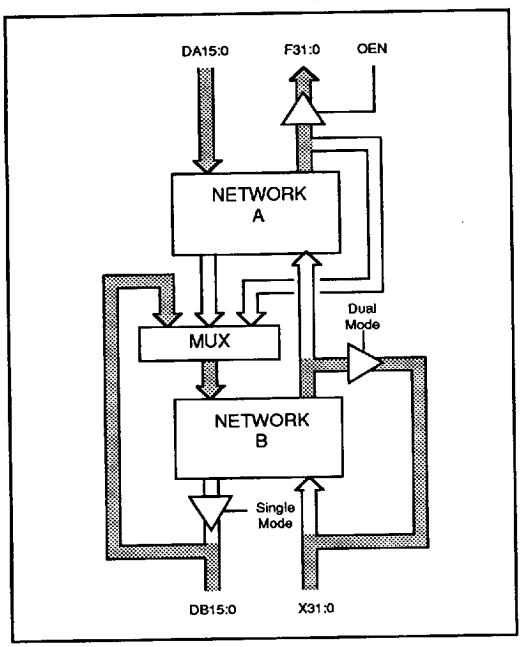

Fig. 8 Dual Independent Filter Bus Utilisation

DUAL CASCADED FILTER OPTIONS

When operating as two cascaded filters the device accepts 16 bit data on the DA bus at the selected sample rate. Results are presented on the 32 bit X bus, see Fig. 9. Each filter must be configured in the same manner. Multiple device expansion is not possible in this mode.

Dual cascaded filter mode is selected by setting control register bit 15 to a zero and bit 4 to a one. The required filter length is selected using control register bits 14 and 13 as summarised in Table 4, which also shows the resulting latency. The decimate by two option is not available in this mode.

The data for the second filter network is extracted as the middle 16 bits from the first networks accumulated result. For successful operation the first filter network must have unity gain. See the section on filter accuracy for more details.

The cascade option is used to increase the stop band rejection in a practical filter application. Theoretically, increasing the number of taps in an FIR filter will increase the stop band rejection, but this assumes floating point calculations with no accuracy limitations. In practice, with fixed point arithmetic, better performance is achieved with two smaller filters in series.

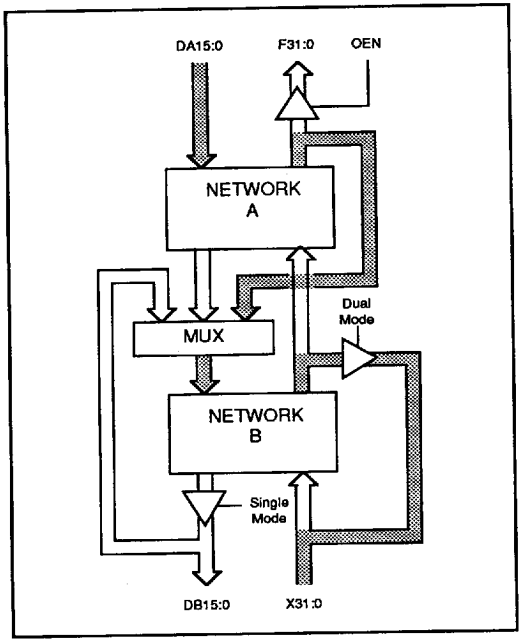

Fig. 9 Dual Cascaded Filter Bus Utilisation

FILTER ACCURACY

Input data and coefficients are both represented by 16bit two's complement numbers. The coefficients are converted to twelve bits by rounding towards zero. This is achieved as follows. If the coefficient is positive then the least significant 4 bits are discarded. If the coefficient is negative then the logical 'OR' of the least significant 4 bits are added to the remainder of the word. Twelve bit coefficients can be used directly provided the least significant four bits are set to zero.

The FIR filter results are calculated using a multiplier accumulator structure as shown in Fig. 10. The truncation and word growth allowed for in the data path are explained in Fig. 11. The 16 bit data and 12 bit coefficient inputs, (each with one sign bit before the binary point), are presented to the multiplier. This produces a 28 bit result with two bits before the binary point. Producing the full 28 bit result ensures that if both the data and coefficients are set to -1 a valid result is generated. Prior to entering the accumulator the least significant 4 bits of the multiplier result are truncated and the resulting 24 bits sign extended to 32 bits. The final accumulator result is 32 bits with 10 bits before the binary point. Thus 9 bits of word growth are allowed within the accumulator. All accumulator bits are made available on the output pins.

In cascade mode the middle 16 bits from the network A accumulator are fed round to the network B data inputs, see Fig. 11.

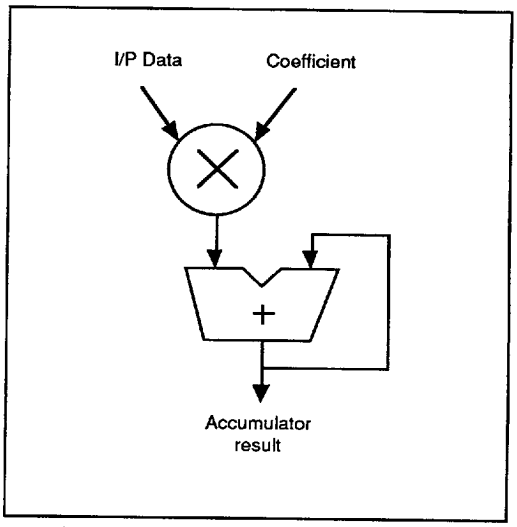

Fig. 10 Multiplier Accumulator

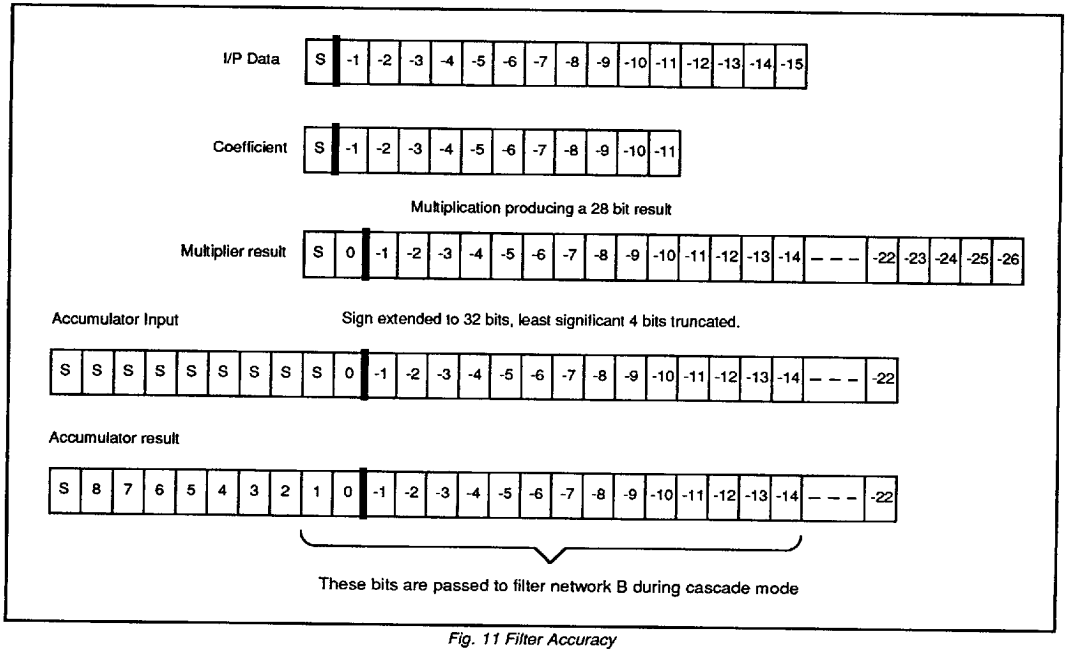

Fig. 11 Filter Accuracy

CASCADING DEVICES

When the filter requirements are beyond the capabilities of a single device, it is possible to connect several devices in cascade increasing the number of taps available at the required sample rate. Within each device all filter length, decimate, and bank swap options are still possible, but each device in the chain must be similarly programmed and configured as a single filter.

The number of devices which can be cascaded is only limited by the possibility of overflow in the 32 bit intermediate accumulations. If more than sixteen devices are cascaded in auto EPROM load mode, then an additional EPROM will be needed.

In modes where the data sample rate does not equal the clock rate. Then the cascade arrangement shown in Fig. 12 is utilised. Delayed data is passed from device to device in one direction, while intermediate results flow in the opposite direction. The interface device both accepts the input data and produces the final result. It is not necessary for each device to know its exact position in the chain, but the device which receives the input data and produces the final result must be identified, as must the device which terminates the chain. The former is known as the Interface device and the latter as the Termination device, all others are Intermediate devices. Control Register bits CR11:10 are used to define these positions as shown in Table 6.

The control logic in each of the devices must be synchronised with respect to the Interface device. This is achieved by connecting the Delayed Filter Enable output (DFEN) to the Filter Enable input (FEN) of the next device in the chain. The Interface device, itself, needs a Filter Enable signal produced by the system, unless the Free Run pin is pulled high. Even when the latter is true, the Filter Enable connection must be made between the remaining devices in the chain.

When devices are cascaded such that the data sample rate equals the clock rate, (Control register bits 14:13 = 00), then a different cascade configuration must be used. This is shown in Fig. 13. The number of devices which can be cascaded is, again, only limited by the 32 bit accumulators.

In this mode the delayed data is passed from device to device in the same direction as the intermediate results. The device which accepts the input data is now at the opposite end of the chain to the device which produces the final result. The control logic in each of the devices must be synchronised this is achieved by connecting all the device FEN inputs to the global Filter enable.

AVAILABLE OPTIONS

No more than 128 coefficients can be stored internally. This limits the filter length / decimate / bank swap options to those which do not require more than that number of coefficients. Thus when a filter with 128 taps is to be implemented in a single device, it is not possible to decimate or bank swap. When a filter with 64 taps is implemented, decimate or bank swap are possible, but not both. With all other filter lengths, all decimate and bank swap configurations are possible.

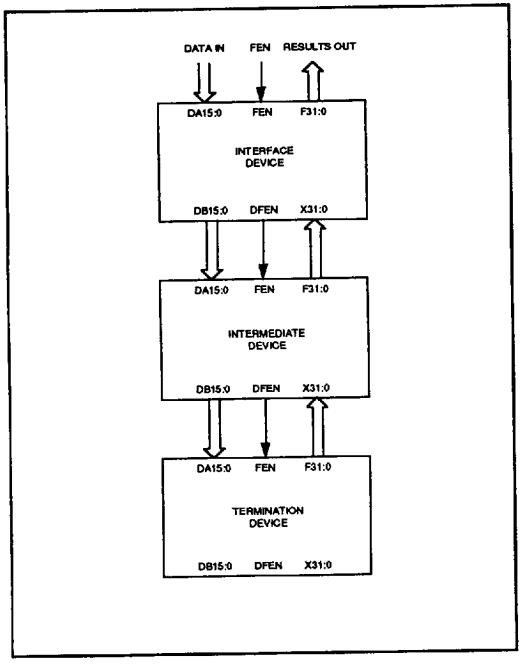

Fig. 12 Three Device Cascaded System

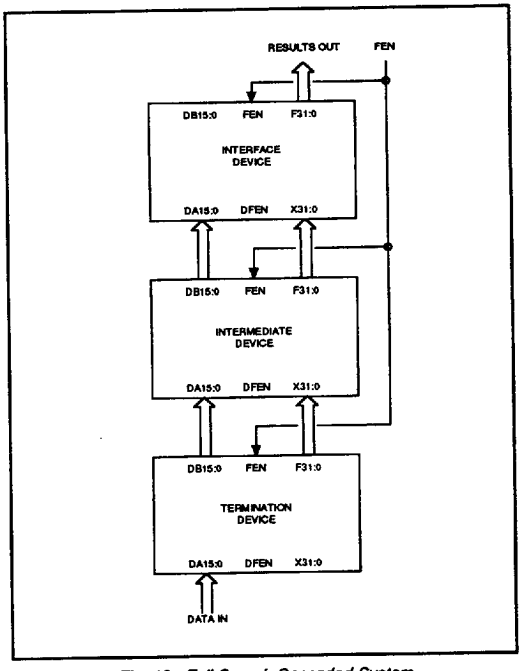

Fig. 13 Full Speed Cascaded System

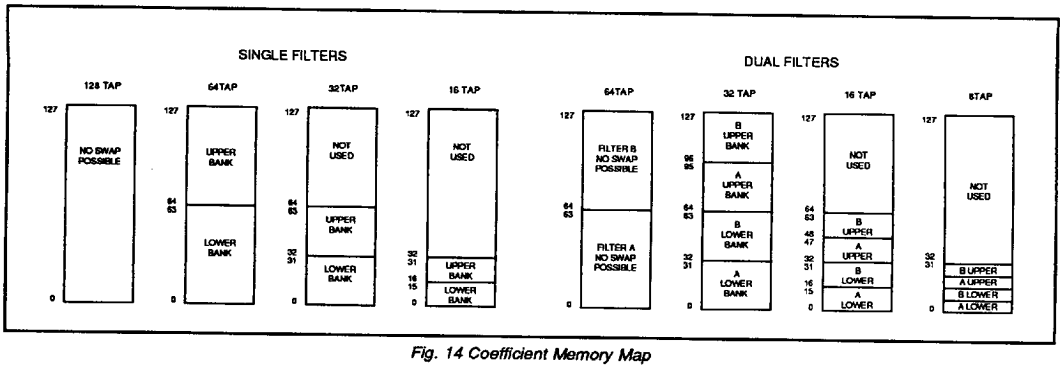

Fig. 14 Coefficient Memory Map

FILTER CONTROL

Two control modes are available selected by input signal FRUN. When FRUN is tied high the device will commence operation once the coefficients have been loaded. The CLKOP signal indicating when new input data is required and that new results are available, see Fig. 7. When FRUN is tied low filter operation will not commence until a high has been detected on signal FEN. This mode allows synchronisation to an existing data stream. Signal FEN should be taken high when the first valid data sample is available so that both are read into the device on the next SCLK rising edge.

During device reset the RES signal must be held low for a minimum of 16 SCLK cycles. After a reset the control register returns to it's default state of 8C80 Hex. This places the device into the following mode :-

- Single filter
- Sample rate equal to the clock rate
- Non-decimating
- A single device (Not in a cascade chain)
- Bank swap selected by bit in the control register

COEFFICIENT BANK SWAP

A Bank Swap feature is provided which allows ALL coefficients to be simultaneously replaced with a different set. A bit in the Control Register (CR7) allows the swap to be controlled by either input signal SWAP or Control Register bit (CR6). The latter is useful if the device is controlled by a microprocessor, when driving a separate pin would entail additional address decoding logic and an external latch.

If the pin or control register bit is low, the coefficients used will be those loaded into the lower banks illustrated in Fig. 14. When the pin or bit is high, the upper banks are used.

The actual swap will occur when the next sampling clock active going transition occurs. This can be up to seven system clocks later than the swap transition, and is filter length dependent. The first valid filtered output will then occur after the pipeline latancies given in Tables 3 and 4.

By setting a bit in the Control Register it is possible to bank swap on every data sampling clock. This function does not depend on the status of the SWAP pin or bit, and the lower bank will be initially selected after FEN goes active. The option can be used to implement filters with complex coefficients.

LOADING COEFFICIENTS

When the device is to operate in a stand alone application then the coefficients can be down loaded as a complete set from a previously programmed EPROM. Alternatively if the system contains a microprocessor they can be individually transferred from a remote master under software control. In any mode the system clock must be present and stable during the transfer, and the addressing scheme is such that the least significant address specifies the coefficient applied to the first multiplier seen by incoming data.

The addresses used during the load operation are those illustrated in Fig. 14. The Control Register is loaded when CCS is high. In BYTE mode address A0 is used to select the portion of control register loaded, otherwise the address bits are redundant. When an EPROM is used to provide coefficients, this redundancy causes the number of locations needed for any device to be double that for the coefficients alone.

AUTO EPROM LOAD

When the EPROM pin is tied low, the PDSP16256 assumes the role of a master device in the system and controls the loading of coefficients from an external EPROM, see Fig.15. A load sequence commences when the RESET input goes inactive, and will continue until every coefficient has been loaded. The BUSY pin goes high to indicate that a load sequence is occurring and the filter output is invalid. The device will not commence a filter operation until the Filter Enable edge is received (FEN) after BUSY has gone low. This requirement can be avoided if the Free Run pin (FRUN) is tied high.

The address bus pins become outputs on the Master device, and produce a new address every four system clock periods. This four clock interval, minus output delays and the data set up time, defines the available EPROM access time.

The coefficients are always loaded as bytes. The state of the BYTE pin on the master device is ignored. This arrangement also allows the eight, most significant, coefficient bus pins (C15:8) to be used for other purposes as described later. Since the 16 bit coefficients are loaded in two bytes the A0 pin specifies the required byte. The maximum number of stored coefficients is 128, eight address outputs are therefore provided for the EPROM. These eight outputs from the Master

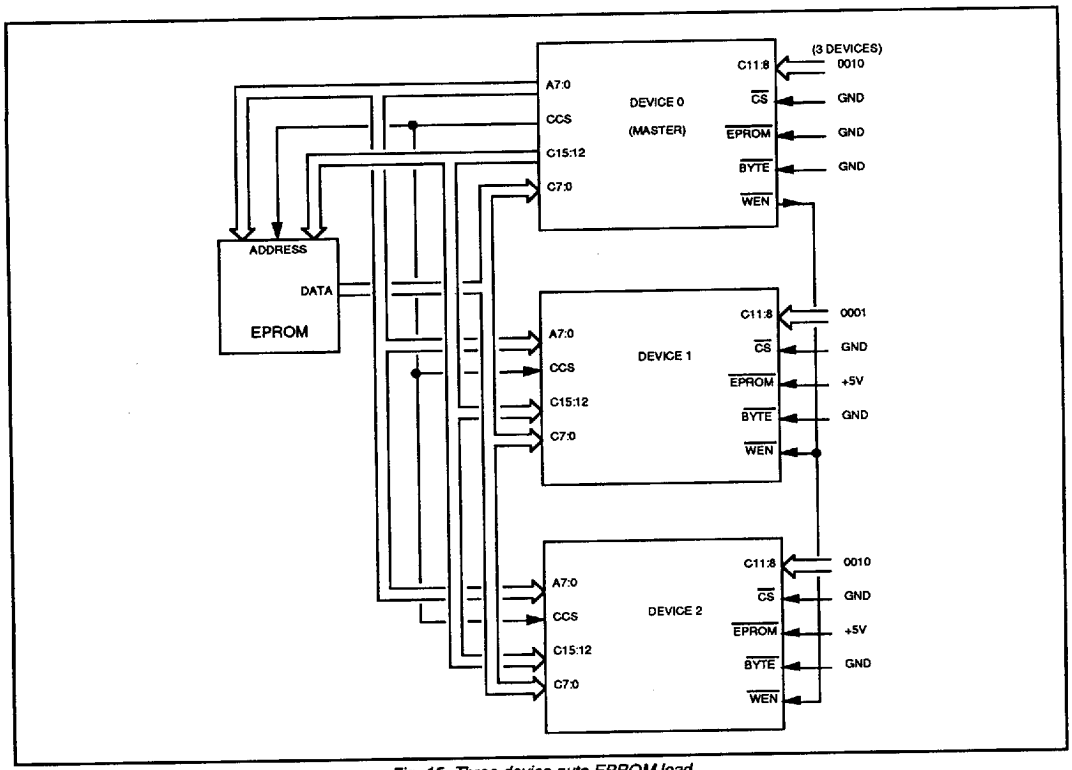

Fig. 15 Three device auto EPROM load

must also drive the address inputs on the slave devices.

When the filter length is less than the maximum, the PDSP16256 will only transfer the correct number of coefficients, and one or more significant address bits will remain low. Sufficient coefficients are always loaded to allow for a possible Bank Swap to occur, and the EPROM allocation must allow for this even if the feature is not to be used. Table 5 shows the number of coefficients loaded for each of the modes.

If several devices are cascaded, only one device assumes the role of the Master by having its EPROM pin grounded. It produces a Write Enable signal for the other devices, plus four higher order address outputs on C15:12. The extra address bits on C15:12 define separate areas of EPROM, containing coefficients for up to fifteen additional devices. The least significant block of memory must always be allocated to the Master device. The additional devices need not in practice be all part of the same cascaded chain, but can consist of several independent filters. They must, however, all have their BYTE pins tied low.

When one EPROM is supplying information for several devices, some means of selectively enabling each additional device must be provided. This is achieved by using the C11:8 pins on the slave devices as binary coded inputs to define one to fifteen extra devices. These coded inputs always correspond to the block address used for the segment of EPROM allocated to that device. Code 'all zeros' must not be used since the Master device has implied use of the bottom segment. This is necessary since the C11:8 pins are alternatively used on the Master device to define the number of devices supported by the EPROM.

In addition to providing the most significant addresses to the EPROM, the C15:12 address outputs from the master device must also drive the C15:12 inputs on the slave devices. These C15:12 inputs are internally compared to the C11:8 inputs to decide if that device is currently to be loaded. This approach avoids the need for external decoders and makes the Chip Enable input redundant. This input, however, must be tied low on every device in an EPROM supported system.

The Control Coefficient pin (CCS) is used to define when the control register is to be loaded. It becomes an output on the Master device which provides an EPROM address bit next in significance above A7:0, and also drives the CCS inputs on the slave devices. This output is high for the first two EPROM transfers in order to access the control information, and then remains low whilst the coefficients are loaded. This control information is thus not stored adjacent to the coefficients within the EPROM, and in fact the EPROM must provide twice the storage necessary to contain the coefficients alone. All but two of the bytes in the additional half are redundant. See Fig.16 for the EPROM memory map.

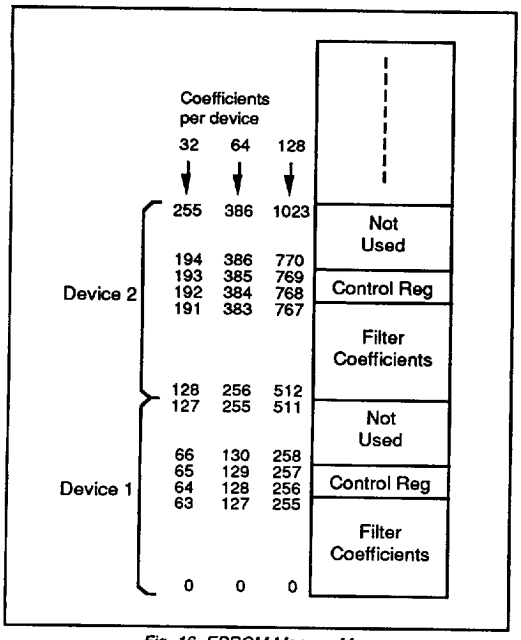

Fig. 16 EPROM Memory Map

Control Register 14 13 12	Number of Coefficients Loaded
0 0 0	32
0 0 1	64
0 1 0	64
0 1 1	128
1 0 0	128
1 0 1	128
1 1 0	128
1 1 1	Invalid Mode

Table 5. Number of Coefficients loaded

NOTE the EPROM memory map Fig. 16 assumes that, for the 32 and 64 coefficient per device options, that the unused address pins are unconnected. If all address pins are connected as shown in Fig. 15 then the 128 coefficients per device memory map column should be used. Only those coefficients required will be read, hence the upper portions of the coefficient address space will be ignored.

USING A REMOTE MASTER

When a remote master is used to load coefficients, the EPROM pin must be tied high and a conventional peripheral interface is then provided. It is not possible, however, to read coefficients already stored. The master supplies an address and data bus, and writes to the PDSP16256 occur under the control of synchronous Chip Enable and Write Strobe inputs. The Coefficient Control Register pin (CCS) must be driven by a master address line higher in significance than A7:0. Both the WEN and CS signals must be low for the load operation to occur. When loading the control register the CS signal must be held low for a further 2 cycles see Fig. 17. Since the internal write operation is actually performed with the system clock, it is necessary for the clock to be present during the transfer.

The BYTE input defines whether coefficients are loaded as a single 16 bit word or two 8 bytes. The latter saves on connections to the remote master. Address bits A7:0 are used in BYTE mode. 16 bit word mode uses bits A6:0, A7 being redundant. When writing in byte mode the least significant byte (A0 = 0) must be written first followed by the most significant byte (A0 = 1).

In the byte mode of working the internal comparison between C15:12 and C11:8 is made, regardless of the state of the EPROM pin. For this reason pins C15:8 should all be tied low when a remote master is used with byte transfers. This ensures that the internal comparison gives equality and allows the load operation to occur.

The address and coefficient busses plus the Write Enable and CS signals must all meet the specified set up and hold times with respect to the system clock, see Fig 17. This synchronous interface is optimum for the majority of high end applications, when individual coefficients must be updated at sample clock rates. If, for convenience reasons, the coefficients are loaded under software control from a general purpose microprocessor, the Write Enable will probably be asynchronous to the system clock used by the PDSP16256. In this case external synchronising logic is needed, see Fig.18.

Fig. 19 shows the recommended loading sequence and filter operation initiation. The simplest technique is to reset the device prior to loading a set of coefficients. Coefficients may be loaded once BUSY returns low or 22 cycles after RESET is taken high.

When loading a device from a remote master the control register must be loaded first followed by the filter coefficients. Fig. 19 shows the required loading sequence, two examples are given one for byte mode the other for word mode. A gap of at least one cycle must be left after loading the control register before loading the first coefficient.

Filter operations are started by presenting the first data word at the same time as raising signal FEN.

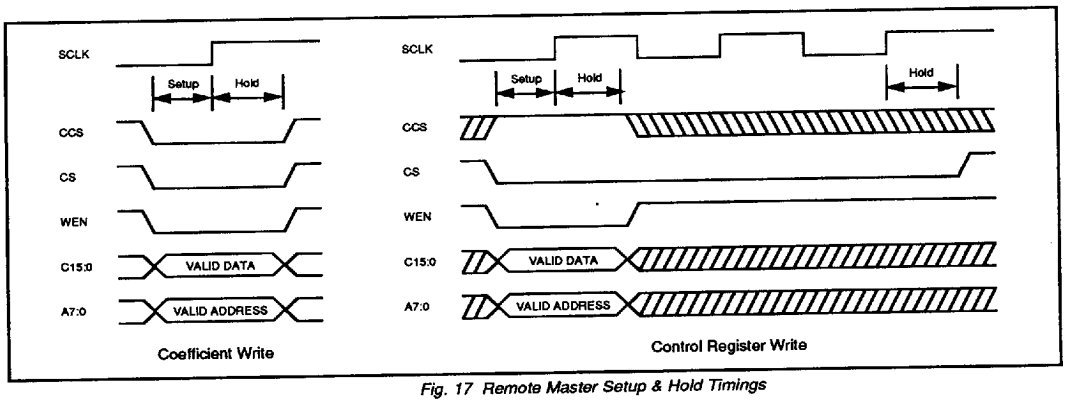

Fig. 17 Remote Master Setup & Hold Timings

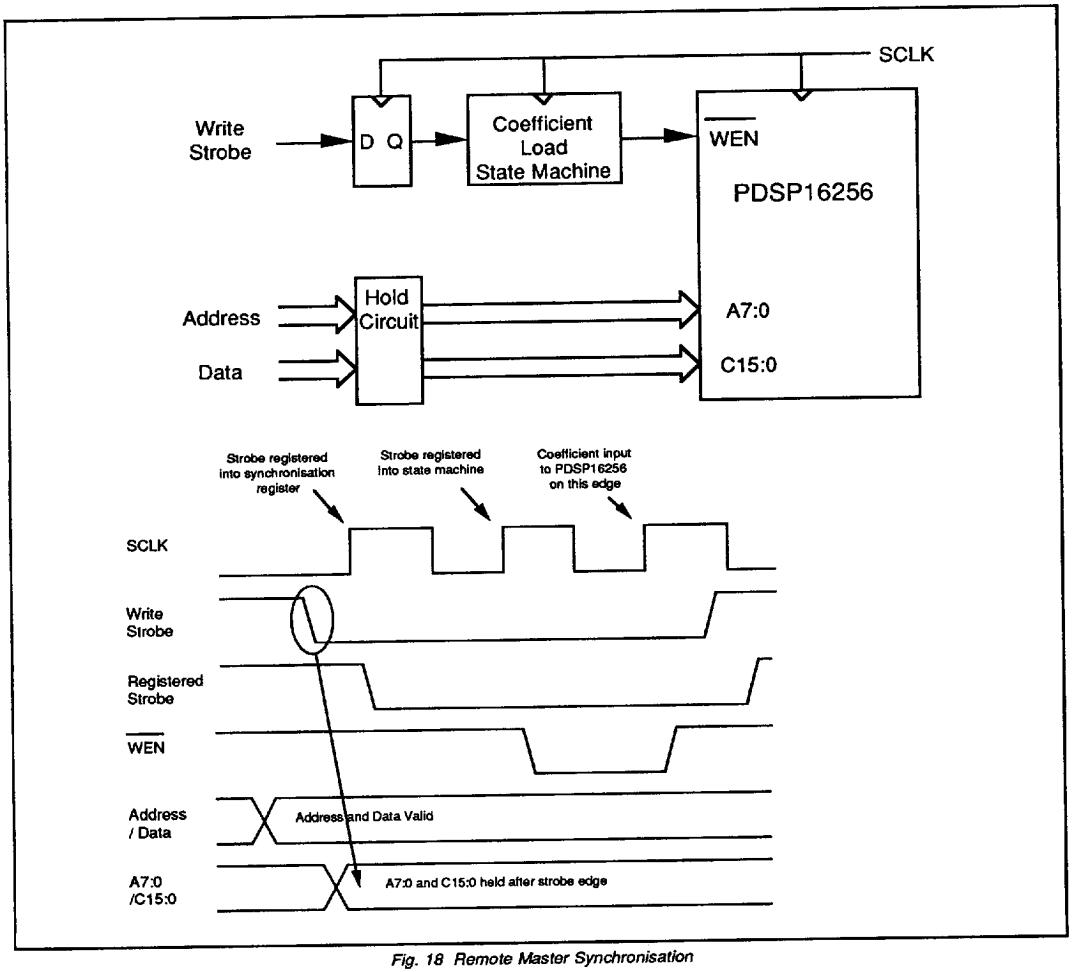

Fig. 18 Remote Master Synchronisation

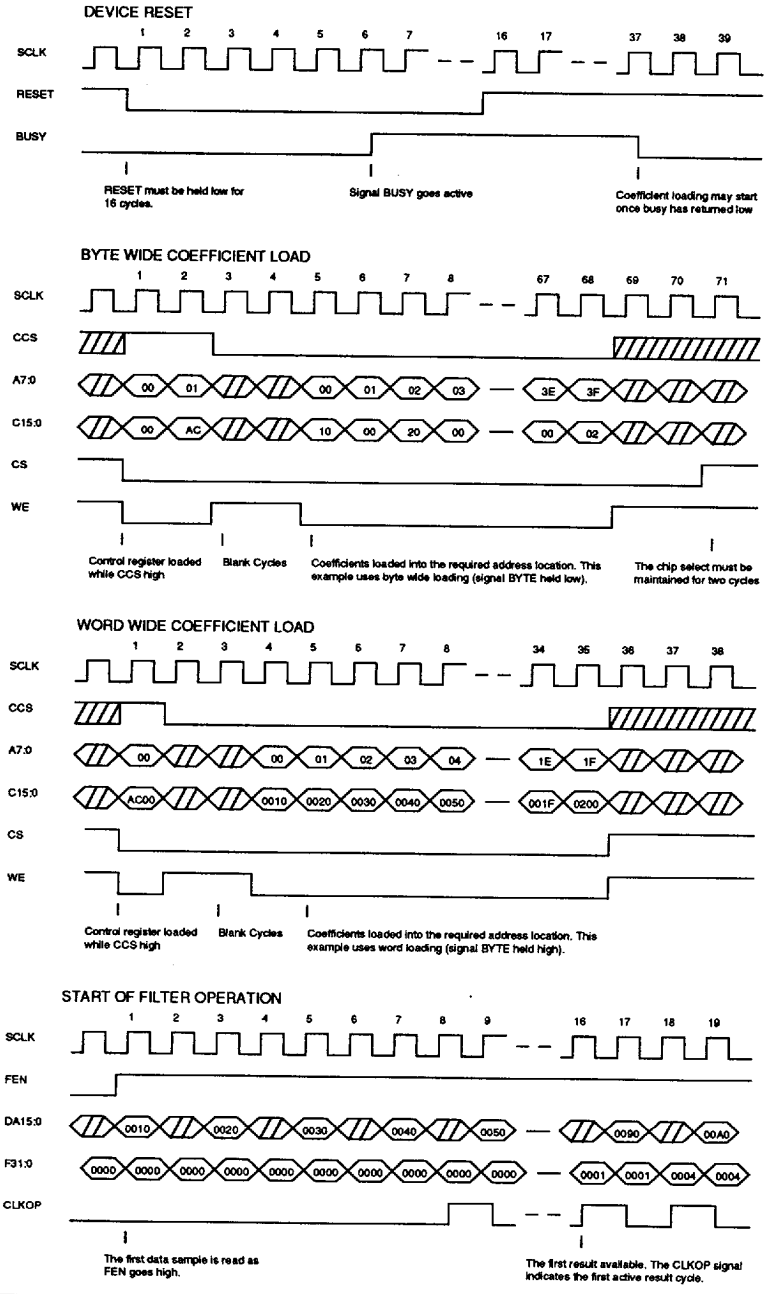

Fig. 19 Device Startup

CONTROL REGISTER

The internal operation of the PDSP16256 is controlled by the status of a 16 bit control register. In the dual filter modes both networks are controlled by the same register. The significance of the various bits are shown in Table 6. Tables 7 and 8 define the control register bit interdependence for the filter and bank swapping modes.

The control register is double buffered. This allows the writing of a new control word without affecting the current operation of the device. To activate the new control register after it has been written to the device the bank swap signal must be toggled. After a reset the active control register is loaded directly and bank swap need not be used.

Control Register Bits		Function
15	4	
0	0	Two independent filters
0	1	Two filters in cascade
1	X	Single Filter

Table 7 Control Register Filter Mode Bits

Control Register Bits			Function
7	6	5	
0	X	0	Control by input pin
1	0	0	Lower bank selected
1	1	0	Upper bank selected
X	X	1	Swap on every sample clock

Table 8 Control Register Bank Swap bits

Bits	Decode	Function
15	0	Dual filter mode
15	1	Single filter mode
14:13	00	Sample rate is the system clock
14:13	01	Sample rate is half the system clock
14:13	10	Sample rate is quarter the system clock
14:13	11	Sample rate is eighth the system clock
12	0	Output rate equals the input rate
12	1	Decimate bt two
11:10	00	Intermediate device
11:10	01	Interface device
11:10	10	Termination device
11:10	11	Single device
9:8	00	These bits MUST be at logical zero
7	0	Bank swap is controlled by input pin
7	1	Bank swap is controlled by Bit 6
6	0	Lower bank if Bit 7 is set
6	1	Upper bank if Bit 7 is set
5	0	Normal Bank Swap
5	1	Bank swap on every sample clock
4	0	Two independent filters
4	1	Two filters in cascade
3:0		These bits MUST be at logical zero

Table 6. Control Register Bit Allocation

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	-55°C to +125°C
Junction temperature with power applied T_J	150°C
Package power dissipation	3000mW
Thermal resistances	
Junction to Case $ø_{JC}$	5°C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device
5. Vcc = Max, Outputs Unloaded, Clock Freq = Max
6. The $ø_{JC}$ data assumes that heat is extracted from the top face of the package.

ELECTRICAL CHARATERISTICS

Operating Conditions (unless otherwise stated)

Commercial:	T_{AMB} = 0°C to +70°C	$T_{J(MAX)}$ = 100°C	Vcc = 5.0V±5%	Ground = 0V
Industrial:	T_{AMB} = -40°C to +85°C	$T_{J(MAX)}$ = 110°C	Vcc = 5.0V±10%	Ground = 0V
Military:	T_{AMB} = -55°C to +125°C	$T_{J(MAX)}$ = 150°C	Vcc = 5.0V±10%	Ground = 0V

Static Charateristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage (CMOS)	V_{IH}	3.5		-	V	SCLK input only
Input low voltage (CMOS)	V_{IL}	-		1.0	V	SCLK input only
Input high voltage (TTL)	V_{IH}	2.0		-	V	All other inputs
Input low voltage (TTL)	V_{IL}	-		0.8	V	All other inputs
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{OS}	10		300	mA	V_{CC} = Max

Switching Characteristic	Commercial		Industrial		Military		Units	Conditions
	Min.	Max.	Min.	Max.	Min.	Max.		
Input signal setup to clock rising edge	8	-	8	-	8	-	ns	
Input signal hold after clock rising edge	4	-	4	-	4	-	ns	
OEN setup to clock rising edge	20	-	20	-	20	-	ns	
OEN hold after clock rising edge	4	-	4	-	4	-	ns	
Clock rising edge to output signal valid	5	26	5	28	5	28	ns	30pF
Clock Frequency	-	25	-	20	-	20	MHz	
Clock High Time	18	-	20	-	20	-	ns	
Clock Low Time	11	-	12	-	12	-	ns	
Clock to data valid from high impedance	-	30	-	30	-	30	ns	see Fig. 20
Clock to data high impedance	-	30	-	30	-	30	ns	see Fig. 20
Vcc Current	-	320	-	250	-	250	mA	see Note 5

Test	Waveform - measurement level
Delay from output high to output high impedance	V_H 0.5V
Delay from output low to output high impedance	V_L 0.5V
Delay from output high impedance to output low	1.5V 0.5V
Delay from output high impedance to output high	1.5V 0.5V

V_H - Voltage reached when output driven hi(
V_L - Voltage reached when output driven lo\

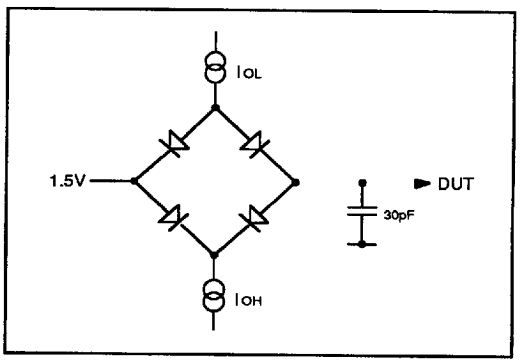

Fig. 20 Three state delay measurement load.

ORDERING INFORMATION

PDSP16256	A0 AC	20MHz, Military, PGA package
PDSP16256	A0 GC	20MHz, Military, QFP package
PDSP16256	B0 AC	20MHz, Industrial, PGA package
PDSP16256	B0 GC	20MHz, Industrial, QFP package
PDSP16256	C0 GC	20MHz, Commercial, QFP package
PDSP16256A	A0 AC	25MHz, Military, PGA package
PDSP16256A	B0 AC	25MHz, Industrial, PGA package
PDSP16256A	C0 AC	25MHz, Commercial, PGA package
PDSP16256A	C0 GC	25MHz, Commercial, QFP package
PDSP16256	MA ACBR	20MHz, MIL-STD-883, PGA package
PDSP16256	MA GCPR	20MHz, MIL-STD-883, QFP package
PDSP16256A	MA GCPR	25MHz, MIL-STD-883, QFP package