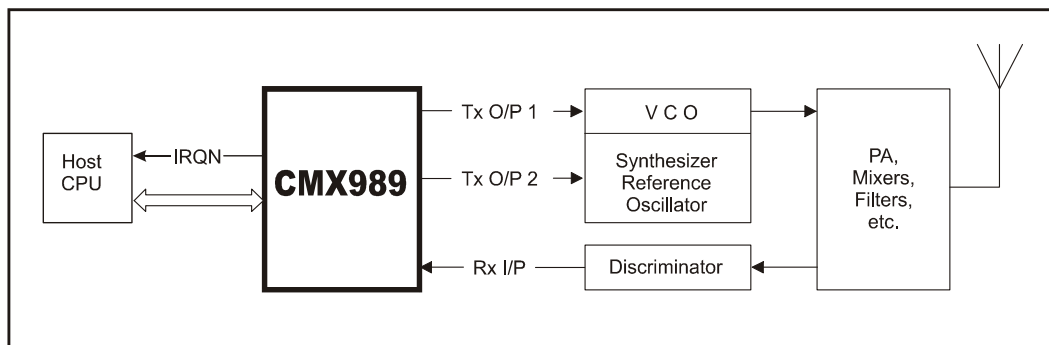


Features

- Reed-Solomon Encoder, Decoder and Error Correction
- MAC and Physical Layer Functions: Minimize Host μ Controller Burden and Power
- Tx and Rx Byte-Wide CDPD Frame FIFOs
- Encapsulates/De-Encapsulates CDPD Frames to/from Over-Air Baseband Signals
- Parallel Bus Hardware Interface to Host CPU
- 2.7V to 5.5V Supply, 28-Pin TSSOP Package

Applications

- CDPD (Cellular Digital Packet Data) Terminals
- PCMCIA/PC-Card Wireless Modem Modules
- Wireless Internet Terminals
- Portable and Mobile Wireless Data Terminals
- Line Power/Battery Applications
- 19.2kbps (BT = 0.5) Full Duplex GMSK Data Modems



The highly integrated CMX989 CDPD MAC and Data Pump Processor integrates complex CDPD MAC and physical layer functions to serve as a core engine for high performance, low power CDPD terminal designs. MAC layer functions decouple the host CPU from the CDPD airlink to simplify and reduce CDPD protocol stack programming, free CPU capacity for applications, eliminate interface components, and allow CPU sleep time for power savings. Physical layer functions mate MAC layer to baseband radio signals with minimal host involvement. MAC and physical layer functions are intelligently coupled to meet airlink timing requirements. For example: Tx emissions automatically start in synchronization with Forward Channel busy/idle status. The Rx CDPD frame FIFO is automatically managed to wait for valid synchronization to occur when first started and after lost signal recovery.

The radio interface supports simple, low cost, VCO-based RF modulators and discriminator-based receivers. Independent, programmable gain Tx outputs are provided for software trimming and balancing of modulating signals.

The host CPU interface is FIFO based and organized in CDPD frames, to provide a simple programming interface with low service latency requirements. Over-the-air frames are automatically encapsulated and de-encapsulated and include complete Reed-Solomon encoding, decoding and error correction, color code insertion and related functions. Device status bits are accessible and may be individually configured to interrupt the host via the parallel hardware interface. The CMX989 operates from a 2.7V to 5.5V supply over -40 to 85°C and comes in a 28-pin TSSOP package (CMX989E1)

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Note:

This product is in development: Changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues.

Information in this data sheet should not be relied upon for final product design.

MX-COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

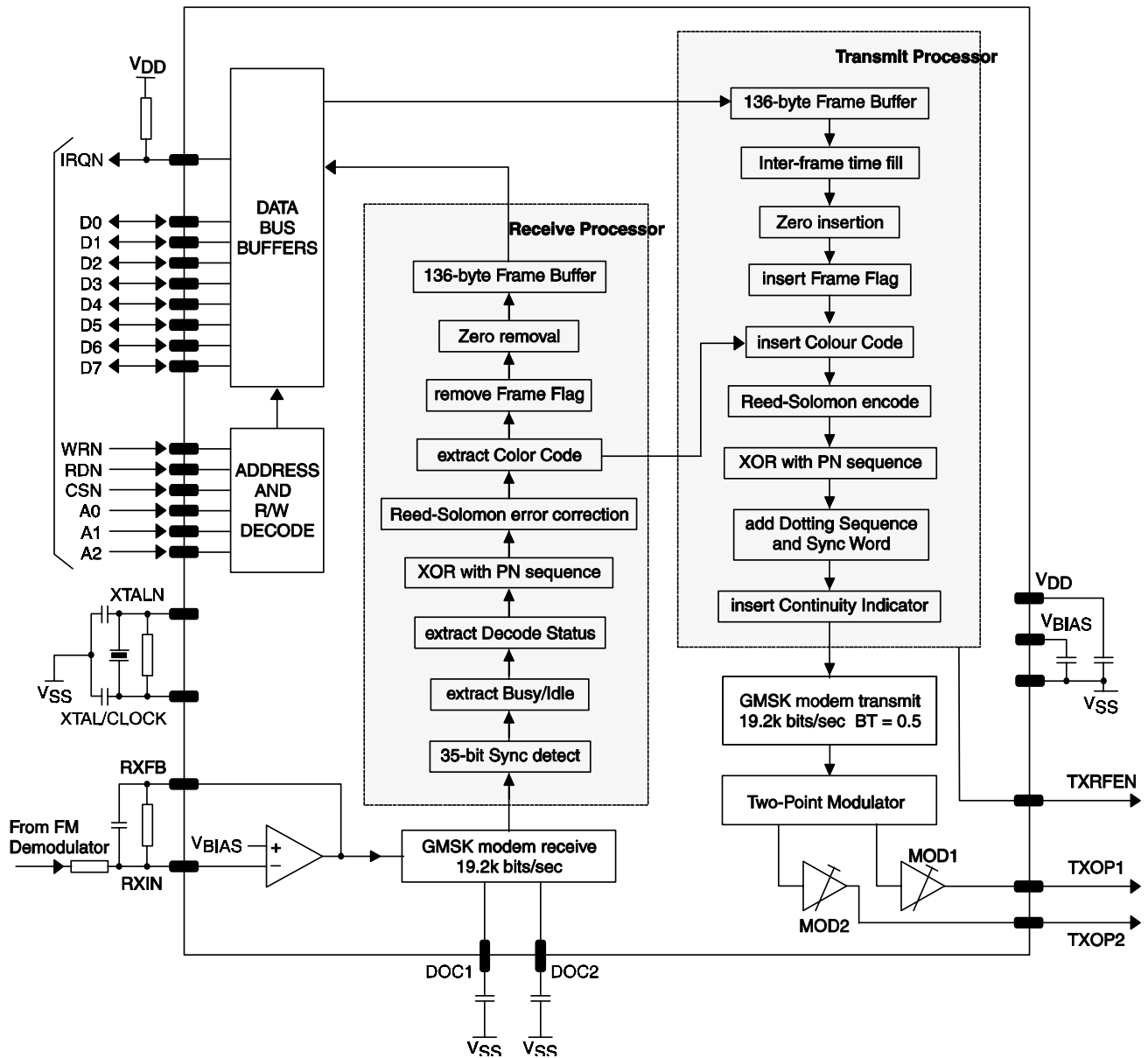


Figure 1: Block Diagram

2. Signal List

Package E1	Signal		Description
Pin No.	Name	Type	
1	XTALN	O/P	The output of the on-chip oscillator
2	XTAL/CLOCK	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock
3	IRQN		A 'wire-ORable' output for connection to the host μ Controller's Interrupt Request input. This output has a low impedance pull down to V_{SS} when active and is high impedance when inactive.
4	D7	BI	8-bit bi-directional 3-state μ Controller interface data lines
5	D6	BI	
6	D5	BI	
7	D4	BI	
8	D3	BI	
9	D2	BI	
10	D1	BI	
11	D0	BI	
12	RDN	I/P	Read. An active low logic level input used to control the reading of data from the device into the host μ Controller.
13	WRN	I/P	Write. An active low logic level input used to control the writing of data into the device from the host μ Controller.
14	V_{SS}	Power	The negative supply rail (ground).
15	DOC 2	O/P	Connections to the Rx level measurement. circuitry. A capacitor should be connected from each pin to V_{SS} .
16	DOC 1	O/P	
17	V_{BIAS}	O/P	A bias line for the internal circuitry, held at $\frac{1}{2} V_{DD}$. This pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
18	RXFB	O/P	The output of the Rx input amplifier and the input to the Rx filter.
19	RXIN	I/P	The input to the Rx input amplifier.
20	N/C		No internal connection, do not use.
21	TXOP2	O/P	Two-point modulator signal output from the device. TXOP2 is in-phase with TXOP1.
22	TXOP1	O/P	
23	TXRFEN	O/P	Tx RF enable. Control line to enable an external RF power amplifier stage. This signal is also available via the parallel μ Controller interface.
24	A2	I/P	Three logic level register select inputs.
25	A1	I/P	
26	A0	I/P	
27	CSN	I/P	Chip Select. An active low logic level input to the device, used to enable a data read or write operation.
28	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor.

Notes:

I/P	=	Input
O/P	=	Output
BI	=	Bidirectional 3-state Input/Output
NC	=	No Connection

3. External Components

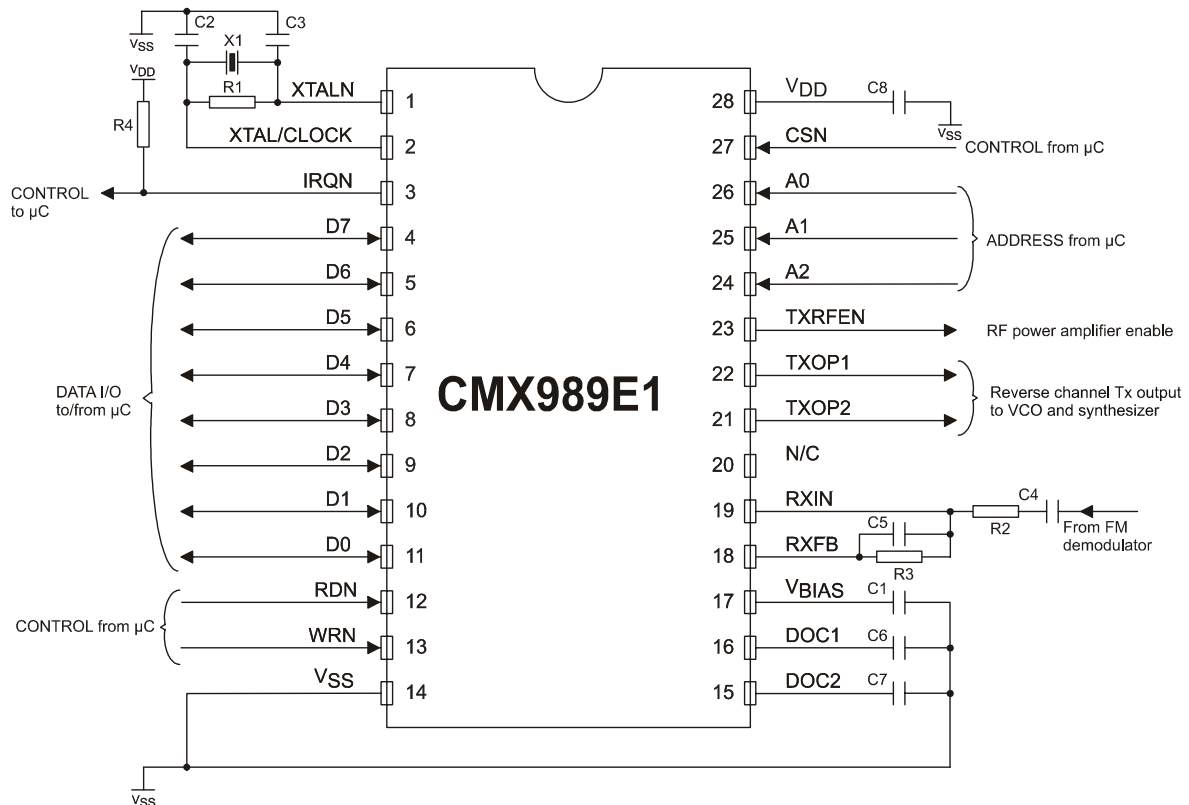


Figure 2: Recommended External Components

3.1 Typical Values:

R1	1MΩ	± 5%
R2	Note 1	± 10%
R3	100kΩ	± 10%
R4	100kΩ	± 10%
X1	4.9152 MHz	(ref. Section 6.1)
C1	0.1µF	± 20%
C2	33pF	± 20%

C3	33pF	± 20%
C4	0.1µF	± 20%
C5	100pF	± 20%
C6	6.8nF	± 20%
C7	6.8nF	± 20%
C8	0.1µF	± 20%

Notes:

- R2, R3, C4 and C5 form the gain components for the Rx INPUT. R2 should be chosen as required by the signal input level, using the following formula:

$$\text{Gain} = -R3/R2$$

- Connections labeled 'N/C': No internal connection, do not use.

To achieve good noise performance it is very important to decouple V_{DD} and V_{BIAS} and to protect the receive path from extraneous in-band signals. It is recommended that the printed circuit board is laid out with a ground plane in the CMX989 area to provide a low impedance connection between the V_{SS} pin and the V_{DD} and V_{BIAS} decoupling capacitors. It is also important to provide a low impedance connection between the Xtal capacitors (C1 and C2) and the ground plane.

4. General Description

This device performs the data encapsulation and synchronization functions of the Medium Access Control (MAC) layer part of the CDPD specification, as well as the generation of baseband signals in the physical layer, all of which are specifically for the Mobile End Station (M-ES). For details of the system requirements and telegram formats, the user is referred to "Cellular Digital Packet Data System Specification" (Release 1.1), Volumes 1 to 5, currently available from:

CDPD Industry Input Coordinator
 Cellular Digital Packet Data System Specification
 650 Town Center Drive, Suite 820
 Costa Mesa, CA 92626
 United States of America

4.1 Principles of Operation

The CMX989 functions (as shown in the block diagram of Figure 1) may be accessed and/or controlled via memory mapped 8-bit registers connected to the host μ Controller parallel bus interface. Write registers allow the device to be set up, controlled and used for transmission of data. Read registers allow received data to be read and the status of the CMX989 to be monitored. There are several registers which can be used to assist end-product manufacture and test and related system test.

It is assumed that many applications will be assisted by the use of interrupt routines, so various functions within the device will cause a hardware interrupt, e.g.: when received data is available to be read or space is available to write data for transmission. Each hardware interrupt source may be individually disabled (masked) or enabled. The interrupt pin (IRQN) is reset high by a read of either IRQ FLAGS or IRQ FLAGS 2 registers and the bits read from these registers and the STATUS register reflect the status of the CMX989 at the time the read is performed. The IRQ FLAGS, IRQ FLAGS2 and STATUS registers can be polled (without the use of a hardware interrupt routine call) if this is preferred.

For reference, the structures of the Reverse and Forward Channel transmissions are shown in Figure 3 and Figure 4.

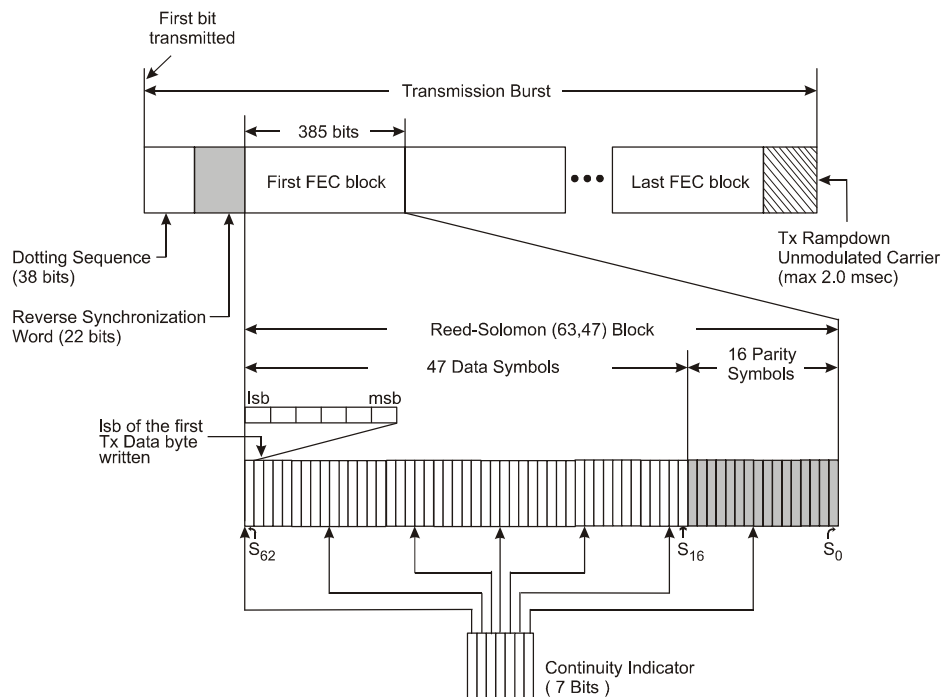


Figure 3: Reverse Channel Transmission Structure

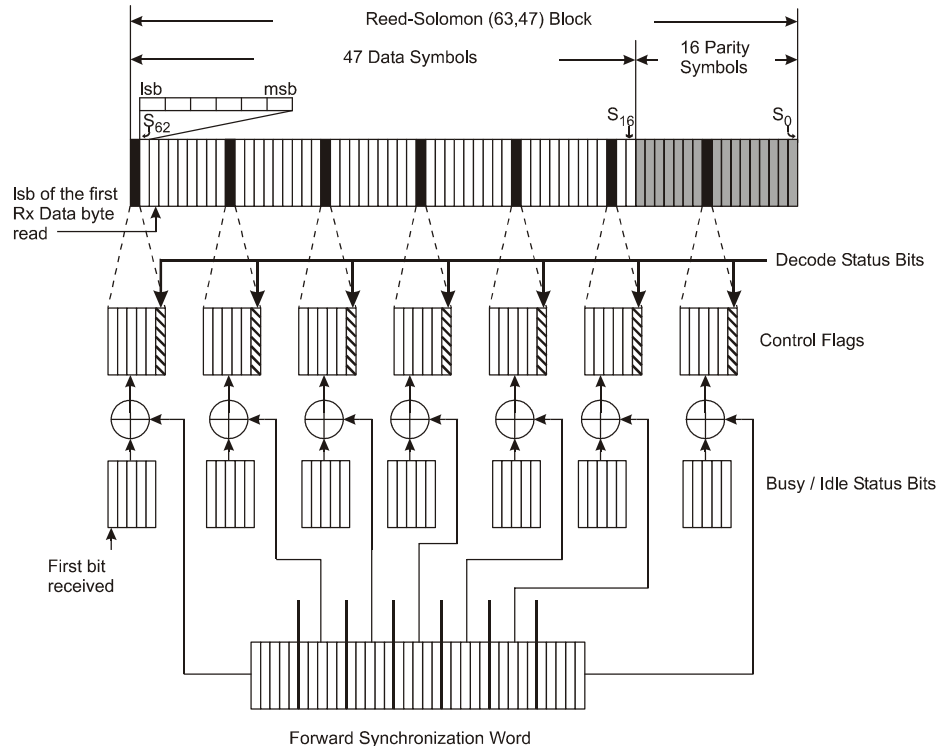


Figure 4: Forward Channel Transmission Structure

4.2 Detailed Function List

4.2.1 Separate 141-byte Tx and Rx data buffers, organized as byte-wide CDPD frame FIFOs

- Large enough to hold an entire maximum length (136-byte) CDPD frame
- Decouples host CPU and CDPD airtlink to provide opportunities for CPU powersave and relaxed service routine timing requirements
- Rx management automatically flushes erroneous frames and resynchronizes Rx buffer on valid frame synchronization
- Empty/full status
- Tx frames are written byte-by-byte style and separated from subsequent frames by writing to an end of frame marker
- Rx frames are read byte-by-byte with each frame boundary indicated by an IRQ and related status
- Read and write status/IRQ handshake paces each byte transferred to and from FIFOs

4.2.2 Encapsulates/de-encapsulates CDPD frames to/from over-air signal systems

- Completed Reed-Solomon block encode and decode with automated 'fill' function for partially filled Tx blocks
- Color Code automatically extracted from Rx stream and inserted into Tx stream
- Pseudo-random number scrambling
- Status flags available for reading or to IRQ on: number of errors corrected in Rx Reed-Solomon block, number errors in forward sync word, Rx busy/idle, Rx Color Code, MDDBS decode, etc.

4.2.3 19.2kbps (BT = 0.5) GMSK modem data pump

- Discriminator Rx interface
- Rx frame synchronization recognizer triggers internal 'upper layer' processing
- Intelligent Tx emission triggering:
 - Tx emission start is synchronized to Rx Busy/Idle flag timing
 - Tx FIFO may be loaded before issuing an emission request or emission request may be issued first and remains pending until Tx FIFO is loaded with enough data to generate a Reed-Solomon block
 - Host μ Controller and TXRFEN signals available to enable ramp-up and ramp-down control of external RF power amplifier stage
- Dual, independent gain controlled Tx outputs for low frequency response transmit VCO architecture

4.3 Software Description

4.3.1 Write Only Registers

Register Address			Register Name	Function							
A2	A1	A0	Write to Modem	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	TX DATA BUFFER	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	TX COLOR CODE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	TX CONTROL	0	0	0	FORCE COLOR CODE	ENDSEQ	ENDFRM	START	ENABTX
0	1	1	RX CONTROL	RESET	0	0	ZERO POWER	ENABRX	← SYNC ERROR LIMIT →		
1	0	0	RX MODEM CONTROL	0	0	LEVRES		AQLEV	AQBC	PLLBW	
1	0	1	TX MODEM CONTROL	← MOD 2 GAIN →				← MOD 1 GAIN →			
1	1	0	IRQ MASK	SYNCM	DECM	IDLEM	TXM	COLORM	ERRM	RXM	RXFRMM
1	1	1	IRQ MASK 2	BLKRDYM	0	RXDEBUG	TXWITHNORX	TXRFM	RXPULSE	RX Bit 1	RX Bit 0

4.3.2 Read Only Registers

Register Address			Register Name	Function							
A2	A1	A0	Read from Modem	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	RX DATA BUFFER	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	RX COLOR CODE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	STATUS	SYNC	DEC	IDLE	0	TXRFEN	ERR	0	0
0	1	1	IRQ FLAGS	SYNCF	DECF	IDLEF	TXF	COLORF	ERRF	RXF	RXFRMF
1	0	0	RX ERROR DATA	← CORRECTED ERRORS →				OVER8	← SYNC ERRORS →		
1	0	1	IRQ FLAGS 2	BLKRDYF	ENV	EOPN	0	TXRFF	0	0	0
1	1	0	*** reserved ***	0	0	0	0	0	0	0	0
0	1	1	*** reserved ***	0	0	0	0	0	0	0	0

4.3.3 Write Only Register Description

4.3.3.1 TX DATA BUFFER Register (Hex address \$00)

This is a write only register of the Tx Data Buffer. It should be written in response to a TXF IRQ FLAG being set to "1". Bit 7 is the msb. The interval between TXF interrupts varies from approximately 16µs to 22ms, depending on the position within the internal data processing sequence.

4.3.3.2 TX COLOR CODE Register (Hex address \$01)

This is a write only register of the Tx Color Code. This value for the Tx Color Code is used when the FORCE COLOR CODE (Bit 4 of the TX CONTROL register) bit is set to "1". Bit 7 is the msb.

4.3.3.3 TX CONTROL Register (Hex address \$02)

(Bits 7,6 and 5)	Unused, set to "0"
FORCE COLOR CODE (Bit 4)	When this bit is "1" the Color Code transmitted in the first block of the Reverse Channel will be the byte defined in the TX COLOR CODE register. When this bit is "0" the Color Code transmitted will be the Color Code byte previously received on the Forward Channel and recorded in the RX COLOR CODE read-only register.
ENDSEQ (Bit 3)	Write a "1" to this bit when the last byte of the last frame in the sequence has loaded.
ENDFRM (Bit 2)	At the end of every frame (2-136 bytes) write a "1" to this bit.
START (Bit 1)	Write a "1" to this bit to start the transmission on the Reverse Channel at the next available slot.
ENABTX (Bit 0)	When this bit is "1" the Tx (Reverse Channel) is enabled. When this bit is "0" the Tx (Reverse Channel) is disabled and enters a powersave condition. In this condition the TXOP1 and TXOP2 outputs are at V_{BIAS} .

4.3.3.4 RX CONTROL Register (Hex address \$03)

RESET (Bit 7)	Write a "1" followed by a "0" to this bit just after power up to initialize the device into a zero-power and "safe" condition.
(Bits 6 and 5)	Unused, set to "0".
ZERO POWER (Bit 4)	When this bit is set to "0" the whole device is disabled and set to minimum power including the crystal oscillator. Allow 20ms for the crystal oscillator to stabilize when coming out of this zero-power state.
ENABRX (Bit 3)	When this bit is "1" the Rx (Forward Channel) is enabled. When this bit is "0" the Rx (Forward Channel) is disabled and enters a powersave condition.
SYNC ERROR LIMIT (Bits 2, 1 and 0)	This 3-bit number specifies the greatest number of bits that can be in error in the synchronization word. Bit 2 is the msb. If the synchronization word is recognized with less than or equal to this number of errors, the SYNC CF bit is set to "1" and the actual number of errors is loaded into SYNC ERRORS (Bits 2, 1 and 0 of the RX ERROR DATA register). The RXDATA in that block is then processed.

4.3.3.5 RX MODEM CONTROL (Hex address \$04)

This register is for test purposes only and should be set to all "0s" for normal operation.

(Bits 7 and 6)	Unused, set to "0"																				
LEVRES (Bits 5 and 4)	<p>These two bits set the response time of the Rx signal amplitude and dc offset measuring circuits according to the table below:</p> <table border="1"> <thead> <tr> <th>B5</th> <th>B4</th> <th>Setting</th> <th>Action</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Peak Averaging</td> <td>Track input signal using bit peak averaging</td> </tr> <tr> <td>0</td> <td>1</td> <td>Peak Detect</td> <td>Track input signal using peak detect</td> </tr> <tr> <td>1</td> <td>0</td> <td>Lossy Peak Detect</td> <td>Track input signal using lossy peak detection</td> </tr> <tr> <td>1</td> <td>1</td> <td>Hold</td> <td>Keep current values of amplitude and offset</td> </tr> </tbody> </table>	B5	B4	Setting	Action	0	0	Peak Averaging	Track input signal using bit peak averaging	0	1	Peak Detect	Track input signal using peak detect	1	0	Lossy Peak Detect	Track input signal using lossy peak detection	1	1	Hold	Keep current values of amplitude and offset
B5	B4	Setting	Action																		
0	0	Peak Averaging	Track input signal using bit peak averaging																		
0	1	Peak Detect	Track input signal using peak detect																		
1	0	Lossy Peak Detect	Track input signal using lossy peak detection																		
1	1	Hold	Keep current values of amplitude and offset																		
This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.																					
AQLEV (Bit 3)	<p>Whenever the AQLEV bit is set to "1" it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, hence improving the measurement accuracy, until the 'normal' value set by the LEVRES bits is reached.</p> <p>Setting this bit to "0" (or changing it from "1" to "0") has no effect.</p>																				
AQBC (Bit 2)	<p>Whenever the AQBC bit is set to "1" it initiates an automatic sequence designed to achieve bit timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits.</p> <p>Setting this bit to "0" (or changing it from "1" to "0") has not effect.</p>																				
PLLBW (Bits 1 and 0)	<p>These two bits set the bandwidth of the Rx clock extraction PLL circuit according to the table below:</p> <table border="1"> <thead> <tr> <th>B1</th> <th>B0</th> <th>PLL Bandwidth</th> <th>Suggested Use</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Medium</td> <td>Wide tolerance Xtals or long preamble acquisition</td> </tr> <tr> <td>0</td> <td>1</td> <td>Wide</td> <td>Quick acquisition</td> </tr> <tr> <td>1</td> <td>0</td> <td>Narrow</td> <td>±20ppm or better Xtals</td> </tr> <tr> <td>1</td> <td>1</td> <td>Hold</td> <td>Signal fades</td> </tr> </tbody> </table>	B1	B0	PLL Bandwidth	Suggested Use	0	0	Medium	Wide tolerance Xtals or long preamble acquisition	0	1	Wide	Quick acquisition	1	0	Narrow	±20ppm or better Xtals	1	1	Hold	Signal fades
B1	B0	PLL Bandwidth	Suggested Use																		
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1	0	Narrow	±20ppm or better Xtals																		
1	1	Hold	Signal fades																		
This setting will be temporarily overridden by the automatic sequencing of an AQBC command.																					

4.3.3.6 TX MODEM CONTROL Register (Hex address \$05)

<p>MOD 2 GAIN (Bits 7, 6, 5 and 4)</p>	<p>These bits control the amplitude of the TXOP2 output according to the table below.</p> <table border="1" data-bbox="623 235 1258 810"> <thead> <tr> <th>(Bit 7)</th> <th>(Bit 6)</th> <th>(Bit 5)</th> <th>(Bit 4)</th> <th>GAIN (dB)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>OFF (o/p at VBIAS)</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>-5.6</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>-5.2</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>-4.8</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>-4.4</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>-4.0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>-3.6</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>-3.2</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>-2.8</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>-2.4</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>-2.0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>-1.6</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>-1.2</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>-0.8</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>-0.4</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0.0</td></tr> </tbody> </table>	(Bit 7)	(Bit 6)	(Bit 5)	(Bit 4)	GAIN (dB)	0	0	0	0	OFF (o/p at VBIAS)	0	0	0	1	-5.6	0	0	1	0	-5.2	0	0	1	1	-4.8	0	1	0	0	-4.4	0	1	0	1	-4.0	0	1	1	0	-3.6	0	1	1	1	-3.2	1	0	0	0	-2.8	1	0	0	1	-2.4	1	0	1	0	-2.0	1	0	1	1	-1.6	1	1	0	0	-1.2	1	1	0	1	-0.8	1	1	1	0	-0.4	1	1	1	1	0.0
(Bit 7)	(Bit 6)	(Bit 5)	(Bit 4)	GAIN (dB)																																																																																		
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<p>MOD 1 GAIN (Bits 3, 2, 1 and 0)</p>	<p>These bits control the amplitude of the TXOP1 output according to the table below.</p> <table border="1" data-bbox="623 896 1230 1472"> <thead> <tr> <th>(Bit 3)</th> <th>(Bit 2)</th> <th>(Bit 1)</th> <th>(Bit 0)</th> <th>GAIN (dB)</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>OFF (o/p at V_{BIAS})</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>-5.6</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>-5.2</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>-4.8</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>-4.4</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>-4.0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>-3.6</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>-3.2</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>-2.8</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>-2.4</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>-2.0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>-1.6</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>-1.2</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>-0.8</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>-0.4</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0.0</td></tr> </tbody> </table>	(Bit 3)	(Bit 2)	(Bit 1)	(Bit 0)	GAIN (dB)	0	0	0	0	OFF (o/p at V _{BIAS})	0	0	0	1	-5.6	0	0	1	0	-5.2	0	0	1	1	-4.8	0	1	0	0	-4.4	0	1	0	1	-4.0	0	1	1	0	-3.6	0	1	1	1	-3.2	1	0	0	0	-2.8	1	0	0	1	-2.4	1	0	1	0	-2.0	1	0	1	1	-1.6	1	1	0	0	-1.2	1	1	0	1	-0.8	1	1	1	0	-0.4	1	1	1	1	0.0
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4.3.3.7 IRQ Mask Register (Hex address \$06)

These bits prevent interrupts from occurring as detailed below:

SYNCM (Bit 7)	When this bit is set to "1" the SYNC interrupt will be gated out to the IRQN pin. When this bit is set to "0" the SYNC interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
DECM (Bit 6)	When this bit is set to "1" the DEC interrupt will be gated out to the IRQN pin. When this bit is set to "0" the DEC interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
IDLEM (Bit 5)	When this bit is set to "1" the IDLE interrupt will be gated out to the IRQN pin. When this bit is set to "0" the IDLE interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
TXM (Bit 4)	When this bit is set to "1" the TX interrupt will be gated out to the IRQN pin. When this bit is set to "0" the TX interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
COLORM (Bit 3)	When this bit is set to "1" the COLOR interrupt will be gated out to the IRQN pin. When this bit is set to "0" the COLOR interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
ERRM (Bit 2)	When this bit is set to "1" the ERR interrupt will be gated out to the IRQN pin. When this bit is set to "0" the ERR interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
RXM (Bit 1)	When this bit is set to "1" the RX interrupt will be gated out to the IRQN pin. When this bit is set to "0" the RX interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
RXFRMM (Bit 0)	When this bit is set to "1" the RXFRM interrupt will be gated out to the IRQN pin. When this bit is set to "0" the RXFRM interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.

4.3.3.8 IRQ MASK 2 Register (Hex address \$07)

This register is the counterpart to IRQ FLAGS 2 register. Apart from TXRFM and possibly BLKRDYM, the bits in this register are mainly for test purposes and should be set to all "0s" for normal operation.

BLKRDYM (Bit 7)	When this bit is set to "1" the BLKRDY interrupt will be gated out to the IRQN pin. When this bit is set to "0" the BLKRDY interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.															
(Bit 6)	Unused, set to "0".															
RXDEBUG (Bit 5)	When this bit is "1" the Rx (Forward Channel) will load data every 420 bits, without detecting a sync word. When this bit is "0" the device operates normally. This bit is normally used for debugging only, but could be used in conjunction with bit error rate measurements.															
TXWITHNORX (Bit 4)	When this bit is "1" the Tx (Reverse Channel) will transmit without waiting for the Rx (Forward Channel) to synchronize as required by the CDPD specification (Release 1.1, Part 402, Section 5.3.1, Figure 402-16). When this bit is "0" the device operates normally.															
TXRFM (Bit 3)	When this bit is set to "1" the TXRF interrupt will be gated out to the IRQN pin. When this bit is set to "0" the TXRF interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.															
RXPULSE (Bit 2)	When the two bits "RX Bit 1" and "RX Bit 0" are set appropriately and this bit has "1" written to it, an internal test sequence will be clocked into the Reed-Solomon decoder and the receiver will output the bits as required by the CDPD specification (Release 1.1, Part 402, Appendix 402-A, Table 402-8).															
RX Bit 1, RX Bit 0 (Bits 1 and 0)	These two bits set the internally generated test sequence for the receiver according to the table below: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Bit 1</th> <th>Bit 0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Normal operation</td> </tr> <tr> <td>0</td> <td>1</td> <td>Test sequence 0 errors</td> </tr> <tr> <td>1</td> <td>0</td> <td>Test sequence 8 errors</td> </tr> <tr> <td>1</td> <td>1</td> <td>Test sequence 9 errors</td> </tr> </tbody> </table>	Bit 1	Bit 0	Function	0	0	Normal operation	0	1	Test sequence 0 errors	1	0	Test sequence 8 errors	1	1	Test sequence 9 errors
Bit 1	Bit 0	Function														
0	0	Normal operation														
0	1	Test sequence 0 errors														
1	0	Test sequence 8 errors														
1	1	Test sequence 9 errors														

4.3.4 Read Only Register Description

4.3.4.1 RX DATA BUFFER Register (Hex address \$00)

This is a read-only register of the receive data buffer. It should be read in response to an RXF IRQ FLAG being set to "1". Bit 7 is the msb. The interval between RXF interrupts varies from approximately 16 μ s to 22ms, depending on the position within the internal data processing sequence.

4.3.4.2 RX COLOR CODE Register (Hex address \$01)

This is a ready-only register of the Color Code on the Rx (Forward Channel). It is updated every time the SYNCF IRQ FLAG is set to "1". Bit 7 is the msb.

4.3.4.3 STATUS Register (Hex address \$02)

This is a read-only register that contains the status of the various functions on the device as described below:

SYNC (Bit 7)	This bit is set to "1" if a Forward Channel synchronization word has been received successfully. (See SYNC ERRORS and SYNC ERROR LIMIT). This bit is reset to "0" when the sync word has not been detected for more than 420 bits (i.e. sync lost).
DEC (Bit 6)	This bit indicates the decode status of the Mobile Data Base Station (MDBS) on the Forward Channel. This bit is set to "1" when the station fails to decode data successfully, and is reset to "0" when the station is successful in decoding data. This bit will only change and be valid if SYNC (Bit 7) is set to "1".
IDLE (Bit 5)	<p>This bit indicates the activity of the Mobile Data Base Station (MDBS) on the Forward Channel. This bit is set to "1" when the station is in an IDLE state, and reset to "0" when the station is in a BUSY state. This bit will only change and be valid if SYNC (Bit 7) is set to "1". The value of this bit is not specified if SYNC (Bit 7) is reset to "0".</p> <p>The IDLE bit is derived from a majority decision on the most recently received group of five consecutive busy/idle bits, as in the CDPD specification (Release 1.1, Part 402, Section 4.5, Figure 402-7).</p> <p>The first block of data received in the Forward Channel will not output any data until the sync word has been found. Once this has been found, the majority decision of the most recent group of busy/idle bits will be output in the STATUS register, and the IDLEF bit will be set to "1" in the IRQ FLAGS register.</p> <p>The next six groups of busy/idle bits generate IDLE bits as they are received and, so long as the sync word remains correct, these successive IDLE bits are output as the groups of busy/idle bits are received.</p>
(Bit 4)	Unused, will be set to "0".
TXRFEN (Bit 3)	This bit is set to "1" approximately two bits (104 μ s) before the dotting sequence leaves TXOP1 or TXOP2 outputs and is reset to "0" at the end of transmission from TXOP1 and TXOP2. This signal is also available as a direct output on the TXRFEN pin, where it can be used to enable an external RF power amplifier stage.
ERR (Bit 2)	<p>This bit indicates whether the data currently being read out from RX DATA BUFFER has any errors. If this bit is set to "1" there are errors that cannot be corrected and the host μController should discard all data in the present frame as that frame cannot be successfully completed. It will then search and re-synchronize to the next frame flag, before making any more data available. When this bit is set to "0" there are no errors in the block currently being read.</p> <p>Note: Due to the CMX989's internal buffer, the data currently being read at the CMX989/μController interface may be up to 5 Reed-Solomon blocks older than the data currently being received at the CMX989/FM demodulator interface.</p>
(Bits 1 and 0)	Unused, will be set to "0".

4.3.4.4 IRQ FLAGS Register (Hex address \$03)

This is a read-only register that contains flags to indicate the source of an interrupt, as described below:

SYNCF (Bit 7)	This bit is set to "1" when the device has decoded the sync word on the Forward Channel. It also is set to "1" if, after detecting sync, it fails to detect it 420 bits later, indicating sync has been lost. The state of the sync can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated, depending on the state of the IRQ MASK register.
DECF (Bit 6)	This bit is set to "1" when the decode status of the Mobile Data Base Station (MDBS) in the Forward Channel changes state. The decode state can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.
IDLEF (Bit 5)	This bit is set to "1" when the idle status of the Mobile Data Base Station (MDBS) in the Forward Channel changes state. The idle state can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.
TXF (Bit 4)	This bit provides handshaking flow control when writing data bytes to the Tx (Reverse Channel) data buffer. It is set to "1" whenever the buffer is not full and new data can be loaded in to the TX DATA BUFFER register. It is reset to "0" after a "write" to the TX DATA BUFFER register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register. The interval between TXF interrupts varies from approximately 16 μ s to 22ms, depending on the position within the internal data processing sequence.
COLORF (Bit 3)	This bit is set to "1" when a color code is successfully received on the Forward Channel and placed in the RX COLOR CODE register. It is reset to "0" after a read of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.
ERRF (Bit 2)	This bit is set to "1" when the ERR status changes. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.
RXF (Bit 1)	This bit provides handshaking flow control when reading data bytes from the Rx (Forward Channel) data buffer. It is set to "1" whenever the buffer is not empty and data is available to be read from the RX DATA BUFFER register. It is reset to "0" after a "read" of the RX DATA BUFFER register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register. The interval between RXF interrupts varies from approximately 16 μ s to 22ms, depending on the position within the internal data processing sequence.
RXFRMF (Bit 0)	This bit is used when reading the receiver data. It is set to "1" when the byte about to be read from the receiver data buffer is the first byte of a new frame. It is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.

4.3.4.5 RX ERROR DATA Register (Hex address \$04)

This is a read-only register that contains receiver performance data.

CORRECTED ERRORS (Bits 7, 6, 5 and 4)	This 4-bit number indicates the number of Reed-Solomon symbol errors before error correction that are in the most recently received 63-symbol Reed-Solomon block. They are updated every time the SYNCF bit is set in the IRQ FLAGS register. Bit 7 is the msb.
OVER8 (Bit 3)	This bit is set to "1" if the most recently received Reed-Solomon block has greater than 8 errors. i.e. the data has too many errors to enable the Reed-Solomon error correction to work. It is updated every time the SYNCF bit is set in the IRQ FLAGS register and is reset to "0" if 8 errors or fewer are encountered.
SYNC ERRORS (Bits 2, 1 and 0)	This 3-bit number indicates the number of errors in the most recently received synchronization word. It is updated whenever the synchronization word is in error less than or equal to the number specified by the SYNC ERROR LIMIT bits of the RX CONTROL register. It also implies the synchronization word has been received successfully and sets the SYNC bit to "1" (See STATUS register above). Bit 2 is the msb.

Note: These bits all refer to the data most recently received at the Rx input and are NOT necessarily the same as previously received and buffered data which is currently being read by the CMX989's host μ Controller.

4.3.4.6 IRQ FLAGS 2 Register (Hex address \$05)

Bits 5 and 6 of this register are for test purposes only and their contents should be ignored during normal operation.

BLKRDYF (Bit 7)	This is the "Block Ready Flag" and is set to "1" when the receiver decodes the currently received Reed-Solomon block. It is reset to "0" after a read of the IRQ FLAGS 2 register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK 2 register.
ENV (Bit 6)	A circuit monitors the DOC voltage levels, which are an indication of the received signal amplitude envelope. If the DOC voltages are more than 6% of V_{DD} apart (0.3V when $V_{DD} = 5.0V$) then this bit will be set to "1". It is reset to "0" when the DOC voltages are less than 6% of V_{DD} apart. Note: The ENV output will also be triggered when receiving high levels of noise or other in-band signals.
EOPN (Bit 5)	A circuit monitors the receive waveform. If the received signal remains close to the centre of the received data levels (as stored on the DOC capacitors) for more than approximately 3 bit-times then this bit will be set to "1". If the input signal level goes towards either of the DOC capacitor values this bit will be set to "0". Note: When a data signal is not being received and the DOC capacitors have discharged or if there are high levels of noise then the value of the EOPN bit will be unreliable and so it should be used in conjunction with the ENV bit.
(Bit 4)	Unused, will be set to "0".
TXRFF (Bit 3)	This bit is set to "1" when the Tx RF enable bit (TXRFEN) changes state. This bit is reset to "0" after a "read" of the IRQ FLAGS 2 register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK 2 register.
(Bits 2, 1 and 0)	Unused, will be set to "0".

5. Application Notes

5.1 Operation Sequence

5.1.1 Power Up

To initialize the registers to a safe, known state, RESET (Bit 7 of the RX CONTROL register) should be set to "1", then set to "0", then set to "1", and then to "0" again. This puts the device into the zero-power mode with all functions disabled and resets the device.

5.1.2 Acquisition of a CDPD channel

The first thing that the device will be required to do is to search for a CDPD Forward Channel data stream.

The sequence below describes how to do this:

1. The likely presence of an Rx data stream (CDPD Forward Channel modulation) may be indicated by the RSSI in a process which is separate from, and external to, the CMX989. Simultaneously, the CMX989 can search for a CDPD Forward Channel synchronization word, as follows:
2. Write "1" to ZERO POWER and "1" to ENABRX (Bits 4 and 3 of the RX CONTROL register) to enable the crystal and the receiver. Also set the SYNC ERROR LIMIT (Bits 2, 1 and 0 of the RX CONTROL register) to a binary value from 0 to 5, depending on the number of errors that can be tolerated in the Forward Channel synchronization word.
3. Write "1" to SYNCM (Bit 7 of the IRQ MASK register) to enable the detection on interrupt of the forward synchronization word.
4. The device will now interrupt when a CDPD Forward Channel synchronization word has been detected. An additional local timer could be set to give a timeout after which the host μ Controller could initiate a change of RF channel to search elsewhere for a CDPD Forward Channel stream.
5. When the interrupt occurs, read the IRQ FLAGS register to confirm and clear the SYNCF flag and read the STATUS register to check the SYNC bit. The SYNCM bit can be left set to "1" as further interrupts would indicate that the device has lost the forward synchronization. Appropriate action should then be taken. However the user may wish to disable it, as the CDPD Reed-Solomon decoder has the ability to indicate when the data has lost its integrity. Loss of the channel or corruption of the data is indicated by errors in the synchronization word and/or errors in a Reed-Solomon decoded data block (RX ERROR DATA register).
6. The RX ERROR DATA register may also be used in the initial acquisition of the channel as detailed in the CDPD specification (Release 1.1, Part 402, Section 3.2.3).

5.1.3 Receive

Having found a CDPD Forward Channel stream, the data can be read using the following sequence:

1. Write a "1" to ERRM, a "1" to RXM and a "1" to RXFRMM (Bits 2, 1 and 0 of the IRQ MASK register), to enable the Rx Error IRQ, the Rx Data IRQ and the Rx Frame Flag IRQ respectively.
2. An RXFRMF interrupt (Bit 0 of the IRQ FLAGS register) indicates that the next byte to be read from the RX DATA BUFFER register is the first byte of a new frame. The contents of the RX DATA BUFFER register prior to the first RXFRMF interrupt event after ENABRX is set to "1" are automatically discarded when the first RXFRMF interrupt occurs. RXF interrupts are also disabled until the first RXFRMF interrupt occurs.
3. Using the RXF interrupt (Bit 1 of the IRQ FLAGS register) as a handshake, data can be read from the device. RXF set to "1" indicates that another byte can be read from the RX DATA BUFFER register. When RXF remains at "0", the buffer is empty. The frame boundaries are indicated by the RXFRMF interrupt (Bit 0 of the IRQ FLAGS register). Note that the host μ Controller should continuously read bytes from the RX DATA BUFFER register and then re-assemble the frame within the host μ Controller's memory, rather than wait for a complete frame (indicated by the next RXFRMF interrupt) before starting data transfer. Since the frame size is not an integer multiple of the block size, overflow will eventually occur if data is only transferred on frame boundaries.
4. If an ERRF interrupt (Bit 2 of the IRQ FLAGS register) and ERR (Bit 2 of the STATUS register) occur, the host μ Controller will be expected to discard the bytes that it has already read from the receiver, which are associated with the unfinished frame. It must then wait for the next Frame flag (RXFRMF) in order to continue. Any unread contents of the RX DATA BUFFER are automatically discarded and no further RXF interrupts will be generated until the next Frame flag (RXFRMF) interrupt occurs.
5. As the device can buffer up to 4 Reed-Solomon blocks i.e. $4 \times 47 \times 6 = 1128$ bits = 141 bytes, in addition to the Reed-Solomon block it is currently decoding, it may be more convenient for the host μ Controller to

use BLKRDYF and BLKRDYM (Bit 7 of the IRQ MASK 2 register and Bit 7 of the IRQ FLAGS 2 register) as a form of counter, such that after 1, 2, 3, or 4 "Block Ready" interrupts, the host μ Controller empties the receive buffer in one go. Since, in this case, there is no way of knowing when the buffer is empty, an external timeout or byte counter is also required.

6. There is no buffer full indication, so if the RX DATA BUFFER register is not sufficiently empty when the fifth block has been processed, the latest received data (i.e. the fourth block) will be overwritten by the just completed fifth block.

5.1.4 Transmit

The host μ Controller then processes the frames and decides upon a reply. Gaining access and replying on the Reverse Channel can be done as follows:

1. Before starting a transmission the COLORF flag (Bit 3 of the IRQ FLAGS register) should be checked to have been set to "1" to ensure the correct Color Code is used on the Reverse Channel (this could be done while also reading the STATUS register during receive).
2. The IDLEF flag (Bit 5 of the IRQ FLAGS register) and the IDLE bit (Bit 5 of the STATUS register) should be checked to see if the Forward Channel is free. If the IDLE bit is "1" the channel is free, if it is "0" then there is communication with another system and the host μ Controller will enter the DEFER state according to the CDPD specification (Release 1.1, Part 402, Sections 5.3.3.1 and 5.3.3.2).
3. With the IDLE bit confirming a free channel, set the desired MOD1 and MOD2 output gains in the TX MODEM CONTROL register, then write "1" to TXRFM (IRQ MASK 2 register, Bit 3) and write "1" to ENABTX (TX CONTROL register, Bit 0). This will take the Tx processing circuits out of powersave, so that blocks of data can then be loaded.
4. Up to 4 Reed-Solomon blocks (i.e. $4 \times 47 \times 6 = 1128$ bits = 141 bytes of data) can be loaded contiguously on a byte-by-byte basis. Before any further data is loaded, the transmission must be started. This is done by writing "1" to START (Bit 1 of the TX CONTROL register), to indicate the start of data, i.e. the dotting sequence, reverse synchronization Color Code (from the Forward Channel) and the first frame byte will automatically be sent before the data in the buffer is despatched.
5. Write the data into the TX DATA BUFFER register a byte at a time, using the IRQN pin and the handshaking of the TXF flag (Bit 4 of the IRQ FLAGS register). TXF set to "1" indicates that another byte can be loaded into the TX DATA BUFFER register. When TXF remains at "0", the buffer is full.
6. At each frame boundary write a "1" to ENDFRM (Bit 2 of the TX CONTROL register).
7. At the end of the transmission sequence, write "1" to ENDSEQ (Bit 3 of the TX CONTROL register). This will fill up the last Reed-Solomon block with "1"s and send it with the continuity indicator set to "0" (see the CDPD specification: Release 1.1, Part 402, Section 4.6.4).
8. The Tx buffer can be kept full and serviced with an interrupt routine. There is no buffer empty indication and failure to provide data after writing the START bit will cause the device to send undefined data. Transmission of data does not begin until one complete block has been loaded into the Tx buffer.
9. The transmission will automatically start within 8 bit-times of the last bit of an idle flag (see the CDPD specification: Release 1.1, Part 402, Section 5.3.1). Approximately two bit-times (104 μ s) before the transmission is present at the TXOP1 and TXOP2 pins, the TXRFEN pin will be set to "1" and the TXRFEN bit (STATUS register Bit 3) will also be set to "1". The interrupt flag TXRFF (Bit 3 of the IRQ FLAGS 2 register) will also be set to "1" and an interrupt (IRQN) will be generated if the mask has previously been enabled (TXRFM, Bit 3 of the IRQ MASK 2 register set to "1").
10. Completion of the last Reed-Solomon block transmission will cause the TXRFEN pin to be reset to "0" and the TXRFEN bit (STATUS register Bit 3) will also be reset to "0". The interrupt flag TXRFF (Bit 3 of the IRQ FLAGS 2 register) will be set to "1" and an interrupt (IRQN) will be generated if the mask has previously been enabled (TXRFM, Bit 3 of the IRQ MASK 2 register set to "1"). Finally, the outputs TXOP1 and TXOP2 will go to V_{BIAS} .
ENABTX (Bit 0 of the TX CONTROL register) should then be reset to "0", if required.
11. DECF (Bit 6 of the IRQ FLAGS register) and DEC (Bit 6 of the STATUS register) should be monitored to determine whether the M-ES Reverse Channel transmitted data has been decoded correctly by the MDBS.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	$V_{DD} + 0.3$	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA
E1 Package			
Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$		400	mW
Derating above 25°C		5.3	mW/ $^{\circ}\text{C}$ above 25°C
Storage Temperature	-55	+125	$^{\circ}\text{C}$
Operating Temperature	-40	+85	$^{\circ}\text{C}$

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)		2.7	5.5	V
Operating Temperature		-40	+85	$^{\circ}\text{C}$
Xtal Frequency		4.9149	4.9155	MHz

6.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

Xtal Frequency = 4.9152MHz, Bit Rate = 19.2k bits/sec, Noise Bandwidth = Bit Rate,
 $V_{DD} = 3.0V$ to $5.5V$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$ and $V_{DD} = 2.7V$ at $T_{AMB} = 25^{\circ}C$.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (zero-power) at $V_{DD} = 3.0V$	1	–	1.0	10.0	μA
I_{DD} (zero-power) at $V_{DD} = 5.0V$	1	–	1.0	10.0	μA
I_{DD} (Rx only) at $V_{DD} = 3.0V$	1	–	2.0	TBD	mA
I_{DD} (Rx only) at $V_{DD} = 5.0V$	1	–	4.0	TBD	mA
I_{DD} (Tx only) at $V_{DD} = 3.0V$	1	–	2.0	TBD	mA
I_{DD} (Tx only) at $V_{DD} = 5.0V$	1	–	4.0	TBD	mA
I_{DD} (Rx and Tx) at $V_{DD} = 3.0V$	1	–	3.5	TBD	mA
I_{DD} (Rx and Tx) at $V_{DD} = 5.0V$	1	–	7.0	TBD	mA
AC Parameters					
Tx Output					
Tx O/P impedance (powersaved)	2	300	500	–	k Ω
Tx O/P impedance (operating)	2	–	1.0	2.5	k Ω
Signal level	7	0.9	1.0	1.1	V_{P-P}
TXF latency	10	TBD	16	TBD	μs
Tx Processing Delay	9	–	1	–	Bit
TXOP1 or TXOP2 dc level (transmitting "1010...")		TBD	50%	TBD	V_{DD}
(in Tx mode, MOD1 and MOD2 gain OFF)		TBD	50%	TBD	V_{DD}
(in Powersave - Tx mode disabled)		TBD	50%	TBD	V_{DD}
(in zero-power mode)		–	0	–	V
Rx Input					
Rx I/P pin impedance (at 100Hz)		10	–	–	M Ω
Rx I/P amp open loop voltage gain (I/P = $1mV_{RMS}$ at 100Hz)		–	500	–	V/V
Input signal level	8	0.7	1.0	1.3	V_{P-P}
RXF latency	10	TBD	16	TBD	μs
Rx Processing Delay	9	–	7	–	Bits
Xtal/Clock Input					
'High' pulse width	3	40	–	–	ns
'Low' pulse width	3	40	–	–	ns
Input impedance (at 100Hz)		10	–	–	M Ω
Gain (I/P = $1mV_{RMS}$ at 1kHz)		20	–	–	dB
μC Interface					
Input logic "1" level	4, 5	80%	–	–	V_{DD}
Input logic "0" level	4, 5	–	–	20%	V_{DD}
Input leakage current ($V_{IN} = 0$ to V_{DD})	4, 5	–5.0	–	+5.0	μA
Input capacitance	4, 5	–	7.5	–	pF
Output logic "1" level ($I_{OH} = 120\mu A$)	5	90%	–	–	V_{DD}
Output logic "0" level ($I_{OL} = 360\mu A$)	5, 6	–	–	10%	V_{DD}
'Off' state leakage current ($V_{OUT} = V_{DD}$)	6	–	–	10	μA

Operating Characteristics Notes:

1. Not including any current drawn from the device pins by external circuitry
2. Small signal impedance
3. Timing for an external input to the CLOCK/XTAL pin
4. WRN, RDN, CSN, A0 – A2 pins
5. D0 - D7 pins
6. IRQN pin
7. Measured at TXOP1 and TXOP2 with MOD1/2 gain blocks set to 0dB
8. Measured at RXFB pin
9. Bit period = 52 μ s
10. From the availability of the last bit in a block. This implies that the first bit in the same block will be delayed by typically 22ms.

6.1.4 Timing Diagrams

For the following conditions unless otherwise specified:

Xtal Frequency = 4.9152MHz,

$V_{DD} = 3.0V$ to $5.5V$, $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$ and $V_{DD} = 2.7V$ at $T_{AMB} = 25^{\circ}C$.

		Notes	Min.	Typ.	Max.	Units
μC Parallel Interface Timings (ref. Figure 5)						
t_{ACSL}	Address valid to CSN low time		0	–	–	ns
t_{AH}	Address hold time		0	–	–	ns
t_{CSH}	CSN hold time		0	–	–	ns
t_{CSHI}	CSN high time	1	6	–	–	clock cycles
t_{CSRWL}	CSN to WRN or RDN low time		0	–	–	ns
t_{DHR}	Read data hold time		0	–	–	ns
t_{DHW}	Write data hold time		0	–	–	ns
t_{DSW}	Write data setup time		15	–	–	ns
t_{RHCSL}	RDN high to CSN low time (write)		0	–	–	ns
t_{RACL}	Read access time from CSN low	2	–	–	30	ns
t_{RARL}	Read access time from RDN low	2	–	–	25	ns
t_{RL}	RDN low time		35	–	–	ns
t_{RX}	RDN high to D0-D7 3-state time		–	–	10	ns
t_{WHCSL}	WRN high to CSN low time (read)		0	–	–	ns
t_{WL}	WRN low time		35	–	–	ns

Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin
2. With 30pF max to VSS on D0 - D7 pins

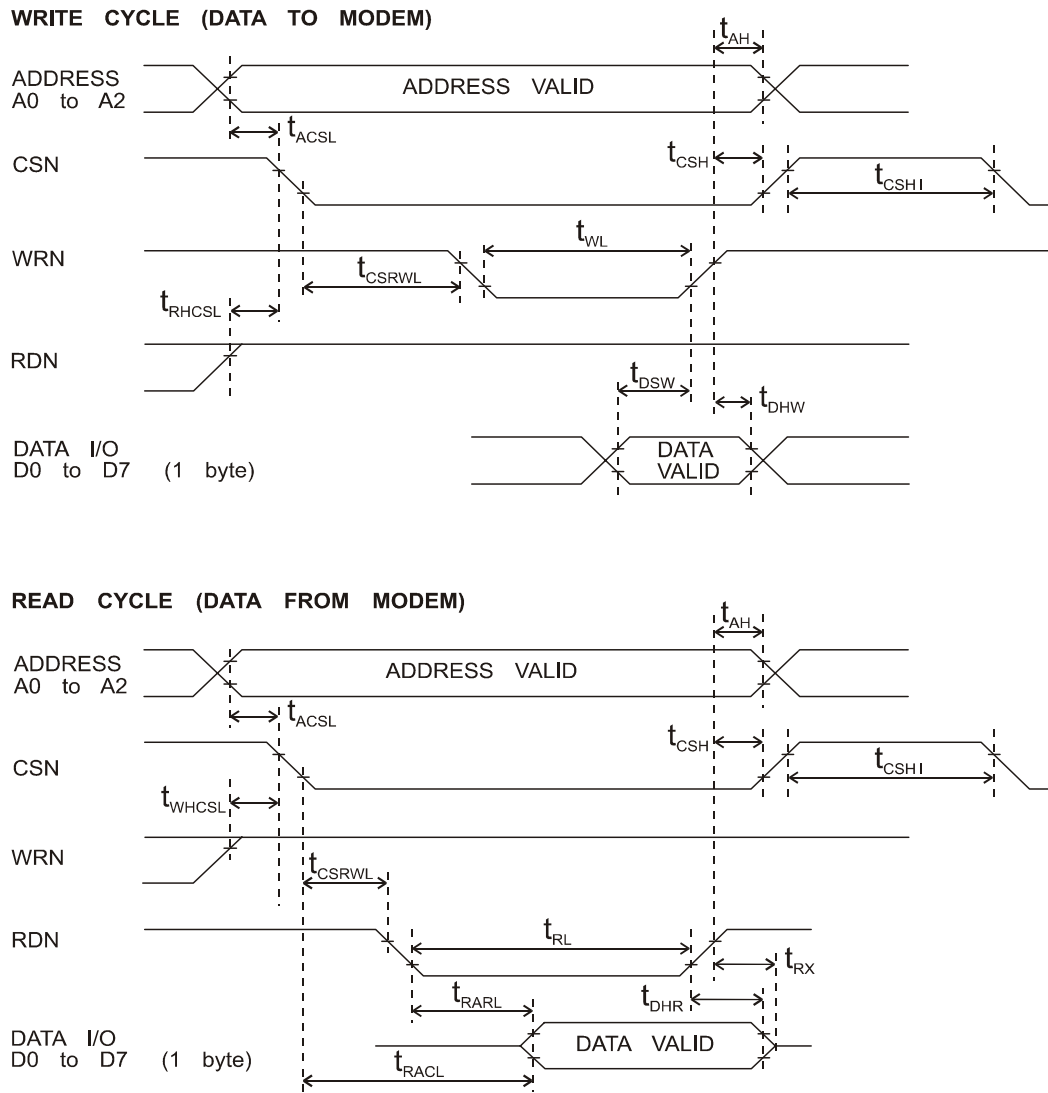
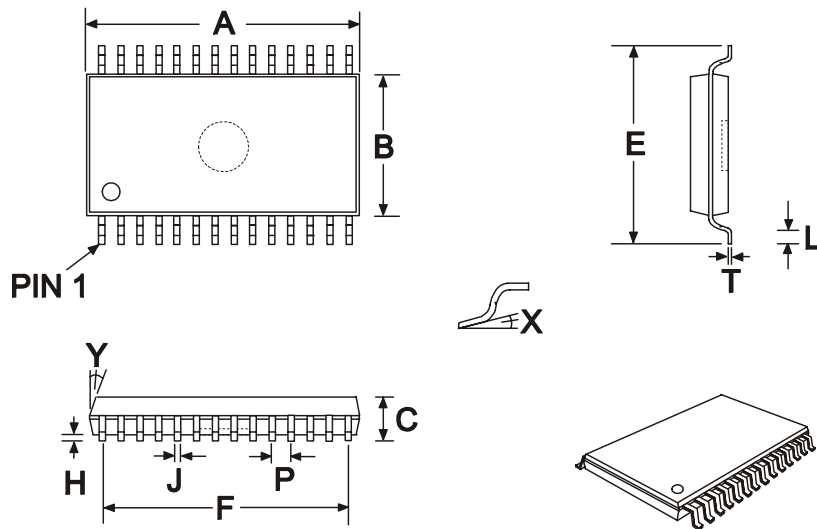


Figure 5: μ Controller Parallel Interface Timings

6.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A	0.378 (9.60)		0.386 (9.80)
* B	0.169 (4.30)		0.177 (4.50)
C	-----		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
F		0.333 (8.45)	
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.026 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
X	0°		7°
Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 28-pin TSSOP Mechanical Outline: Order as part no. CMX989E1