6/23/04

Errata: CS5376A Rev A Errata

(Reference CS5376A data sheet revision DS612F1 dated FEB'04)

Erratum #1: EEPROM configuration boot loader.

Description:

The digital filter does not initialize properly from the EEPROM 'Filter Start' command.

Work Around:

Replace the EEPROM 'Filter Start' command:

07

With the following patch code:

0B 00 30 00 00 30 03 97 80 C2 FF 22 80 D7 40 00 D2 06 0E 0D 00 30 00

Erratum #2: No IIR filter at 4000 SPS (0.25 ms sampling).

Description:

The IIR filter does not function properly for the 4000 SPS output word rate. At 4000 SPS most of the available digital filter calculation cycles are dedicated to the FIR filter.

Work Around:

Enable only SINC, FIR1, or FIR2 output when operating at the 4000 SPS output word rate.

CONTACTING CIRRUS LOGIC SUPPORT

For a complete listing of direct Distributor, Sales, and Sales Representative contacts, visit the Cirrus Logic website at http://www.cirrus.com/

Erratum #3: Minimum digital filter clock rate settings.

Description:

Some relatively slow output word rates (200 SPS, 40 SPS) require the maximum digital filter clock rate. The minimum required digital filter clock for each output word rate is listed below.

Output Word Rate (SPS)	Output Period (ms)	Digital Filter Clock Rate (MHz)
4000	0.25	16.384 - no IIR
2000	0.5	16.384
1000	1	8.192
500	2	4.096
333	3	8.192
250	4	4.096
200	5	16.384
125	8	2.048
100	10	8.192
50	20	2.048
40	25	16.384
25	40	2.048
20	50	8.192
10	100	2.048
5	200	2.048
1	1000	2.048

Work Around:

Always use the maximum 16.384 MHz digital filter clock, or independently select the minimum digital filter clock for each output word rate.

Erratum #4: Filter stop/start required when writing a new digital filter configuration.

Description:

Unexpected results can occur when reconfiguring the digital filter during operation.

Work Around:

Send the ‘Filter Stop’ command before writing updated configuration information, followed by the ‘Filter Start’ command to restart the digital filter using the updated configuration.

Erratum #5: All zero initial data write to the serial data FIFO.

Description:

Initializing the digital filter with the 'Filter Start' command causes a false write into the output data FIFO. The first serial data available from the SD port is an all zero word followed by the first digital filter result. At the first serial data read, the FIFO contains more data than expected.

Work Around:

The first serial data transaction should send 8 x 32 = 256 clocks into SDCLK to purge all data in the output FIFO. Later serial data read transactions can expect the digital filter result only.

Erratum #6: MCLK output at 4.096 MHz.

Description:

MCLK has incorrect timing for the CS5371/72 modulator when set to 4.096 MHz.

Work Around:

None. The 4.096 MHz setting for MCLK is normally not used.

Erratum #7: Boundary scan JTAG port.

Description:

A break in the scan chain prevents boundary scan JTAG from functioning properly.

Work Around:

None. Boundary scan JTAG is not available.