

# DRAM

## MT4LC16M4G3, MT4LC16M4H9

For the latest data sheet, please refer to the Micron Web site: [www.micronsemi.com/mti/msp/html/datasheet.html](http://www.micronsemi.com/mti/msp/html/datasheet.html)

### FEATURES

- Single +3.3V ±0.3V power supply
- Industry-standard x4 pinout, timing, functions, and packages
- 12 row, 12 column addresses (H9) or 13 row, 11 column addresses (G3)
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTTL-compatible
- Extended Data-Out (EDO) PAGE MODE access
- Optional self refresh (S) for low-power data retention
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms

### OPTIONS

- Refresh Addressing  
4,096 (4K) rows  
8,192 (8K) rows
- Plastic Packages  
32-pin SOJ (400 mil)  
32-pin TSOP (400 mil)
- Timing  
50ns access  
60ns access
- Refresh Rates  
Standard Refresh  
Self Refresh (128ms period)

### MARKING

H9  
G3

DJ  
TG

None  
S\*

- NOTE:** 1. The 16 Meg x 4 EDO DRAM base number differentiates the offerings in one place—MT4LC16M4H9. The fifth field distinguishes the address offerings: H9 designates 4K addresses and G3 designates 8K addresses.
2. The “#” symbol indicates signal is active LOW.

\*Contact factory for availability

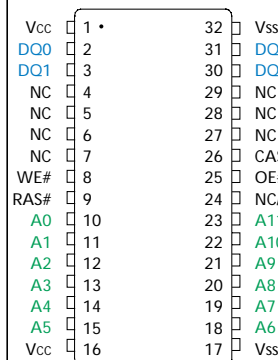
Part Number Example:  
**MT4LC16M4H9DJ-6**

### KEY TIMING PARAMETERS

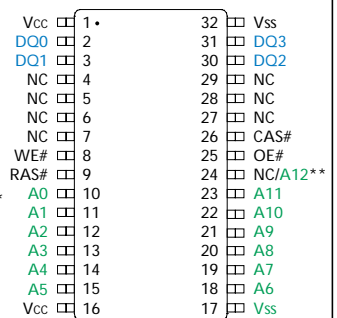
SPEED	t <sub>RC</sub>	t <sub>RAC</sub>	t <sub>PC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>CAS</sub>
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

### PIN ASSIGNMENT (Top View)

#### 32-Pin SOJ



#### 32-Pin TSOP



\*\*NC on H9 version, A12 on G3 version

### 16 MEG x 4 EDO DRAM PART NUMBERS

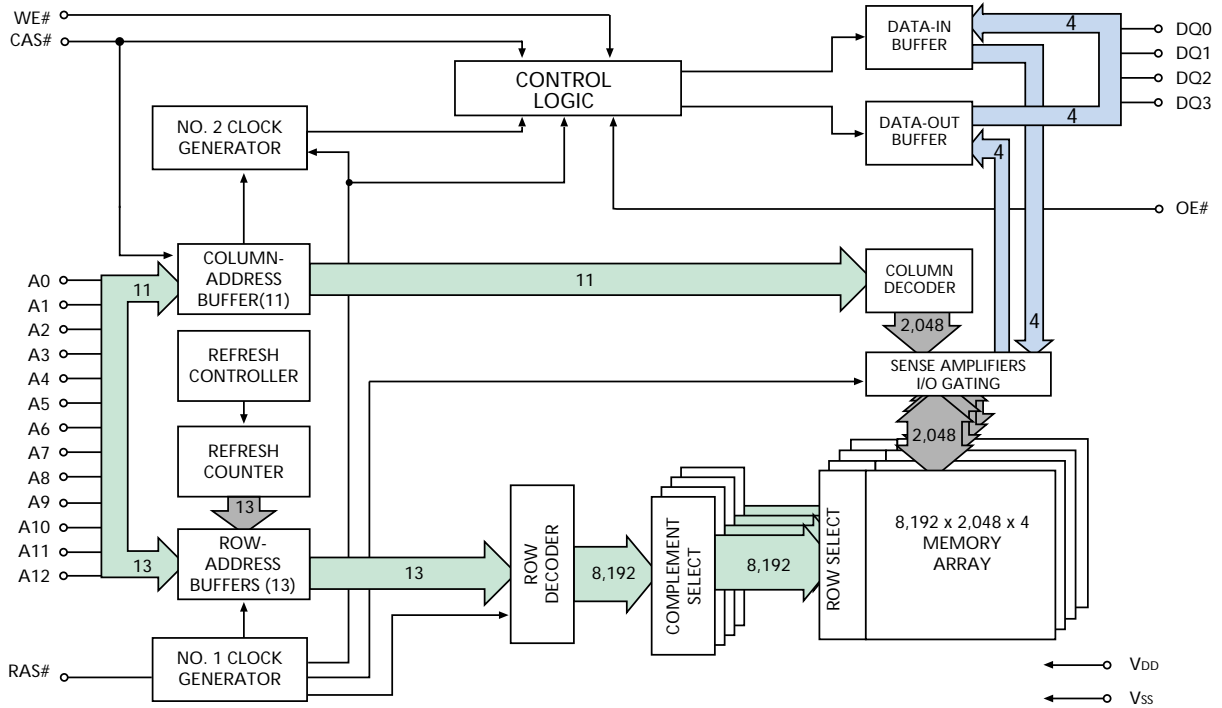
PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC16M4H9DJ-x	4K	SOJ	Standard
MT4LC16M4H9DJ-x S	4K	SOJ	Self
MT4LC16M4H9TG-x	4K	TSOP	Standard
MT4LC16M4H9TG-x S	4K	TSOP	Self
MT4LC16M4G3DJ-x	8K	SOJ	Standard
MT4LC16M4G3DJ-x S	8K	SOJ	Self
MT4LC16M4G3TG-x	8K	TSOP	Standard
MT4LC16M4G3TG-x S	8K	TSOP	Self

x = speed

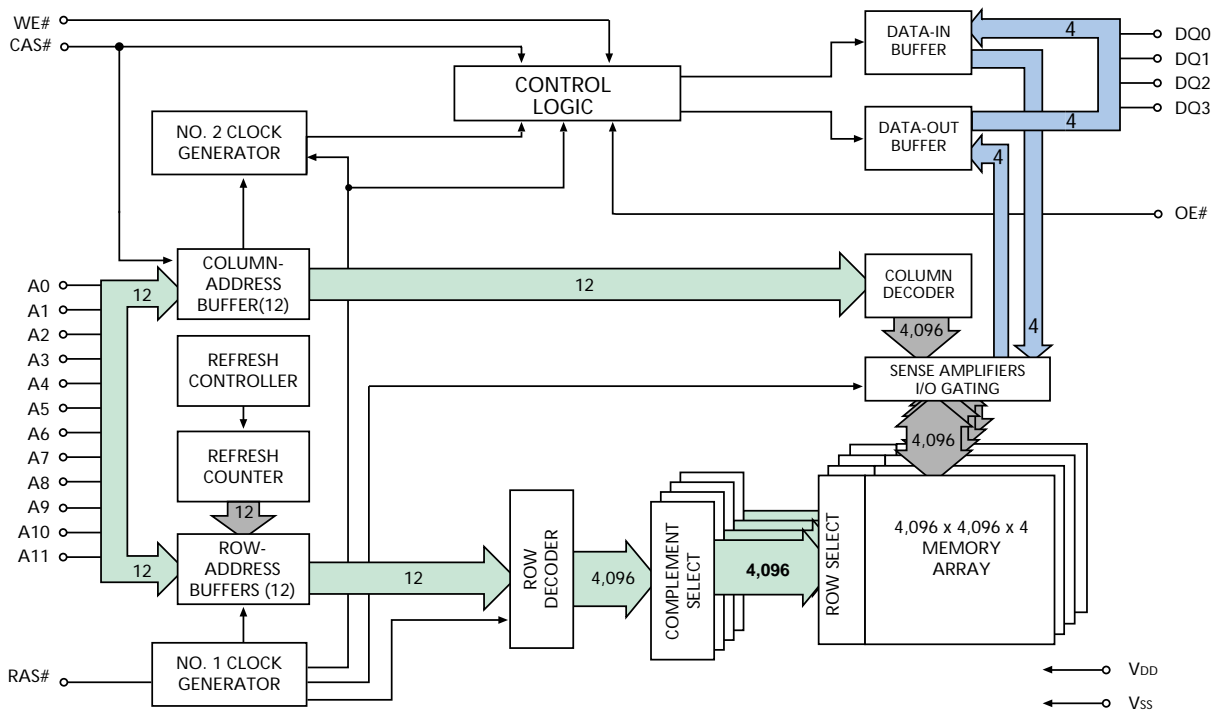
### GENERAL DESCRIPTION

The 16 Meg x 4 DRAM is a high-speed CMOS, dynamic random-access memory device containing 67,108,864 bits and designed to operate from 3V to 3.6V. The MT4LC16M4H9 and MT4LC16M4G3 are functionally organized as 16,777,216 locations containing 4 bits each. The 16,777,216 memory locations are arranged in 4,096 rows by 4,096 columns on the H9 version and 8,192 rows by 2,048 columns on the G3 version. During READ or WRITE cycles, each location is

**FUNCTIONAL BLOCK DIAGRAM  
MT4LC16M4G3 (13 row addresses)**



**FUNCTIONAL BLOCK DIAGRAM  
MT4LC16M4H9 (12 row addresses)**



## GENERAL DESCRIPTION (Continued)

uniquely addressed via the address bits. First, the row address is latched by the RAS# signal, then the column address is latched by CAS#. The device provides EDO-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE, or READ-MODIFY-WRITE) within a given row.

The 16 Meg x 4 DRAM must be refreshed periodically in order to retain stored data.

## DRAM ACCESS

Each location in the DRAM is uniquely addressable, as mentioned in the General Description. The data for each location is accessed via the four I/O pins (DQ0-DQ3). A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

## EDO PAGE MODE

DRAM READ cycles have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. If CAS# went HIGH and OE# was LOW (active), the output buffers would be disabled. The 16 Meg x 4 DRAM offers an accelerated page mode cycle by eliminating output disable from CAS# HIGH. This option is called EDO and it allows CAS# precharge time ( $t_{CP}$ ) to occur without the output data going invalid (see READ and EDO-PAGE-MODE READ waveforms).

EDO operates like any DRAM READ or FAST-PAGE-MODE READ, except data is held valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW and WE# is held HIGH. OE# can be brought LOW or HIGH while CAS# and RAS# are LOW, and the DQs will transition between valid data and High-Z. Using OE#, there are two methods to disable the outputs and keep them disabled during the CAS# HIGH time. The first method is to have OE# HIGH when CAS# transitions HIGH and keep OE# HIGH for  $t_{OEHC}$  thereafter. This will disable the DQs, and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again. The second method is to have OE# LOW when CAS#

transitions HIGH and then bring OE# HIGH for a minimum of  $t_{OEP}$  anytime during the CAS# HIGH period. This will disable the DQs, and they will remain disabled (regardless of the state of OE# after that point) until CAS# falls again. (Please refer to Figure 1.) During other cycles, the outputs are disabled at  $t_{OFF}$  time after RAS# and CAS# are HIGH or at  $t_{WHZ}$  after WE# transitions LOW. The  $t_{OFF}$  time is referenced from the rising edge of RAS# or CAS#, whichever occurs last. WE# can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

EDO-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the EDO-PAGE-MODE operation.

## DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (G3) or all 4,096 rows (H9) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC16M4G3 internally refreshes two rows for every CBR cycle, whereas the MT4LC16M4H9 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. The CBR refresh will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method, some compatibility issues may become apparent. For example, both G3 and H9 versions require 4,096 CBR REFRESH cycles, yet each requires a different number of RAS#-ONLY REFRESH cycles (G3 = 8,192 and H9 = 4,096). JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified  $t_{RASS}$ . The "S" option allows for an extended refresh period of 128ms, or 31.25 $\mu$ s per row for a 4K refresh and 15.625 $\mu$ s per row for an 8K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

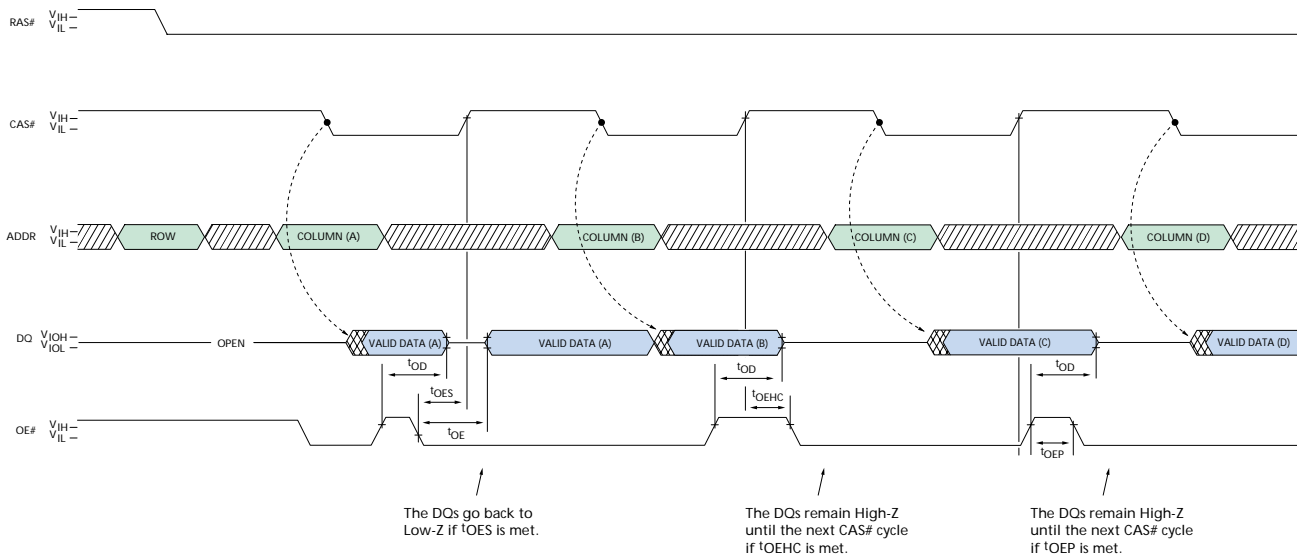
### DRAM REFRESH (Continued)

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of  $t_{RPS}$ . This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller uses RAS#-ONLY or burst CBR refresh, all rows

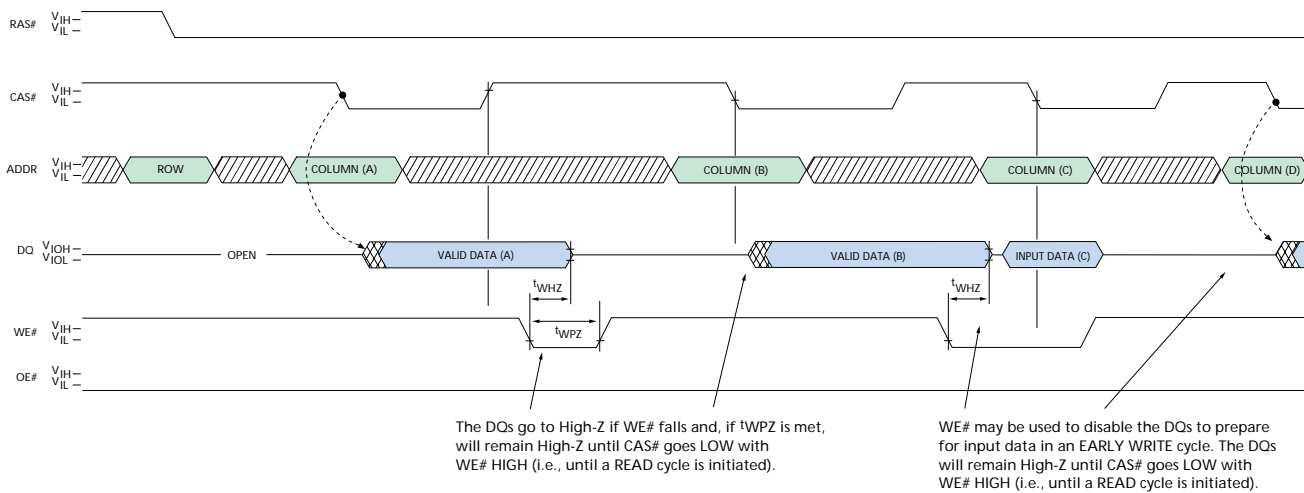
must be refreshed with a refresh rate of  $t_{RC}$  minimum prior to resuming normal operation.

### STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.



**Figure 1**  
**OE# Control of DQs**



**Figure 2**  
**WE# Control of DQs**

DON'T CARE  
 UNDEFINED

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on V<sub>CC</sub> Relative to V<sub>SS</sub> ..... -1V to +4.6V  
 Voltage on NC, Inputs or I/O Pins  
     Relative to V<sub>SS</sub> ..... -1V to +4.6V  
 Operating Temperature, T<sub>A</sub> (ambient) ... 0°C to +70°C  
 Storage Temperature (plastic) ..... -55°C to +150°C  
 Power Dissipation ..... 1W

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS**

(Note: 1) (V<sub>CC</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V <sub>CC</sub>	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V <sub>IH</sub>	2	V <sub>CC</sub> + 0.3	V	26
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V <sub>IL</sub>	-0.3	0.8	V	26
INPUT LEAKAGE CURRENT: Any input at V <sub>IN</sub> (0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> + 0.3V); All other pins not under test = 0V	I <sub>I</sub>	-2	2	μA	27
OUTPUT HIGH VOLTAGE: I <sub>OUT</sub> = -2mA	V <sub>OH</sub>	2.4	-	V	
OUTPUT LOW VOLTAGE: I <sub>OUT</sub> = 2mA	V <sub>OL</sub>	-	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V <sub>OUT</sub> (0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> + 0.3V); DQ is disabled and in High-Z state	I <sub>OZ</sub>	-5	5	μA	

**ICC OPERATING CONDITIONS AND MAXIMUM LIMITS**

 (Notes: 1, 2, 3, 5, 6) ( $V_{CC} = +3.3V \pm 0.3V$ )

PARAMETER/CONDITION	SYMBOL	SPEED	4K REFRESH	8K REFRESH	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = $V_{IH}$ )	I <sub>CC1</sub>	ALL	1	1	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# $\geq V_{CC} - 0.2V$ ; DQs may be left open; Other inputs: $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ )	I <sub>CC2</sub>	ALL	500	500	$\mu A$	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC}$ [MIN])	I <sub>CC3</sub>	-5 -6	170 160	130 120	mA	25
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = $V_{IL}$ , CAS#, address cycling: $t_{PC} = t_{PC}$ [MIN])	I <sub>CC4</sub>	-5 -6	150 120	150 120	mA	25
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = $V_{IH}$ : $t_{RC} = t_{RC}$ [MIN])	I <sub>CC5</sub>	-5 -6	170 160	130 120	mA	22
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC}$ [MIN])	I <sub>CC6</sub>	-5 -6	160 150	160 150	mA	4, 7
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = $t_{RAS}$ (MIN); WE# = $V_{CC} - 0.2V$ ; A0-A11, OE# and D <sub>IN</sub> = $V_{CC} - 0.2V$ or 0.2V (D <sub>IN</sub> may be left open)	I <sub>CC7</sub>	ALL	400	400	$\mu A$	4, 7
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# $\geq t_{RASS}$ (MIN) and CAS# held LOW; WE# = $V_{CC} - 0.2V$ ; A0-A11, OE# and D <sub>IN</sub> = $V_{CC} - 0.2V$ or 0.2V (D <sub>IN</sub> may be left open)	I <sub>CC8</sub>	ALL	400	400	$\mu A$	4, 7

## CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance: Address pins	C <sub>I1</sub>	5	pF
Input Capacitance: RAS#, CAS#, WE#, OE#	C <sub>I2</sub>	7	pF
Input/Output Capacitance: DQ	C <sub>IO</sub>	7	pF

## AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V<sub>CC</sub> = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Access time from column address	t <sub>AA</sub>		25		30	ns	
Column-address setup to CAS# precharge	t <sub>ACH</sub>	12		15		ns	
Column-address hold time (referenced to RAS#)	t <sub>AR</sub>	38		45		ns	
Column-address setup time	t <sub>ASC</sub>	0		0		ns	
Row-address setup time	t <sub>ASR</sub>	0		0		ns	
Column address to WE# delay time	t <sub>AWD</sub>	42		49		ns	18
Access time from CAS#	t <sub>CAC</sub>		13		15	ns	
Column-address hold time	t <sub>CAH</sub>	8		10		ns	
CAS# pulse width	t <sub>CAS</sub>	8	10,000	10	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	t <sub>CHD</sub>	15		15		ns	
CAS# hold time (CBR Refresh)	t <sub>CHR</sub>	8		10		ns	4
CAS# to output in Low-Z	t <sub>CLZ</sub>	0		0		ns	
Data output hold after CAS# LOW	t <sub>COH</sub>	3		3		ns	
CAS# precharge time	t <sub>CP</sub>	8		10		ns	13
Access time from CAS# precharge	t <sub>CPA</sub>		28		35	ns	
CAS# to RAS# precharge time	t <sub>CRP</sub>	5		5		ns	
CAS# hold time	t <sub>CSH</sub>	38		45		ns	
CAS# setup time (CBR Refresh)	t <sub>CSR</sub>	5		5		ns	4
CAS# to WE# delay time	t <sub>CWD</sub>	28		35		ns	18
WRITE command to CAS# lead time	t <sub>CWL</sub>	8		10		ns	
Data-in hold time	t <sub>DH</sub>	8		10		ns	19
Data-in setup time	t <sub>DS</sub>	0		0		ns	19
Output disable	t <sub>OD</sub>	0	12	0	15	ns	23, 24
Output enable time	t <sub>OE</sub>		12		15	ns	20
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t <sub>OEH</sub>	8		10		ns	24
OE# HIGH hold time from CAS# HIGH	t <sub>OEHC</sub>	5		10		ns	
OE# HIGH pulse width	t <sub>OEP</sub>	5		5		ns	
OE# LOW to CAS# HIGH setup time	t <sub>OES</sub>	4		5		ns	
Output buffer turn-off delay	t <sub>OFF</sub>	0	12	0	15	ns	17, 23

## AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ( $V_{CC} = +3.3V \pm 0.3V$ )

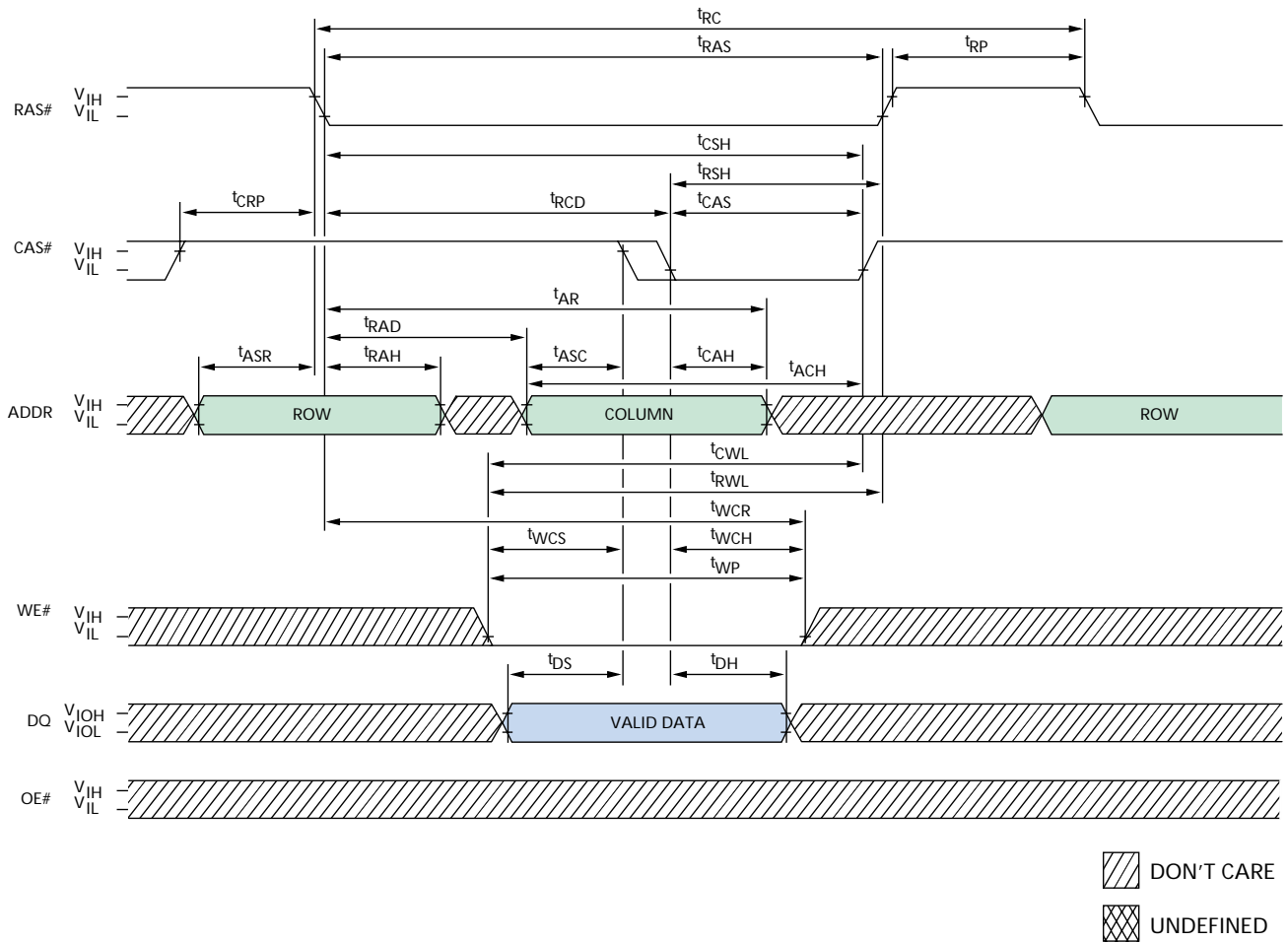
AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
OE# setup prior to RAS# during HIDDEN REFRESH cycle	$t_{ORD}$	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	$t_{PC}$	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	$t_{PRWC}$	47		56		ns	
Access time from RAS#	$t_{RAC}$		50		60	ns	23
RAS# to column-address delay time	$t_{RAD}$	9		12		ns	15
Row-address hold time	$t_{RAH}$	9		10		ns	
RAS# pulse width	$t_{RAS}$	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	$t_{RASP}$	50	125,000	60	125,000	ns	
RAS# pulse width during Self Refresh	$t_{RASS}$	100		100		$\mu s$	
Random READ or WRITE cycle time	$t_{RC}$	84		104		ns	
RAS# to CAS# delay time	$t_{RCD}$	11		14		ns	14
READ command hold time (referenced to CAS#)	$t_{RCH}$	0		0		ns	16
READ command setup time	$t_{RCS}$	0		0		ns	
Refresh period	$t_{REF}$		64		64	ms	22
Refresh period (4,096 cycles) "S" version	$t_{REF}$		128		128	ms	4
RAS# precharge time	$t_{RP}$	30		40		ns	
RAS# to CAS# precharge time	$t_{RPC}$	5		5		ns	
RAS# precharge time exiting Self Refresh	$t_{RPS}$	90		105		ns	
READ command hold time (referenced to RAS#)	$t_{RRH}$	0		0		ns	16
RAS# hold time	$t_{RSH}$	13		15		ns	
READ-WRITE cycle time	$t_{RWC}$	116		140		ns	
RAS# to WE# delay time	$t_{RWD}$	67		79		ns	18
WRITE command to RAS# lead time	$t_{RWL}$	13		15		ns	
Transition time (rise or fall)	$t_T$	2	50	2	50	ns	
WRITE command hold time	$t_{WCH}$	8		10		ns	
WRITE command hold time (referenced to RAS#)	$t_{WCR}$	38		45		ns	
WE# command setup time	$t_{WCS}$	0		0		ns	18
WE# to outputs in High-Z	$t_{WHZ}$	0	12	0	15	ns	
WRITE command pulse width	$t_{WP}$	5		5		ns	
WE# pulse width to disable outputs	$t_{WPZ}$	10		10		ns	
WE# hold time (CBR Refresh)	$t_{WRH}$	8		10		ns	4, 23
WE# setup time (CBR Refresh)	$t_{WRP}$	8		10		ns	4, 23



## NOTES

1. All voltages referenced to  $V_{SS}$ .
2. This parameter is sampled.  $V_{CC} = +3.3V$ ;  $f = 1$  MHz;  $T_A = 25^\circ C$ .
3.  $I_{CC}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100 $\mu s$  is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
7. AC characteristics assume  $t_T = 2.5ns$ .
8.  $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ).
9. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
10. If CAS# and RAS# =  $V_{IH}$ , data output is High-Z.
11. If CAS# =  $V_{IL}$ , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF; and  $V_{OL} = 0.8V$  and  $V_{OH} = 2V$ .
13. If CAS# is LOW at the falling edge of RAS#, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for  $t_{CP}$ .
14. The  $t_{RAD}$  (MAX) limit is no longer specified.  $t_{RAD}$  (MAX) was specified as a reference point only. If  $t_{RAD}$  was greater than the specified  $t_{RAD}$  (MAX) limit, then access time was controlled exclusively by  $t_{AA}$  ( $t_{RAC}$  and  $t_{CAC}$  no longer applied). With or without the  $t_{RAD}$  (MAX) limit,  $t_{AA}$ ,  $t_{RAC}$ , and  $t_{CAC}$  must always be met.
15. The  $t_{RCD}$  (MAX) limit is no longer specified.  $t_{RCD}$  (MAX) was specified as a reference point only. If  $t_{RCD}$  was greater than the specified  $t_{RCD}$  (MAX) limit, then access time was controlled exclusively by  $t_{CAC}$  ( $t_{RAC}$  [MIN] no longer applied). With or without the  $t_{RCD}$  limit,  $t_{AA}$  and  $t_{CAC}$  must always be met.
16. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
17.  $t_{OFF}$  (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
18.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$ , and  $t_{CWD}$  are not restrictive operating parameters.  $t_{WCS}$  applies to EARLY WRITE cycles. If  $t_{WCS} > t_{WCS}$  (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle.  $t_{RWD}$ ,  $t_{AWD}$ , and  $t_{CWD}$  define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ , and  $t_{AWD}$  are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.
22. RAS#-ONLY REFRESH requires that all rows be refreshed at least once every 64ms (4,096 rows for the H9 version and 8,192 rows for the G3 version). CBR REFRESH requires that at least 4,096 cycles be completed every 64ms.
23. The DQs open during READ cycles once  $t_{OD}$  or  $t_{OFF}$  occur. If CAS# stays LOW while OE# is brought HIGH, the DQs will open. If OE# is brought back LOW (CAS# still LOW), the DQs will provide the previously read data.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OD}$  and  $t_{OE}$  met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE# is taken back LOW while CAS# remains LOW, the DQs will remain open.
25. Column address changed once each cycle.
26.  $V_{IH}$  overshoot:  $V_{IH}$  (MAX) =  $V_{CC} + 2V$  for a pulse width  $\leq 10ns$ , and the pulse width cannot be greater than one third of the cycle rate.  $V_{IL}$  undershoot:  $V_{IL}$  (MIN) =  $-2V$  for a pulse width  $\leq 10ns$ , and the pulse width cannot be greater than one third of the cycle rate.
27. NC pins are assumed to be left floating and are not tested for leakage.

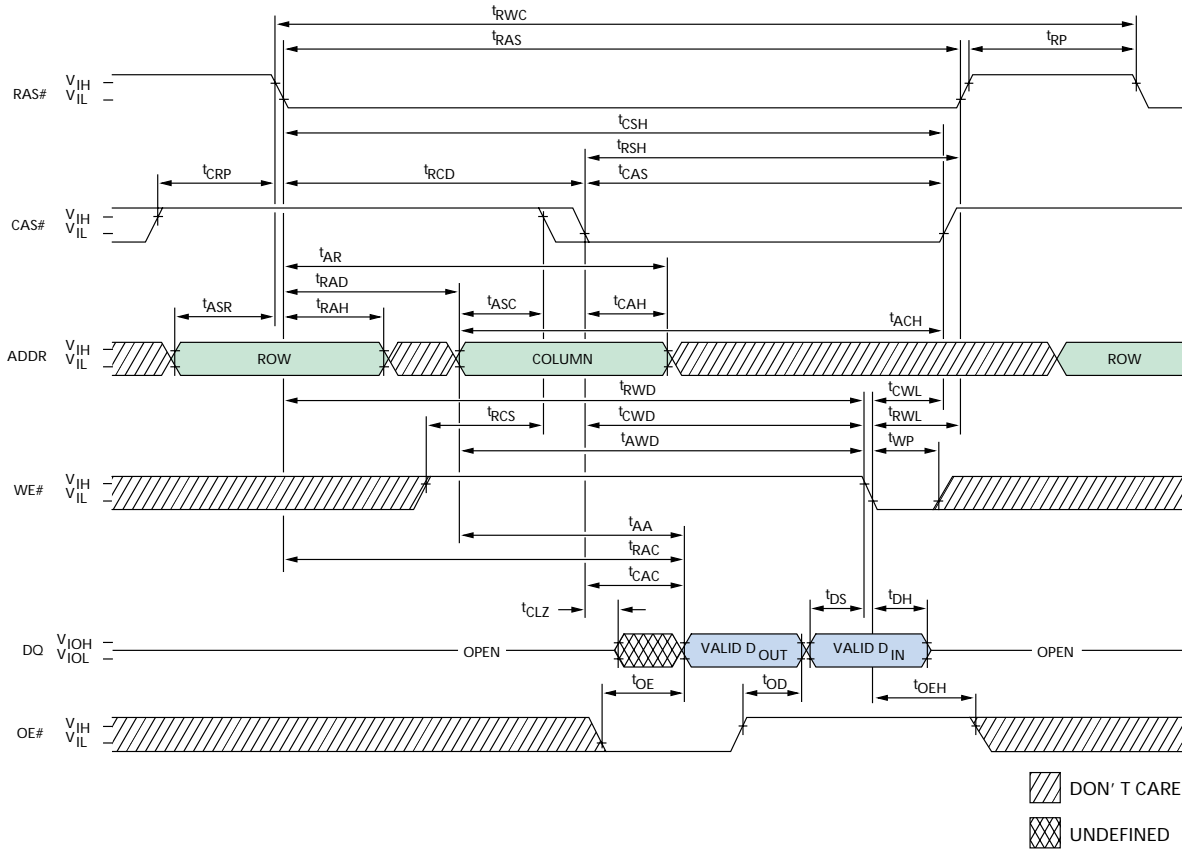


**EARLY WRITE CYCLE**

**TIMING PARAMETERS**

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
$t_{ACH}$	12		15		ns
$t_{AR}$	38		45		ns
$t_{ASC}$	0		0		ns
$t_{ASR}$	0		0		ns
$t_{CAH}$	8		10		ns
$t_{CAS}$	8	10,000	10	10,000	ns
$t_{CRP}$	5		5		ns
$t_{CSH}$	38		45		ns
$t_{CWL}$	8		15		ns
$t_{DH}$	8		10		ns
$t_{DS}$	0		0		ns
$t_{RAD}$	9		12		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
$t_{RAH}$	9		10		ns
$t_{RAS}$	50	10,000	60	10,000	ns
$t_{RC}$	84		104		ns
$t_{RCD}$	11		14		ns
$t_{RP}$	30		40		ns
$t_{RSH}$	13		15		ns
$t_{RWL}$	13		15		ns
$t_{WCH}$	8		10		ns
$t_{WCR}$	38		45		ns
$t_{WCS}$	0		0		ns
$t_{WP}$	5		5		ns

## READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)

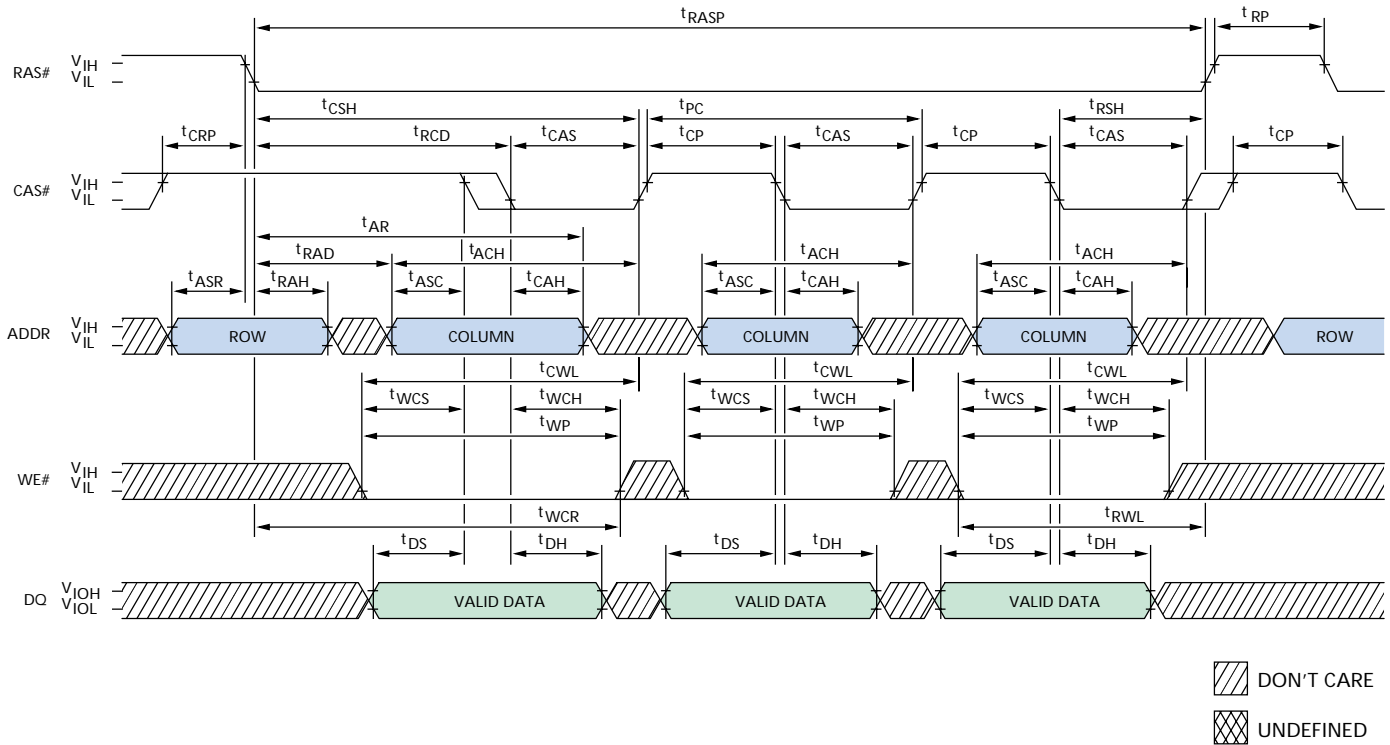


### TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC	116		140		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns



**EDO-PAGE-MODE EARLY WRITE CYCLE**


DON'T CARE  
 UNDEFINED

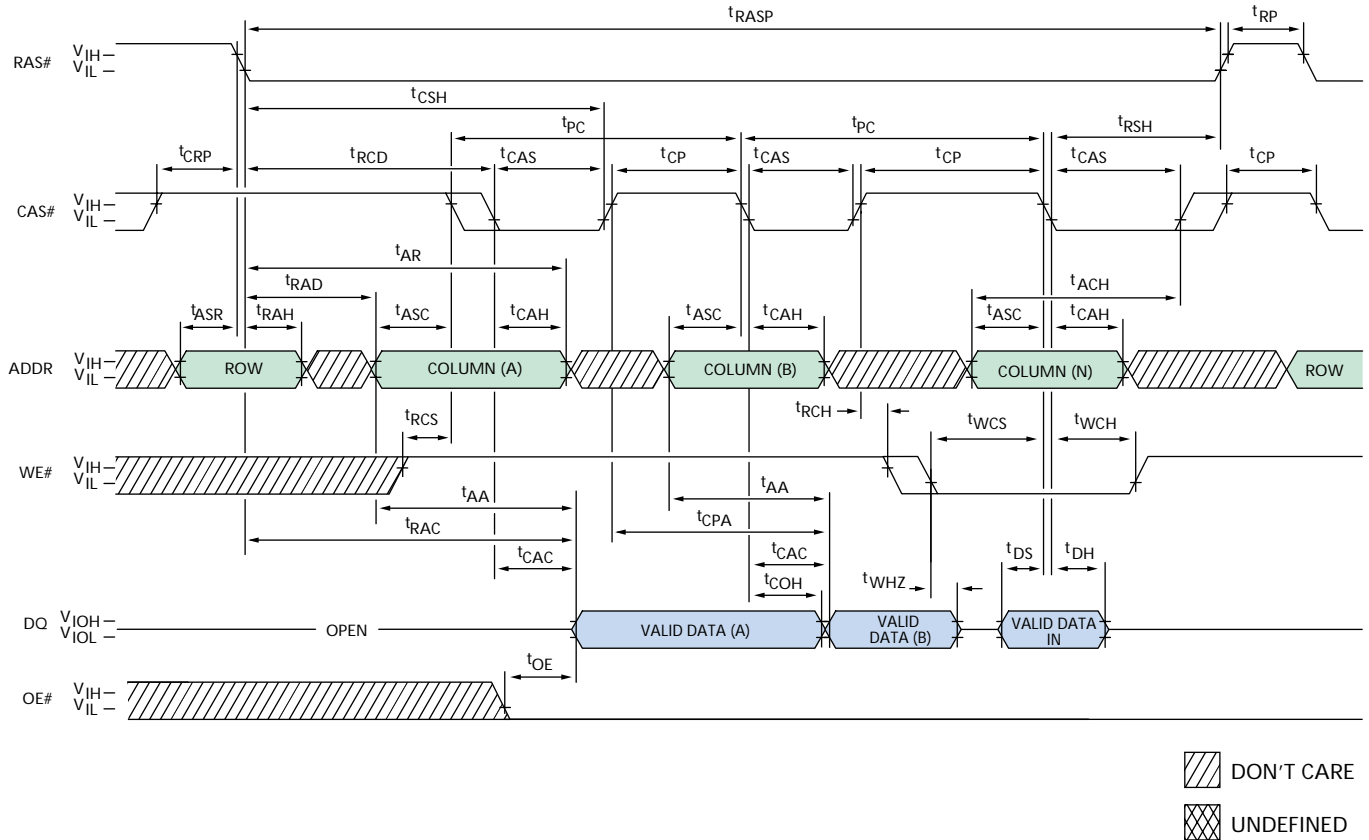
**TIMING PARAMETERS**

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t <sub>ACH</sub>	12		15		ns
t <sub>AR</sub>	38		45		ns
t <sub>ASC</sub>	0		0		ns
t <sub>ASR</sub>	0		0		ns
t <sub>CAH</sub>	8		10		ns
t <sub>CAS</sub>	8	10,000	10	10,000	ns
t <sub>CP</sub>	8		10		ns
t <sub>CRP</sub>	5		5		ns
t <sub>CSH</sub>	38		45		ns
t <sub>CWL</sub>	8		10		ns
t <sub>DH</sub>	8		10		ns
t <sub>DS</sub>	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t <sub>PC</sub>	20		25		ns
t <sub>RAD</sub>	9		12		ns
t <sub>RAH</sub>	9		10		ns
t <sub>RASP</sub>	50	125,000	60	125,000	ns
t <sub>RCD</sub>	11		14		ns
t <sub>RP</sub>	30		40		ns
t <sub>RSH</sub>	13		15		ns
t <sub>RWL</sub>	13		15		ns
t <sub>WCH</sub>	8		10		ns
t <sub>WCR</sub>	38		45		ns
t <sub>WCS</sub>	0		0		ns
t <sub>WP</sub>	5		5		ns



### EDO-PAGE-MODE READ EARLY WRITE CYCLE (Pseudo READ-MODIFY-WRITE)



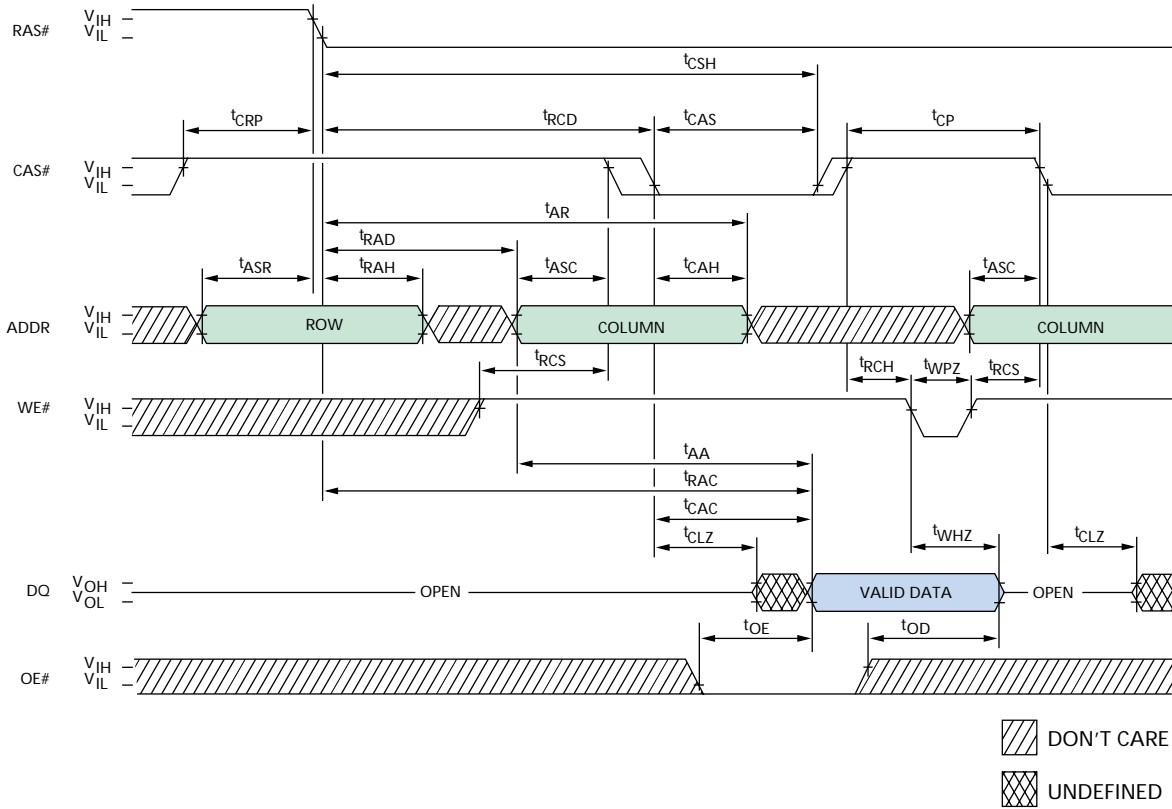
### TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns



### READ CYCLE (With WE#-controlled disable)

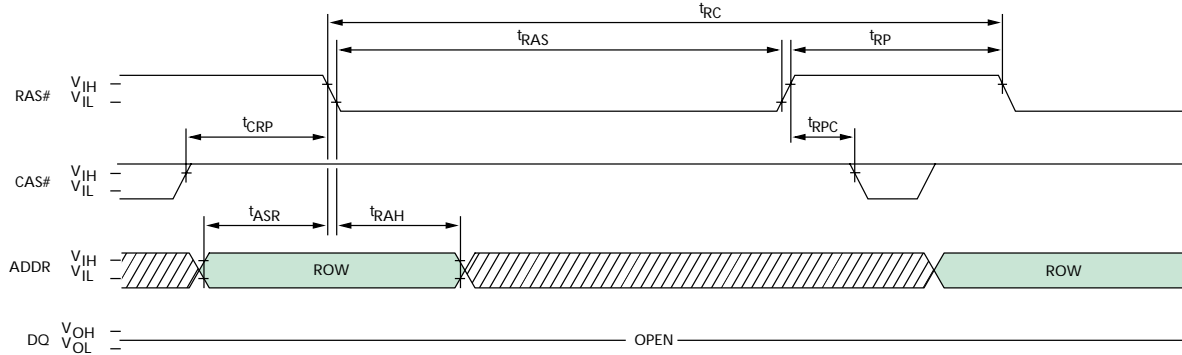


#### TIMING PARAMETERS

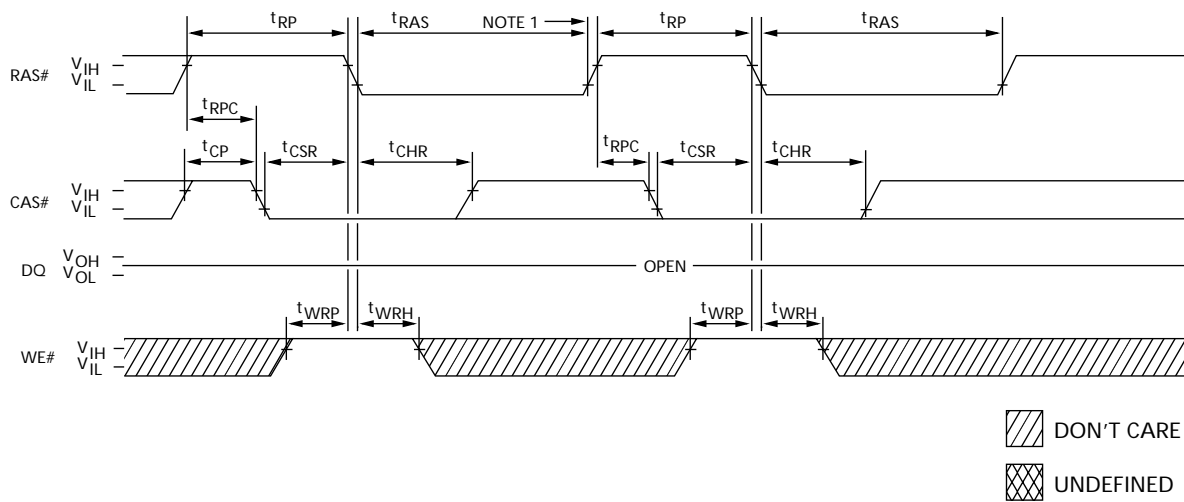
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
$t_{AA}$		25		30	ns
$t_{AR}$	38		45		ns
$t_{ASC}$	0		0		ns
$t_{ASR}$	0		0		ns
$t_{CAC}$		13		15	ns
$t_{CAH}$	8		10		ns
$t_{CAS}$	8	10,000	10	10,000	ns
$t_{CLZ}$	0		0		ns
$t_{CP}$	8		10		ns
$t_{CRP}$	5		5		ns
$t_{CSH}$	38		45		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
$t_{OD}$	0	12	0	15	ns
$t_{OE}$		12		15	ns
$t_{RAC}$		50		60	ns
$t_{RAD}$	9		12		ns
$t_{RAH}$	9		10		ns
$t_{RCD}$	11		14		ns
$t_{RCH}$	0		0		ns
$t_{RCS}$	0		0		ns
$t_{WHZ}$	0	12	0	15	ns
$t_{WPZ}$	10		10		ns

### RAS#-ONLY REFRESH CYCLE (OE# and WE# = DON'T CARE)



### CBR REFRESH CYCLE (Addresses and OE# = DON'T CARE)



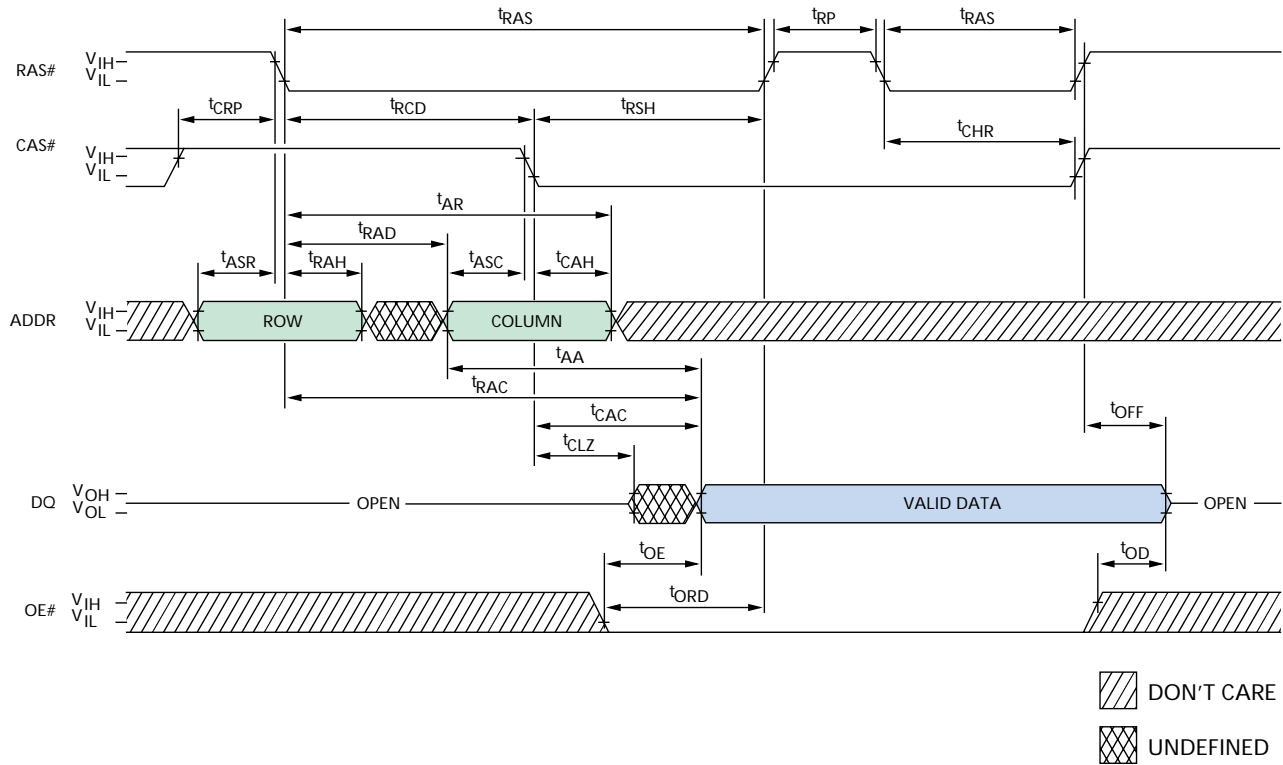
#### TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t <sub>ASR</sub>	0		0		ns
t <sub>CHR</sub>	8		10		ns
t <sub>CP</sub>	8		10		ns
t <sub>CRP</sub>	5		5		ns
t <sub>CSR</sub>	5		5		ns
t <sub>RAH</sub>	9		10		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t <sub>RAS</sub>	50	10,000	60	10,000	ns
t <sub>RC</sub>	84		104		ns
t <sub>RP</sub>	30		40		ns
t <sub>RPC</sub>	5		5		ns
t <sub>WRH</sub>	8		10		ns
t <sub>WRP</sub>	8		10		ns

**NOTE:** 1. End of first CBR REFRESH cycle.

### HIDDEN REFRESH CYCLE <sup>1</sup> (WE# = HIGH; OE# = LOW)



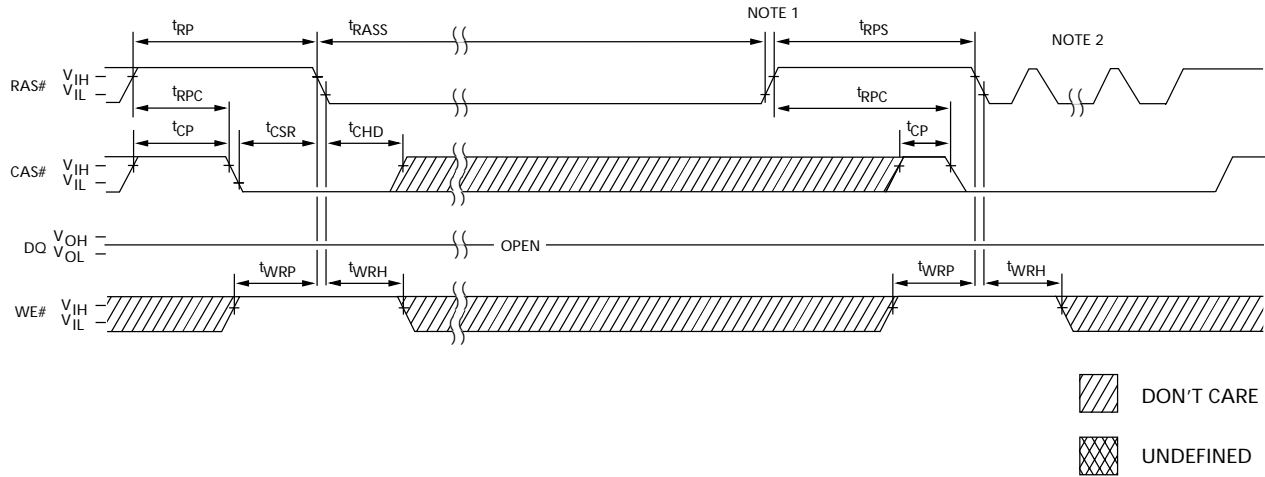
#### TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t <sub>AA</sub>		25		30	ns
t <sub>AR</sub>	38		45		ns
t <sub>ASC</sub>	0		0		ns
t <sub>ASR</sub>	0		0		ns
t <sub>CAC</sub>		13		15	ns
t <sub>CAH</sub>	8		10		ns
t <sub>CHR</sub>	8		10		ns
t <sub>CLZ</sub>	0		0		ns
t <sub>CRP</sub>	5		5		ns
t <sub>OD</sub>	0	12	0	15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t <sub>OE</sub>		12		15	ns
t <sub>OFF</sub>	0	12	0	15	ns
t <sub>ORD</sub>	0		0		ns
t <sub>RAC</sub>		50		60	ns
t <sub>RAD</sub>	9		12		ns
t <sub>RAH</sub>	9		10		ns
t <sub>RAS</sub>	50	10,000	60	10,000	ns
t <sub>RCD</sub>	11		14		ns
t <sub>RP</sub>	30		40		ns
t <sub>RSH</sub>	13		15		ns

**NOTE:** 1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.

### SELF REFRESH CYCLE (Addresses and OE# = DON'T CARE)



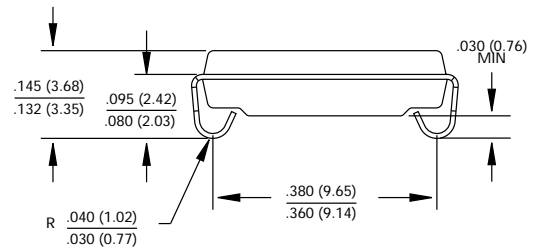
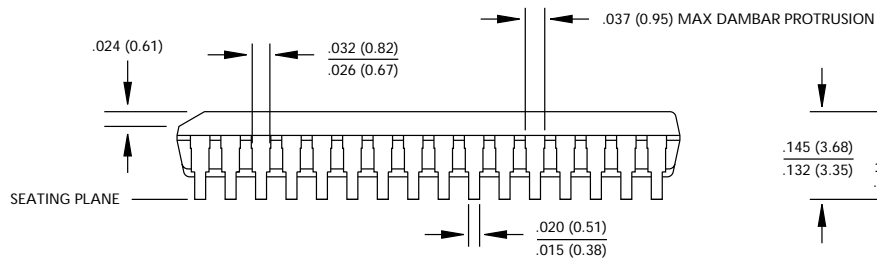
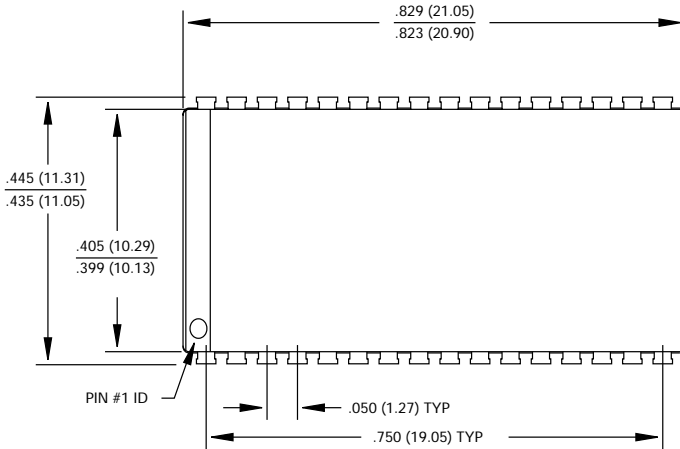
#### TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
$t_{CHD}$	15		15		ns
$t_{CP}$	8		10		ns
$t_{CSR}$	5		5		ns
$t_{RASS}$	100		100		$\mu$ s
$t_{RP}$	30		40		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
$t_{RPC}$	5		5		ns
$t_{RPS}$	90		105		ns
$t_{WRH}$	8		10		ns
$t_{WRP}$	8		10		ns

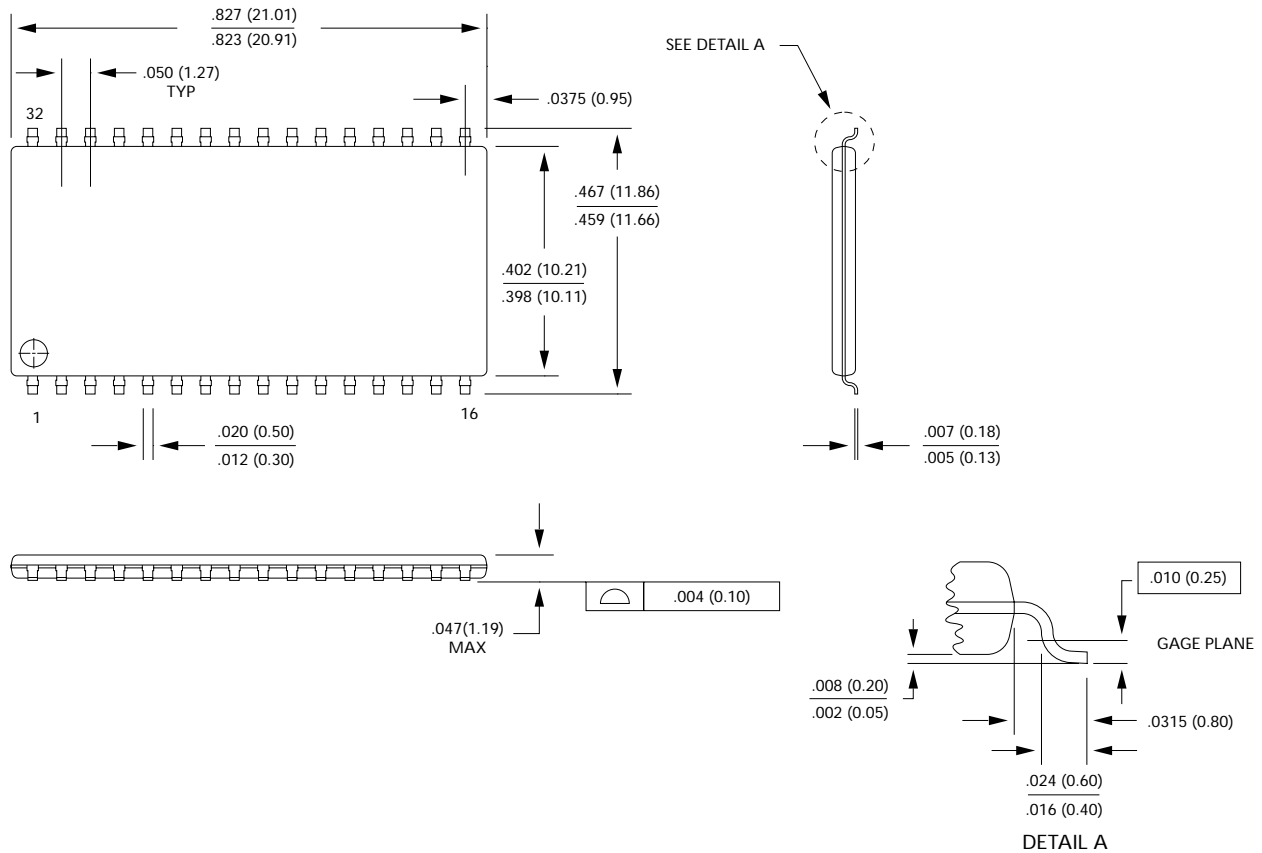
- NOTE:** 1. Once  $t_{RASS}$  (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.  
 2. Once  $t_{RPS}$  is satisfied, a complete burst of all rows should be executed if RAS#-only por Burst CBR refresh is being used.

32-PIN PLASTIC SOJ (400 mil)



**NOTE:** 1. All dimensions in inches (millimeters) MAX or typical where noted.  
MIN

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

**32-PIN PLASTIC TSOP (400 mil)**


- NOTE:** 1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.  
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.



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