



4-Input Quad OR/NOR Gate

Product Preview

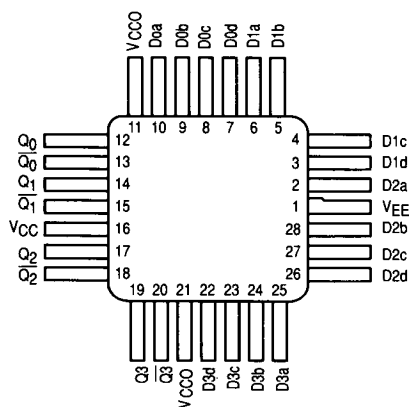
ELECTRICALLY TESTED PER:
100E501

The 100E501 is a quad 4-Input **OR/NOR** gate.

- 500 ps Max. Propagation Delay
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 k Ω Input Pulldown Resistors

PIN NAME

Pin	Function
$D_{0a} - D_{3d}$	Data Inputs
$Q_0 - Q_3$	True Outputs
$\overline{Q_0} - \overline{Q_3}$	Inverting Outputs



Military 100E501

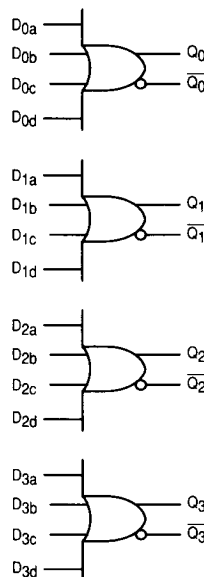


AVAILABLE AS

- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: Planned
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

LOGIC DIAGRAM



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA MILITARY MECL DATA
5-41

100E501

100E Series DC CHARACTERISTICS: $V_{EE} = -4.2 \text{ V to } -5.46 \text{ V}$, $V_{CC} = V_{CCO} = \text{GND}$; $-55^{\circ}\text{C to } +125^{\circ}\text{C}$

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH}(\text{max})$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL}(\text{min})$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH}(\text{min})$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL}(\text{max})$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		μA	$V_{IN} = V_{IL}(\text{min})$	

DC CHARACTERISTICS: $V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$, $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	$+25^{\circ}\text{C}$		$+125^{\circ}\text{C}$		-55°C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input Current High		150		150		150	μA	
I_{EE}	Power Supply Current		36		42		36	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$, $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	$+25^{\circ}\text{C}$		$+125^{\circ}\text{C}$		-55°C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q								
		200	500	200	500	200	500	ps	
t_{Skew}	Within-device Skew	50		50		50		ps	(Note 1)
t_{Skew}	Within-gate Skew	25		25		25		ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	300	575	300	575	300	575	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the variation in propagation delays of a gate when driven from its different inputs.