REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24									
REV STATUS OF SHEETS				REV															
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-02-23

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, INTERFACE, TRANSPARENT ASYNCHRONOUS RECEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90528
A	67268	

SHEET 1 OF 24

DESC FORM 193
JUL 91

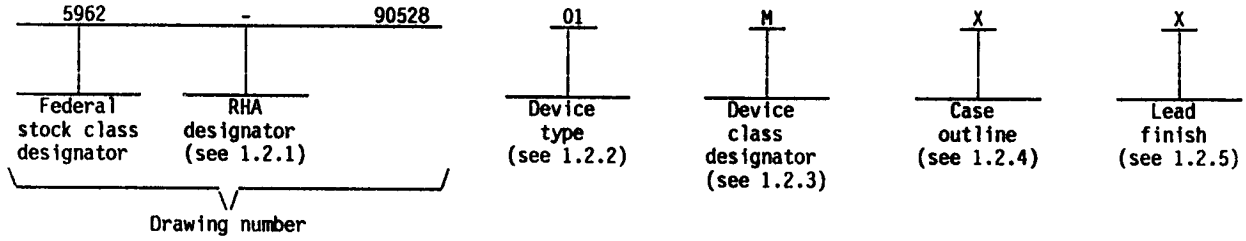
5962-E046-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7969-125V	1/ Transparent asynchronous receiver interface

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
3	CQCC2-N28	28	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ The cascade mode of this device does not work.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{CC}) to ground potential continuous.	-0.5 V to +7.0 V
DC voltage range applied to outputs	-0.5 V to V_{CC} maximum
DC input voltage range.	-0.5 V to +5.5 V
DC output current	±100 mA
DC input current.	-30 to +5.0 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation P_D 3/	2.6 W
Lead temperature (soldering, 10 seconds). .	+300°C
Thermal resistance junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	155°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}).	+4.75 V dc to +5.5 V dc
Minimum high-level input voltage (V_{IH}). . .	2.0 V
Maximum low-level input voltage (V_{IL}) . . .	0.8 V
Case operating temperature range (T_C) . . .	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) . . . . . XX percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Must withstand the added P_D due to short circuit test; e.g., I_{SC}.
4/ Values will be added when they become available.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Functional block diagram(s). The functional block diagram(s) shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 104 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Limits		Unit
				Min	Max	
Bus interface signals: DO_0-DO_7, DO_8/CO_3, DO_9/CO_2, CO_0-CO_1, DSTRB, CSTRB, IGM, CLK, CNB, VLTN						
Output high voltage	V_{OH}	V_{CC} = 4.75 V, I_{OH} = -1 mA V_{IN} = 0.0 V or 3.0 V	1, 2, 3	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.75 V, I_{OL} = 8 mA V_{IN} = 0.0 V or 3.0 V			0.45	
Input high voltage	V_{IH}	V_{CC} = 5.5 V 2/		2.0		
Input low voltage	V_{IL}	V_{CC} = 5.5 V 2/			0.8	
Input clamp voltage	V_I	V_{CC} = 4.75 V, I_{IN} = -18 mA			-1.5	
Input low current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V			-400	µA
Input high current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	
Input leakage current	I_I	V_{CC} = 5.5 V, V_{IN} = 5.5 V			50	
Output short circuit current	I_{SC}	3/		-15	-85	mA
Serial interface signals: SERIN+, SERIN-						
Input high voltage SERIN+	V_{IHS}	2/ 4/	7, 8	V_{CC} -1.165	V_{CC} -0.88	V
Input low voltage SERIN+	V_{ILS}	2/ 4/		V_{CC} -1.81	V_{CC} -1.475	
Test mode threshold SERIN-	V_{THT}	V_{CC} = 5.5 V			0.25	
Differential input voltage SERIN+	V_{DIF}		1, 2, 3	0.3	1.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/		Group A subgroups	Limits		Unit
					Min	Max	
Serial interface signals: SERIN+, SERIN - Continued							
Input common mode voltage	V_{ICM}	5/		1, 2, 3	3.05	V_{CC} -0.55	V
Input low current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = V_{CC}-1.81 V			0.5		µA
Input high current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = V_{CC}-0.88 V				220	
Miscellaneous signals: X_1, V_{CC1}, V_{CC2}							
Input high threshold X_1	V_{IHX}			1, 2, 3	2.0		V
Input low voltage X_1	V_{ILX}					0.8	
Input low current X_1	I_{ILX}	V_{IN} = 0.45 V				-900	µA
Input high current X_1	I_{IHX}	V_{IN} = 2.4 V				+600	
Supply current	I_{CC}	DMS = 0 V_{CC1} = V_{CC2} = 5.5 V	pin V_{CC1} (TTL)			55	mA
			pin V_{CC2} (CML)			335	
Bus interface signals: DO_0-DO_7, DO_8/CO_3, DO_9/CO_2, CO_0-CO_1, DSTRB, CSTRB, IGM, CLK, CNB, VLTN 6/							
CLK period 7/	t_{35}	See figure 4 8/		9, 10, 11	8n	25n	ns
Data valid to STRB ↑ delay	t_{36}	See figure 4, TTL output load 8/			$\frac{2t_{35}}{n}$		
CLK ↓ to STRB ↑	t_{37}					$(2t_{35}/n)$ + 15	
CLK ↑ to STRB ↓	t_{38}				$\frac{t_{35}}{n}$ -7		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.75\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Limits		Unit
				Min	Max	
STRB ↑ to CLK ↑ 9/	t_{38a}	See figure 4, 8/ TTL output load	9, 10, 11	$\frac{3t_{35}}{n}$ -14		ns
CLK ↓ to data valid delay	t_{39}				$-(t_{35}/n)$ + 23	
STRB pulse width high	t_{40}			$\frac{5t_{35}}{2n}$	$\frac{5t_{35}}{n}$	
CLK pulse width high	t_{41}			$\frac{5t_{35}}{n}$ -15		
CLK pulse width low	t_{42}			$\frac{5t_{35}}{2n}$ -15		
SERIN to CLK ↓ delay	t_{43}			$\frac{t_{35}}{2n}$ +17	$\frac{2t_{35}}{n}$ +26	
Serial interface signals: SERIN+, SERIN-						
SERIN± peak to peak input jitter tolerance	t_{57}	10/ 11/ See figure 4	9, 10, 11		5	ns
Miscellaneous: X_1 12/						
X_1 pulse width high	t_{60}	1/ 4/ See figure 4	9, 10, 11	35		ns
X_1 pulse width low	t_{61}			35		

1/ Unless otherwise specified, for dc test parameters, all test conditions shall be worst case conditions; V_{IH} = 2.0 V and V_{IL} = 0.8 V. For ac test parameters, all tests are performed using the input waveforms shown in figure 4.

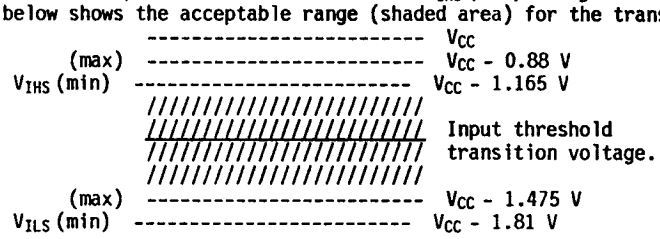
The following conditions also apply:

All timing references are made with respect to +1.5 V for TTL-level signals or to the 50 percent point between V_{OH} and V_{OL} for ECL signals. ECL input rise and fall times must be 2 ns ±0.2 ns between 20 percent and 80 percent points. TTL input rise and fall times must be 2 ns ±0.2 ns between 1 V and 2 V.

2/ Measured with device in test mode while monitoring output logic states.

3/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4/ Device thresholds on the SERIN (+/-) pin(s) are verified during production test by ensuring that the input threshold is less than V_{IHS} (min) and greater than V_{ILS} (max). The figure below shows the acceptable range (shaded area) for the transition voltage.



5/ Voltage applied to either SERIN± pins must not be above V_{CC} nor below +2.5 V to assure proper operation.

6/ "STRB" is either CSTRB or DSTRB and "Data" is either DO_0-DO_7, DO_8/CO_3, DO_9/CO_2, CO_0-CO_1.

7/ This parameter does not apply during reacquisition when CLK stretch can occur.

8/ Switching characteristics are tested during 8-bit local mode operation. "n" is determined by the following table:

DMS	SERIN-	"n"
GND	< V_{THTMAX} or open	n = 1; 8 Bit test mode
	> 2.5 V	n = 10; 8 Bit local mode
VCC	< V_{THTMAX} or open	n = 1; 9 Bit test mode
	> 2.5 V	n = 11; 9 Bit local mode
Open or 1/2 V_{CC}	< V_{THTMAX} or open	n = 1; 10 Bit test mode
	> 2.5 V	n = 12; 10 Bit local mode

9/ The limit for this parameter cannot be derived from t_{37} and t_{42}.

10/ This parameter is the sum of the data dependent jitter, duty cycle distortion, and random jitter.

11/ Parameter guaranteed. Not included in production and group A testing. Supporting data on file to validate limit.

12/ Jitter on X_1 input must be less than ±0.2 ns to ensure that automatic test equipment is able to properly measure device switching characteristics. The X1 input frequency will determine the byte rate reference for the receiver byte clock.

Cases X and 3

Pin or terminal number	Symbol	Pin or terminal number	Symbol
1	DO_3	15	CO_0
2	DO_2	16	CO_1
3	DO_1	17	DO_9/CO_2
4	DO_0	18	DO_8/CO_3
5	IGM	19	CLK
6	$\overline{\text{RESET}}$	20	GND_1 (TTL)
7	VCC1 (TTL)	21	GND_2 (CML)
8	V_{CC2} (CML)	22	X_1
9	SERIN+	23	X_2
10	SERIN-	24	CNB
11	DMS	25	DO_7
12	DSTRB	26	DO_6
13	CSTRB	27	DO_5
14	VLTN	28	DO_4

FIGURE 1. Terminal connections.

Encoder patterns					
4B/5B encoder scheme			5B/6B encoder scheme		
Hex data	4-bit binary data	5-bit encoded symbol	Hex data	5-bit binary data	6-bit encoded symbol
0	0000	11110	00	00000	110110
1	0001	01001	01	00001	010001
2	0010	10100	02	00010	100100
3	0011	10101	03	00011	100101
4	0100	01010	04	00100	010010
5	0101	01011	05	00101	010011
6	0110	01110	06	00110	010110
7	0111	01111	07	00111	010111
8	1000	10010	08	01000	100010
9	1001	10011	09	01001	110001
A	1010	10110	0A	01010	110111
B	1011	10111	0B	01011	100111
C	1100	11010	0C	01100	110010
D	1101	11011	0D	01101	110011
E	1110	11100	0E	01110	110100
F	1111	11101	0F	01111	110101
			10	10000	111110
			11	10001	011001
			12	10010	101001
			13	10011	101101
			14	10100	011010
			15	10101	011011
			16	10110	011110
			17	10111	011111
			18	11000	101010
			19	11001	101011
			1A	11010	101110
			1B	11011	101111
			1C	11100	111010
			1D	11101	111011
			1E	11110	111100
			1F	11111	111101

Note: Hex data is parallel input data which is represented by the 4-bit or 5-bit binary data listed in the column to the immediate right of Hex data. Binary bits are listed from left to right in the following order:

8-bit mode = D_7, D_6, D_5, D_4, (4-bit binary), and D_3, D_2, D_1, D_0, (4-bit binary)
9-bit mode = D_8, D_7, D_6, D_5, D_4, (5-bit binary), and D_3, D_2, D_1, D_0, (4-bit binary)
10-bit mode = D_8, D_7, D_6, D_5, D_4, (5-bit binary), and D_9, D_3, D_2, D_1, D_0, (5-bit binary)

Serial bits are shifted out with the most significant bit of the most significant nibble coming out first.

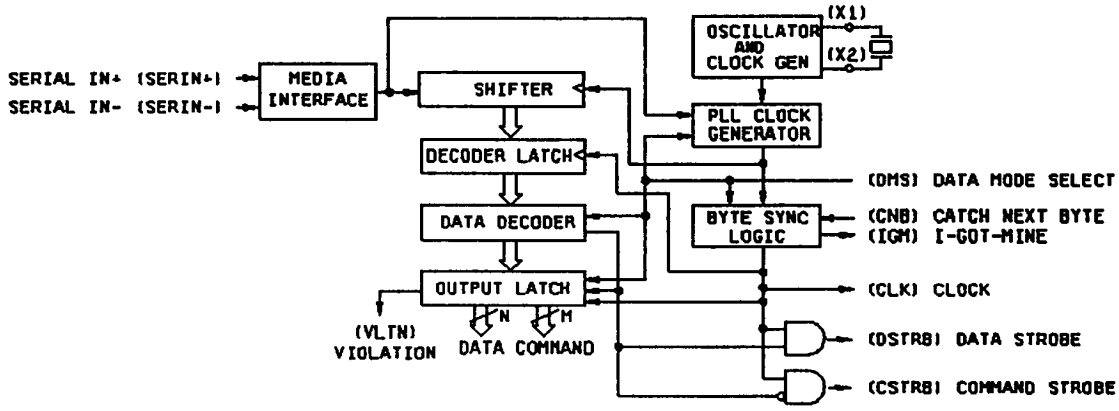
FIGURE 2. Truth table.

Command symbols					
Transparent asynchronous transmitter (5962-90527)				Transparent asynchronous receiver (5962-90528)	
Command input				Command output	
Hex	Binary	Encoded symbol	Mnemonic	Hex	Binary
Symbol 8-bit transparent asynchronous transmitter interface					
0 No STRB (note 1)	0000 No STRB (note 1)	XXXXX XXXXX 11000 10001	Data JK (8-bit sync)	No change (note 2) 0	No change (note 2) 0000
1	0001	11111 11111	II	1	0001
2	0010	01101 01101	TT	2	0010
3	0011	01101 11001	TS	3	0011
4	0100	11111 00100	IH	4	0100
5	0101	01101 00111	TR	5	0101
6	0110	11001 00111	SR	6	0110
7	0111	11001 11001	SS	7	0111
8 (note 3)	1000	00100 00100	HH	8	1000
9	1001	00100 11111	HI	9	1001
A (note 3)	1010	00100 00000	HQ	A	1010
B	1011	00111 00111	RR	B	1011
C	1100	00111 11001	RS	C	1100
D (note 3)	1101	00000 00100	QH	D	1101
E (note 3)	1110	00000 11111	QI	E	1110
F (note 3)	1111	00000 00000	QQ	F	1111
9-bit transparent asynchronous transmitter interface					
0 No STRB (note 1)	000 No STRB (note 1)	XXXXXX XXXXX 011000 100011	Data LK (9-bit sync)	No change (note 2) 0	No change (note 2) 000
1	001	111111 11111	I'I	1	001
2	010	011101 01101	T'T	2	010
3	011	011101 11001	T'S	3	011
4	100	111111 00100	I'H	4	100
5	101	011101 00111	T'R	5	101
6	110	111001 00111	S'R	6	110
7	111	111001 11001	S'S	7	111
10-bit transparent asynchronous transmitter interface					
0 No STRB (note 1)	00 No STRB (note 1)	XXXXXX XXXXXX 011000 100011	Data LM(10-bit sync)	No change (note 2) 0	No change (note 2) 00
1	01	111111 111111	I'I'	1	01
2	10	011101 011101	T'T'	2	10
3	11	011101 111001	T'S'	3	11

Notes:
1. Command pattern sync cannot be explicitly sent by the transmitter with any combination of inputs and STRB, but is used to pad between user data.
2. A strobe with all 0's on the command input lines will cause data to be sent. See figure 2(encoder patterns).
3. While these commands are legal data and will not disrupt normal operation if used occasionally, they may cause data errors if grouped into recurrent fields. Normal PLL operation cannot be guaranteed if one or more of these commands is continuously repeated.

FIGURE 2. Truth table - Continued.

Functional block diagram



NOTE: N can be 8, 9, or 10 bits total of N + M = 12

Logic symbol

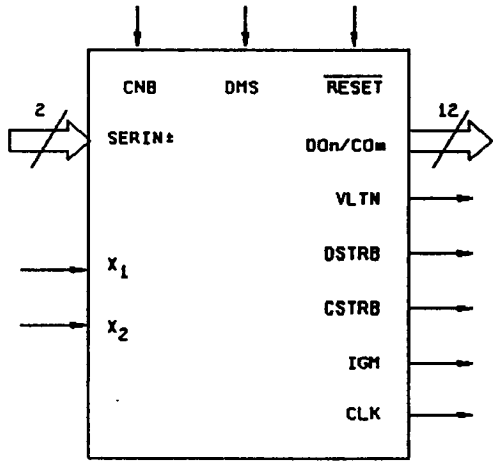


FIGURE 3. Functional block/logic diagram.

Key to switching waveforms

WAVEFORM SYMBOL	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

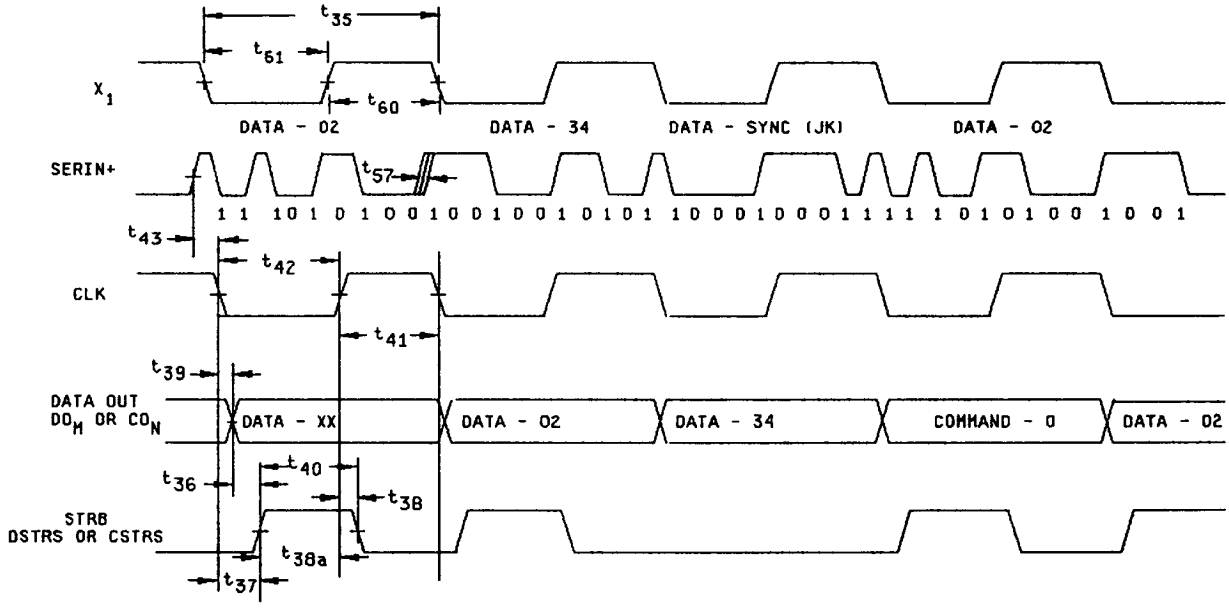


FIGURE 4. Switching waveforms and test circuit.

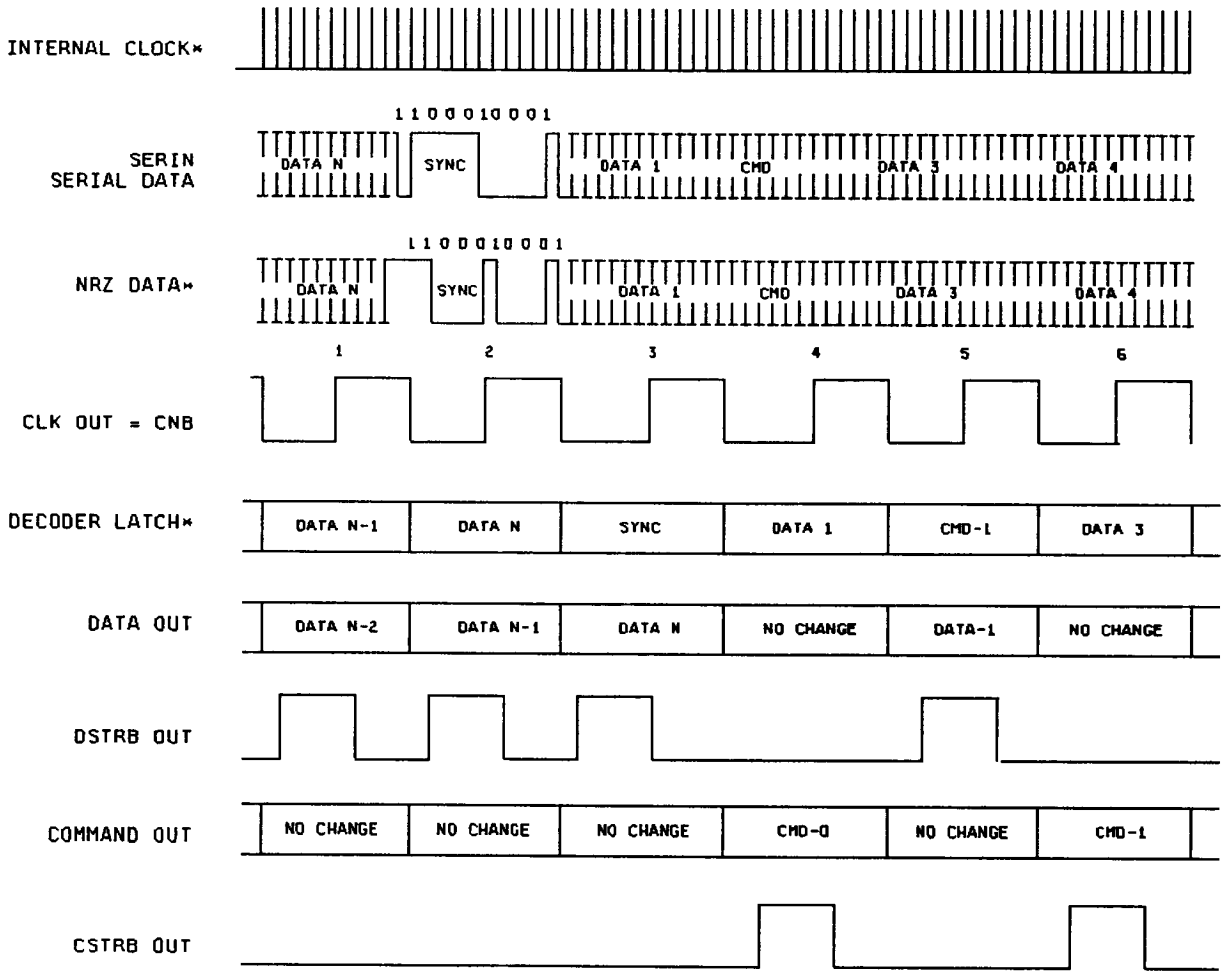
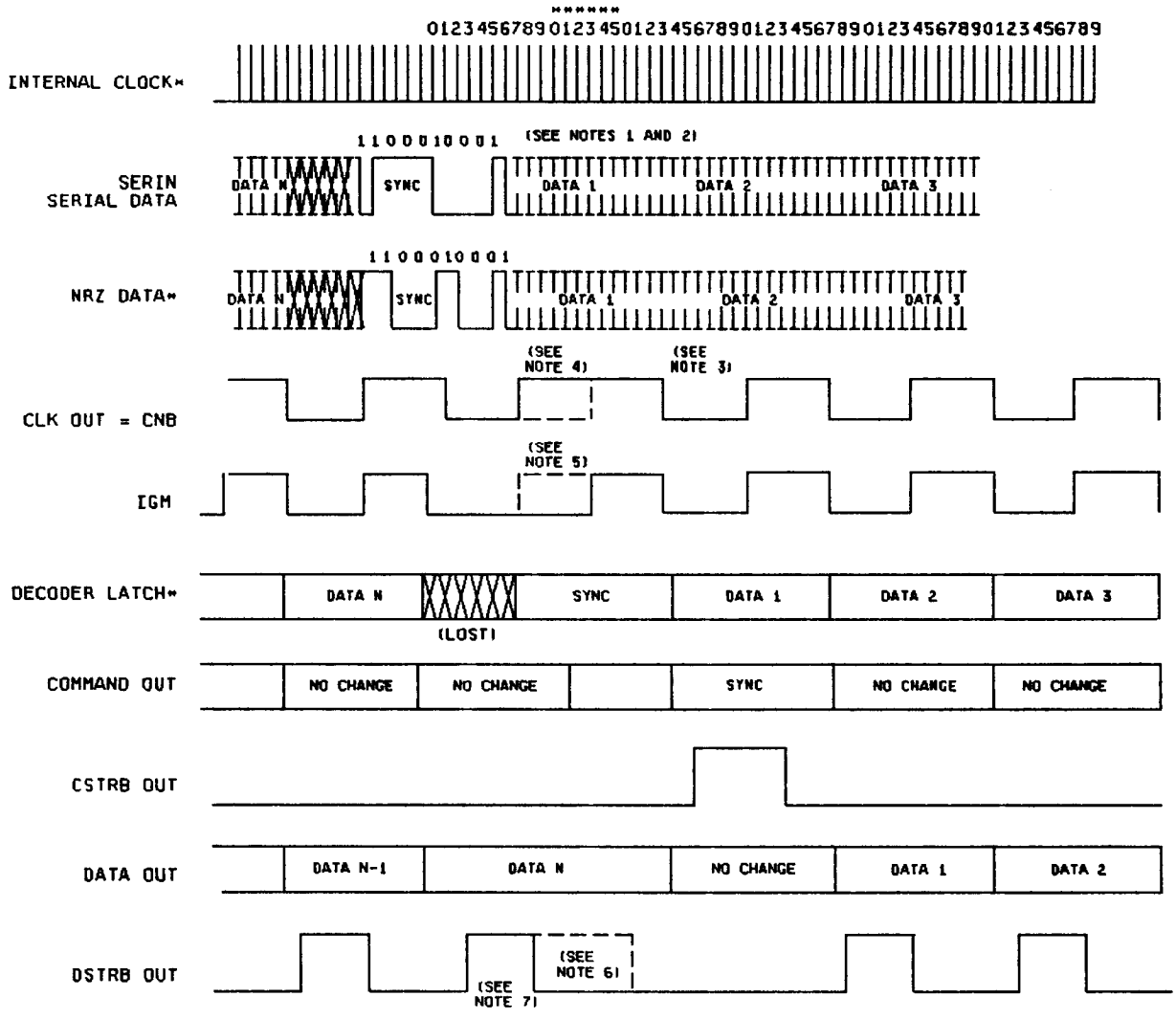


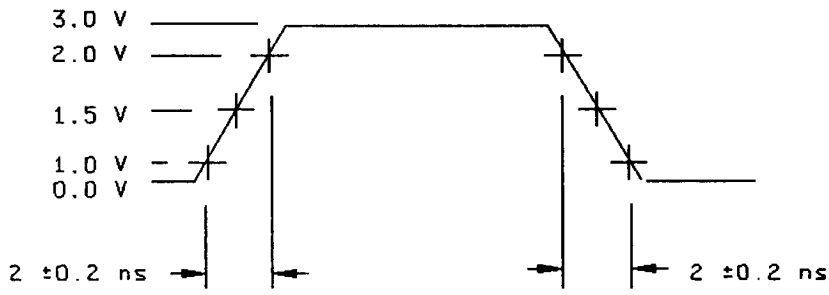
FIGURE 4. Switching waveforms and test circuit - Continued.



Receiver timing (8-bit mode/local) showing external effect of sync error.
* Internal signals

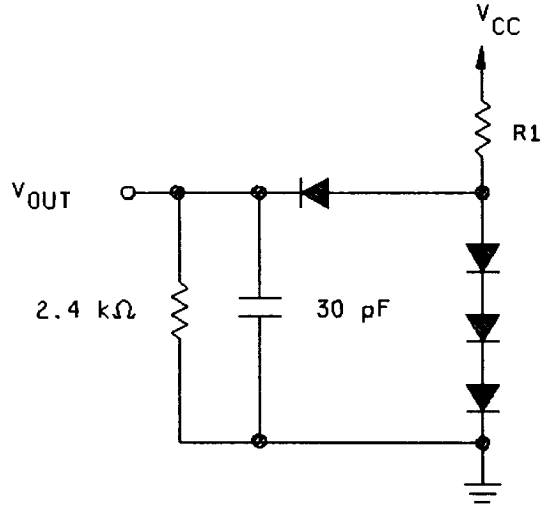
NOTES:
1. Sync detected in shifter, but not synchronized with internal state machine.
2. State machine re-synched to new sync position.
3. Clock output delayed to new position.
4. The low time or high time gets stretched depending on what state of the internal machine is reset.
5. IGM rises at the 6.5th state of the state machine.
6. Strobe falls at the rising edge of the clock out.
7. Strobe may be shifted one bit time if the state machine is reset at state 1.

FIGURE 4. Switching waveforms and test circuit - Continued.



TTL INPUT WAVEFORM

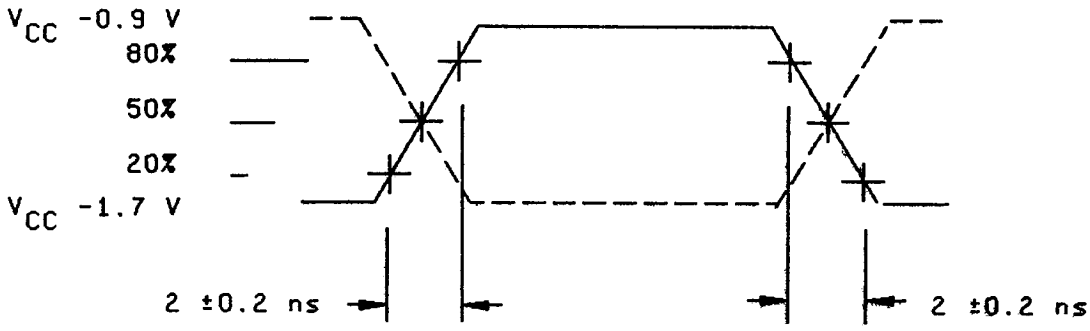
(USED FOR TABLE I
AC ELECTRICAL
PERFORMANCE TESTING)



TTL OUTPUT LOAD

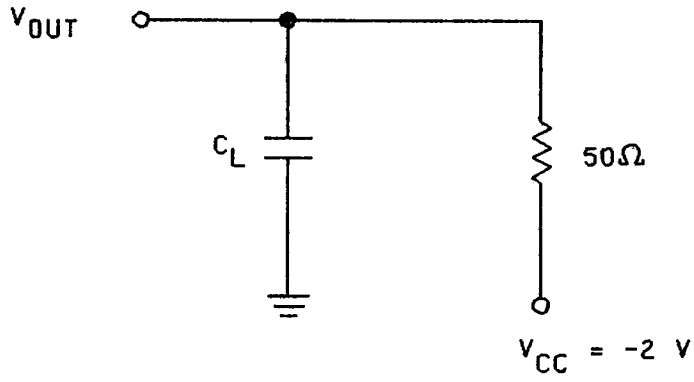
NOTES:
1. R_1 = 500Ω for the I_{OL}= 8 mA.
2. All diodes IN916 or IN3064, or equivalent.
3. C_L= 30 pF includes scope probe, wiring and stray capacitances without device in test fixture. Automatic test equipment load configurations and forcing functions are used, therefore this load figure is for reference only.

FIGURE 4. Switching waveforms and test circuit - Continued.



ECL INPUT WAVEFORM

(USED FOR TABLE I
AC ELECTRICAL
PERFORMANCE TESTING)



ECL OUTPUT LOAD

NOTES:
1. $C_L \leq 3$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. Automatic test equipment load configurations and forcing functions are used, therefore this load figure is for reference only.

FIGURE 4. Switching waveforms and test circuit - Continued.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)		•	1,7		1,7
Final electrical parameters (see 4.2)	1/ 1,2,3 7,8,9 10,11	1/ 1,2,3 7,8,9 10,11	2/ 1,2,3 7,8,9 10,11	1/ 1,2,3 7,8,9 10,11	2/ 1,2,3 7,8,9 10,11
Group A test requirements (see 4.4)	1,2,3,4 7,8,9, 10,11	1,2,3,4 7,8,9, 10,11	1,2,3,4 7,8,9, 10,11	1,2,3,4 7,8,9, 10,11	1,2,3,4 7,8,9, 10,11
Group B end-point electrical parameters (see 4.4)			2,8A,10		
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3		1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331 and as follows:

Symbol	Name and function
DO_0 - DO_7	Parallel data out (TTL inputs). These eight (8) outputs reflect the most recent data received by the 7969 receiver.
DO_8/CO_3	Parallel data (8) out or command (3) out (TTL input). DO_8/CO_3 output is either data or command, depending upon the state of DMS.
DO_9/CO_2	Parallel data (9) out or command (2) out (TTL input). DO_9/CO_2 output will be either a data or command bit, depending upon the state of DMS.
CO_0 - CO_1	Parallel command in (TTL outputs). These two (2) outputs reflect the most recent command data received by the 7969 receiver.
DSTRB	output data strobe (TTL output) The rising edge of this output signals the presence of new data on the DO_0-DO_9 lines. Data is valid just before the rising edge of DSTRB.
CSTRB	Command data strobe (TTL output) The rising edge of this output signals the presence of new data on the DO_0-DO_9 on the CO_0-CO_3 lines. Command bits are valid just before the rising edge of CSTRB.
VLTN	Violation (TTL output) The rising edge of this output indicates that a transmission error has been detected. It changes state at the same time DOi or COi change and will be followed by either DSTRB or CSTRB. This pin goes LOW when the next valid byte is decoded.
IGM	I-got-mine (TTL output) This pin is not used for Military Applications, it's operation is not guaranteed.
CLK	Clock (TTL I/O). This is a free-running clock output which runs at the byte rate, and is synchronous with the serial transfer rate. It falls at the time that the decoder latch is loaded from the Shifter, and rises at mid-byte. The CLK output of the receiver is not suitable as a frequency source for another TAXI transmitter or receiver. It is intended to be used by the host system as a clock synchronous with the received data.

6.5 Abbreviations, symbols, and definitions - continued.

CNB	Catch next byte input (TTL input) In local mode, CNB must be connected to the receiver CLK output. Each received byte will be captured, decoded and latched to the outputs. If the CNB input is high, it allows the 7969 receiver to capture the first byte after a sync. The 7969 receiver will wait for another sync before latching the data out, and capturing another. If CNB is toggled low, it will react as if it had decoded a sync byte.
SERIN+, SERIN-	Differential serial data in (ECL inputs). Data is shifted serially into the shifter. The SERIN+ and SERIN- differential ECL inputs accept ECL voltage swings, which are referenced to +5.0 V. When SERIN- is grounded, the 7969 is put into test mode; SERIN+ becomes a single-ended ECL Input, the PLL clock generator is bypassed, and X_1 determines the bit rate (rather than the byte rate). Both pins have internal pull down resistors which cause unterminated inputs to stay low.
X_1, X_2	Crystal 1 (input), crystal 2 (output). These two crystal pins connect to an internal parallel mode oscillator which operates at the fundamental frequency of the crystal. During normal operation, the byte rate matches the crystal frequency. Alternatively, X_1 can be driven by an external frequency source. In multiple TAXI systems, this external source could be another 7968's CLK output. In In this case, X_2 should be grounded.
DMS	Data mode select (input). Data mode select input determines the data pattern width. When it is wired to GND, the 7969 receiver will assume data to be eight bits wide, with four bits command. When it is wired to V_{CC}, the 7969 receiver will assume data to be nine bits wide, with three bits of command. If DMS is left floating (or terminated to 1/2 V_{CC}), the 7969 receiver will assume data to be ten bits wide, with two bits of command.
$\overline{\text{Reset}}$	PLL Reset (input). This pin is normally left open, but can be momentarily (1 ms minimum) grounded to force the internal PLL to reactivate lock. This allows for correction in the unlikely occurrence of PLL lockup on application of power. $\overline{\text{Reset}}$ has an internal pull-up resistor (50 K nominal) which causes it to float high when left unconnected.
V_{CC1}, V_{CC2},	Power supply. V_{CC1} and V_{CC2} are +5.0 volt nominal power supply pins. V_{CC1} powers TTL and V_{CC2} powers internal logic and analog circuitry.

6.5 Abbreviations, symbols, and definitions - Continued.

GND_1, GND_2	Ground pins. GND_1 is a TTL I/O ground and GND_2 is logic and analog ground.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.