HDTV 1.5 Gbit/s Re-timer GD14526

Preliminary

General Information

The GD14526 Re-timer is designed for 1.2 Gbit/s - 1.5 Gbit/s point-to-point serial transmission systems such as HDTV signals according to SMPTE292. Alternatively the GD14526 can be configured to operate in the 300 Mbit/s - 375 Mbit/s range.

The device provides a fully integrated solution for Clock Recovery and Data (CDR) Re-timing and includes an output driver for 50/75 Ω cables. The CDR can be bypassed for data rates outside the VCO range.

The Clock and Data Recovery circuit consists of:

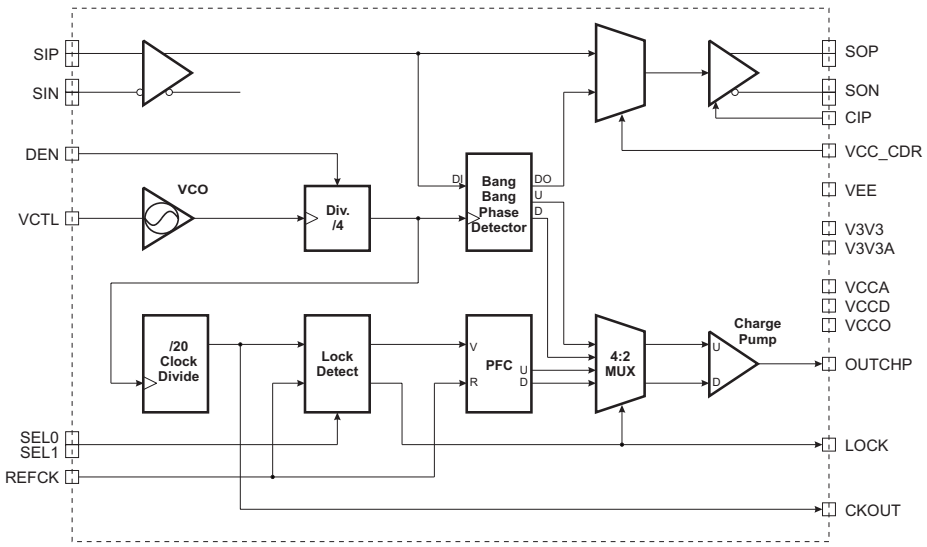
- a Bang-Bang Phase Detector (PD) with data re-timing
- a Phase-Frequency Comparator (PFC)
- a Lock Detect Circuit (LDC) with Lock Alarm Output
- a Tristatable Charge Pump
- a wide tuning range VCO.

The VCO centre frequency is determined by the REFCK multiplied by 20. The loop filter time constant is determined by an external RC filter.

When in lock, the digital Lock Detect Circuit (LDC) uses the incoming data to control the PLL. When not in lock, i.e. the VCO frequency is more than 500 ppm away from the REFCK frequency, the LDC switches to the local clock (REFCK) until the VCO frequency once more enters the ±500 ppm range. Then it switches back to the PD, comparing the VCO clock to the incoming data stream. The LDC continuously monitors the VCO frequency against the REFCK input, clearing LOCK if the VCO leaves the lock range.

The high-speed data input is differential and compatible with PECL levels. It is connected via loop-through transmission lines to minimise stub related reflections. The open collector cable driver has differential outputs and the current in the output stage can be adjusted to a maximum of 36 mA.

The GD14526 is packaged in a 40 pin leaded Multi Layer Ceramic (MLC) package with cavity down for easy cooling.



Features

- Two operating ranges:
  - 1.2 -1.5 Gbit/s
  - 300 - 375 Mbit/s
- Jitter in accordance with SMPTE292.
- High-speed data input and output use Loop-through bondings to reduce reflections.
- Complete Clock/20, Data Recovery, and Lock Acquisition on one IC.
- Digitally controlled capture and lock.
  - Full capture range with true Phase/Frequency detect between VCO-CLK and REFCK.
  - Bang-Bang Phase Detector between VCO-CLK and DATA.
  - Lock in range ±500 ppm or ±2000 ppm referred to REFCK.
  - Lock Alarm Output.
- Re-timed differential 50/75 Ω cable driver output with external termination resistors.
- Supply operation: 5 V and 3.3 V.
- Power dissipation: 1100 mW typ.
- Power down mode for bypass operation.
- 40 pin Multi Layer Ceramic (MLC) leaded package with transmission lines.

Applications

- HDTV Studio equipment.
- Gigabit Ethernet

Function Details

The Clock and Data Recovery (CDR) part of the GD14526 consists of:

- an Input Amplifier
- a Voltage Controlled Oscillator (VCO)
- a Phase Detector (PD)
- a Loop Filter Circuit
- a Charge Pump
- a Phase-Frequency Comparator (PFC)

The Charge Pump performs the transformation between the digital error signal of the Phase Detector and the voltage controlling the Oscillator.

The true Phase-Frequency Comparator is used when acquiring lock and a Lock Detection circuit determines whether or not the PLL is locked onto incoming data.

A selectable divide-by-4 (DEN input) following the on-chip oscillator provides two tuning ranges for the VCO:
1200 - 1500 MHz (DEN = “0”)
300 - 375 MHz (DEN = “1”).

The Phase Detector

The *Phase Detector* (PD) used in the CDR is designed to give minimum static phase error of the PLL. It is of the true digital type (Bang-Bang), producing a binary output. It samples data prior to, in the vicinity of and after any potential bit transition. When a transition has occurred the value of the sample in the vicinity of the transition tells whether the VCO clock leads or lags the incoming data and the PD produces a binary output accordingly. Hence the PLL is controlled by the bit transition point.

The output of the PD is binary with three values indicating whether the VCO must go UP or DOWN in frequency, if a bit transition has occurred, or stay, if not (consecutive “1"s or ”0"s). This information is fed into the Charge Pump, which transfers it into three output levels:

- sinking current
- sourcing current
- tristating the output.

The output of the Charge Pump is integrated and filtered outside the chip by two resistors and a capacitor. The initial values have been determined to 27 Ω and 1 μF, with a resistor of 330 Ω connected in series with the charge pump output to decrease loop-gain. These values can be altered to achieve the optimal characteristics for the application.

The Phase Frequency Comparator

The *Phase-Frequency Comparator* (PFC) ensures predictable lock up conditions for the GD14526. It is used during acquisition, and serves as means to pull the VCO into the range of the data rate where the Phase Detector is capable of acquiring lock. The detector is of the Set-Reset type, comparing the edges of the VCO frequency divided by 20 and the local reference clock (REFCK).

The output of the PFC tells whether the VCO must be adjusted UP or DOWN, proportional to the phase error between the clocks. This information is fed into the Charge Pump, which provides sinking or sourcing current for the loop filter capacitor.

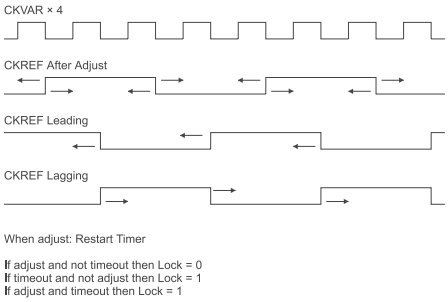


Figure 1. *Lock Detect Scheme.*

The REFCK input is a single ended TTL input with a 1.4 V threshold.

The Lock Detect Circuit

The *Lock Detect Circuit* (LDC) is the guaranty of a fast and reliable lock up. It monitors the difference between the divided VCO clock and the reference clock (REFCK) when the PLL is locked onto the incoming data by the PD. If the difference between the divided VCO clock and the clock reference is greater than ±500 ppm, the LDC considers the PLL to be out of lock and switches to the PFC to pull the VCO frequency into the data rate range.

When LDC has monitored the VCO frequency to be within the data rate range over a period corresponding to ±500 ppm, it switches back to the PD and starts acquiring lock onto data. This way the recovered output clock is always kept within the ±500 ppm, regardless of the serial data line is active or not.

Power Down Mode

GD14526 has been designed with a Power Down mode to allow data to bypass the re-timer. This can be useful in applications with multiple data rates.

Please note that even in Power Down mode the appropriate supply voltages should always be applied to the V_{3V3}, V_{CC} and V_{EE} pins:

CDR (V_{CC_cdr} = +5V):
Re-timed repeater with CDR, VCO and Lock Detect active.

Bypass (V_{CC_cdr} = 0V):
Asynchron repeater with only serial input and output active.

V_{CC_cdr} requires approximately 1 mA and can be switched by 5V CMOS logic.

Applications

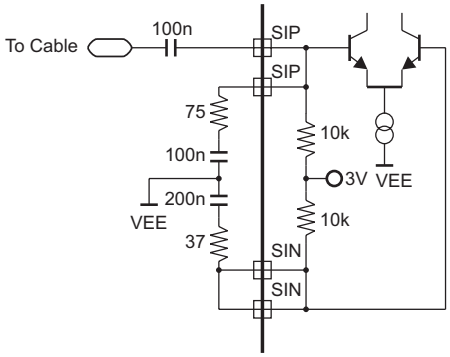


Figure 2. *Standard Input Configuration*

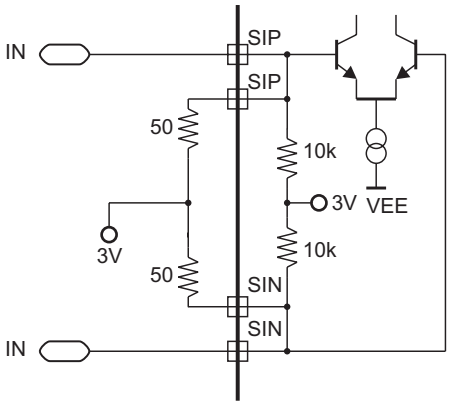


Figure 3. *PECL Input Configuration*

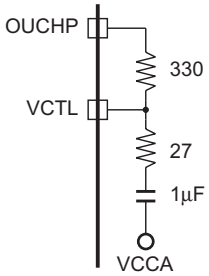


Figure 4. *Loop Filter*

Note: Decoupling should be made from VCC to VEE plane. Use 33 nF chip capacitors close to package pins.

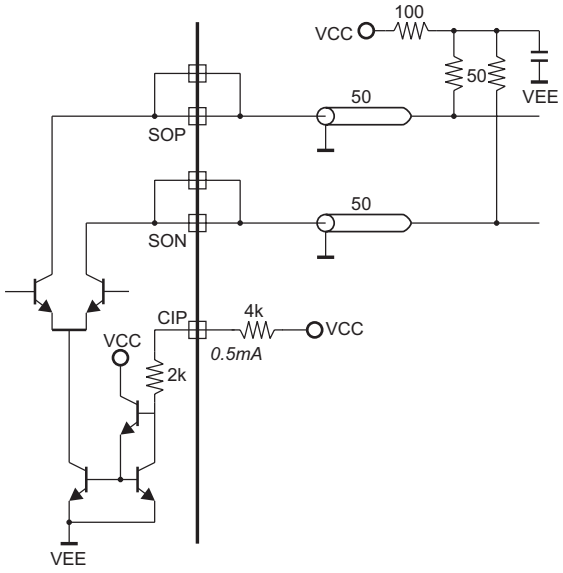


Figure 5. *Differential, PECL Driver*

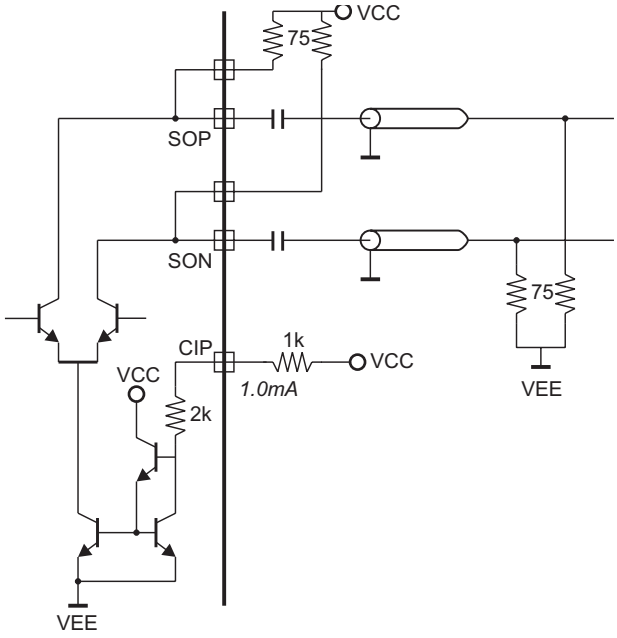


Figure 6. *Dual 75 Ω Cable Driver*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
SIP SIN	14, 15 12, 13	Analog IN	Serial data input (differential). Compatible with PECL levels. Loop-back termination: Each input is connected to two pins, one for input and the other for the termination resistor. See Figures on page 3.
SOP SON	9, 10 6,7	Open Collector	Differential serial data output. High speed Open Collector outputs to be used with 75 Ω cable or 50 Ω termination for optical transmitter. See Figures on page 3.
CIP	16	Analog IN	DC-Current control input for SOP, SON: 1 mA current into CIP generates 25 mA bias for the differential output stage. Maximum setting is for 36 mA output stage bias. If CIP is pulled low, the output stage will turn off.
CKOUT	28	TTL OUT	Regenerated output clock, VCO frequency divided by 20.
REFCK	23	TTL IN	Reference clock input with frequency equal to data rate divided by 20.
SEL0	24	TTL IN	Lock Detect Range select “0” ± 2000 ppm “1" ± 500 ppm
SEL1	17	TTL IN	PLL override “0” PFC always used “1” Lock Detect Circuit selects PFC or PD
LOCK	22	TTL OUT	CDR Lock alarm output. When low, the divided VCO frequency deviates more than ±500/±2000 ppm from REFCK.
VCTL	18	Analog IN	VCO control voltage input.
OUCHP	21	Analog OUT	Charge Pump output providing sink or source current for the integrating capacitor in the external loop filter. See Figure 4 on page 3.
DEN	25	TTL IN	Control of VCO divide by 4 “0” disable divide by 4 “1” enable divide by 4
VCC_CDR	26	PWR CTL	Power Down of re-timer. “0” power down (asyncr. repeater) “1” enable re-timer
V3V3	3, 30, 32, 39	PWR	+3.3 V power for data path.
V3V3A	20	PWR	+3.3 V power for PFC and CDR.
VCCA	19	PWR	+5 V power for VCO.
VCCD	5, 8	PWR	+5 V power for cable driver.
VCCO	4, 29, 38	PWR	+5 V power for TTL I/O.
VEE	1, 2, 11, 27, 31, 33, 34, 35, 36, 37, 40	PWR	0 V power.

Package Pinout

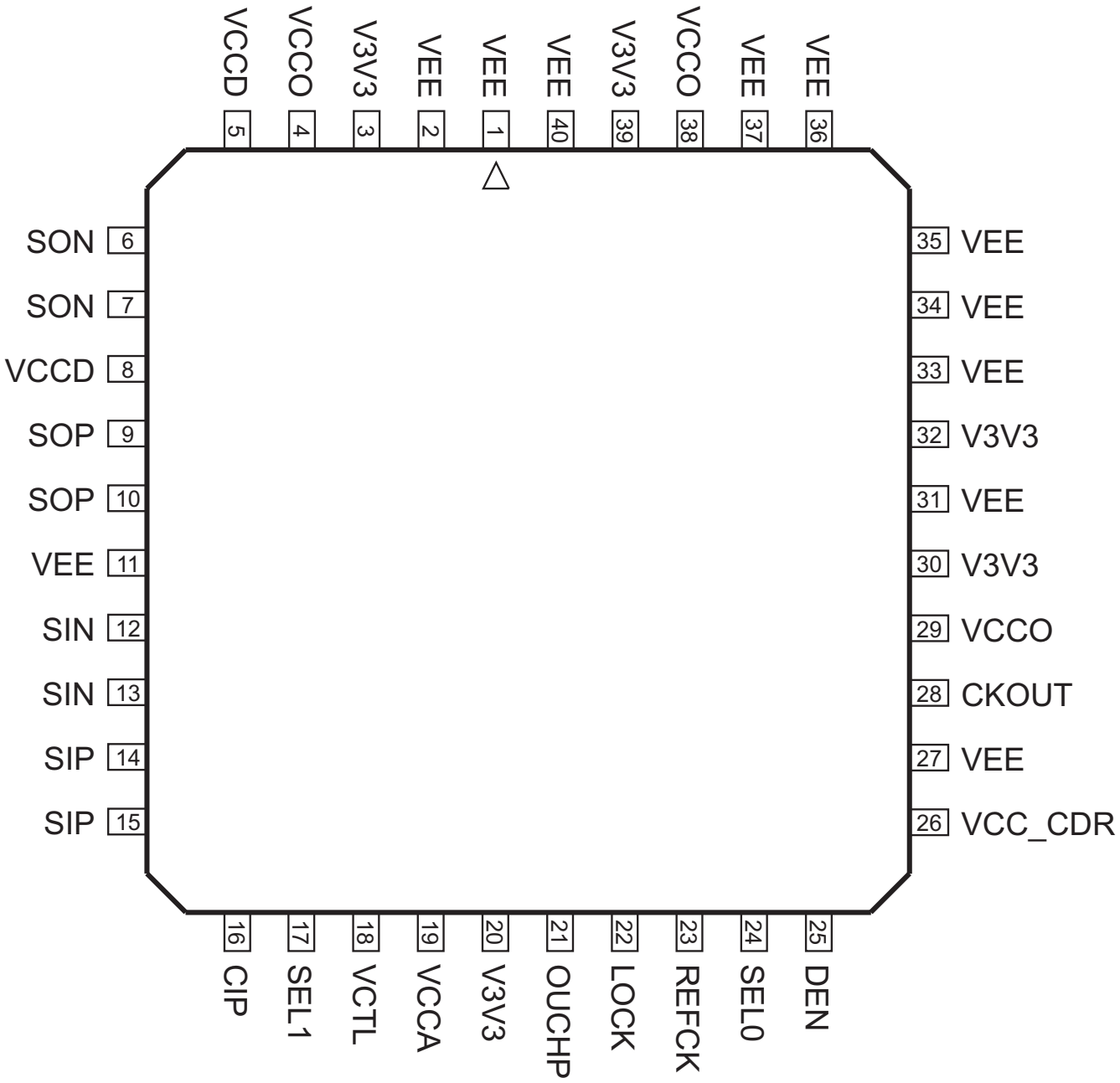


Figure 7. *Package 40 pin MLC - Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{3V3}, V_{CC}	Positive Supply		V_{EE} -0.5		7	V
$V_{I\ max,\ CIP}$	Input Voltage for CIP		V_{EE} -0.5		V_{CC} +0.5	V
$I_{I\ max,\ CIP}$	Input Current for CIP		-1.0		3.0	mA
$V_{O\ max}$	Output Voltage		V_{EE} -0.5		V_{CC} +0.5	V
$I_{O\ max}$	Output Current				40	mA
$V_{I\ max}$	Input Voltage		V_{EE} -0.5		V_{CC} +0.5	V
$I_{I\ max}$	Input Current		-1.0		1.0	mA
T_O	Operating Temperature	Junction	-40		+125	°C
T_S	Storage Temperature		-65		+175	°C

Note 1: Temperature range specify only reliability regarding damage. Performance is only tested and quaranteed for the T_{CASE} as given below.

DC Characteristics

T_{CASE} = 0 °C to 70 °C, $\theta_{J\text{-}C}$ = 9°C/W. Appropriate heat sinking is required.
All voltages in the table are referred to V_{EE} .

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC} V_{CCA} V_{CCO}	5 V Supply Voltage		4.75	5.00	5.25	V
I_{CC}	Total Supply Current V_{CC} , V_{CCA} , V_{CCO}			165		mA
V_{3V3}	3.3 V Supply Voltage		3.1	3.3	3.5	V
I_{3V3}	Total Supply Current V_{3v3}			85		mA
PD	Power Dissipation			1100		mW
$V_{C\ SIP/SIN}$	SIP/SIN Data Common Mode Voltage		V_{CC} -2.0		V_{CC} -0.5	V
$V_{I\ SIP/SIN}$	SIP/SIN Data Minimum Input Voltage SIP/SIN Data Maximum Input Voltage	Note 1		200	400 1000	$mV_{P\text{-}P}$ $mV_{P\text{-}P}$
$V_{IIH\ TTL}$	TTL Input HI Voltage		2.0		4.0	V
$V_{IIL\ TTL}$	TTL Input LO Voltage				0.8	V
$I_{IH\ TTL}$	TTL Input HI Current	$V_{IH\ max}$			500	µA
$I_{IL\ TTL}$	TTL Input LO Current	$V_{IL\ min}$			-500	µA
$V_{OH\ TTL}$	TTL Output HI Voltage	Note 2	2.4			V
$V_{OL\ TTL}$	TTL Output LO Voltage	Note 2			0.5	V
$I_{OH\ SOP/SON}$	Open Collector Output HI Sink Current	Note 3	-20	-25	-36	mA
$I_{OL\ SOP/SON}$	Open Collector Output LO Sink Current	Note 3			-0.5	mA
V_{VCTL}	VCO Control Voltage	I_{VCTL}< 30 µA	0.5		V_{CC} -1.5	V
$I_{OH\ CHP}$	OUCHP Source Current (DC steady)	Note 4	500	1000		µA
$I_{OL\ CHP}$	OUCHP Sink Current (DC steady)	Note 4	-500	-1000		µA

Note 1: Data eye diagram in accordance with SMPTE292, terminated via loop-through to 75 Ω.
Note 2: R_{load} = 500 Ω to 1.4 V.
Note 3: R_{load} = 50 Ω to V_{CC}. Current into CIP =1 mA. Output logic level “1" corresponds to LO sink current into output.
Note 4: Output terminated to 2.5 V during test.

AC Characteristics

T_{CASE} = 0 °C to 70 °C
V_{CC} = 5.0 V, V_{3V3} = 3.3 V

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{Tol}	Jitter Tolerance	10Hz < F < 150MHz (Note1) 100kHz < F < 150MHz (Note1)	1.0 0.2			UI_{P-P} UI_{P-P}
J_{Trf}	Jitter Transfer	F < Loop bandwidth (Note 2)		0.1		dB
T_A	Acquisition Time	2^{23}-1 PRBS		5	50	µs
L_{CID}	Consecutive Identical Digits	# of bits with no transitions	100			bits
D_C	Input Clock / REFCK Frequency Deviation	Note 3			±200	ppm
$C_{DUTY\ REFCK}$	REFCK Clock Duty Cycle	$V_{Thresh.}$ = 1.4 V	40		60	%
$C_{DUTY\ CKOUT}$	Output Clock Duty Cycle	Note 4	45		55	%
$T_{TLH\ Clock}$	CKOUT Rise Time	20 - 80% (Note 4)		2000		ps
$T_{THL\ Clock}$	CKOUT Fall Time	80 - 20% (Note 4)		2000		ps
$T_{TLH\ SON/SOP}$	SOP/SON Rise Time	1 m cable, 75 Ω load			270	ps
$T_{THL\ SON/SOP}$	SOP/SON Fall Time	1 m cable, 75 Ω load			270	ps

Note 1: 1 UI = 673 ps. Measured according to RP184: Measurement of Jitter in Bit-Serial Digital Interfaces.
Note 2: Data Pattern 2^{23}-1 PRBS. Through careful filter design, loop peaking may be controlled which is the major contribute to Jitter Transfer.
Note 3: Maximum deviation between reference clock input and divided clock when in lock.
Note 4: Threshold voltage = 1.4 V. Load = 500 Ω || 10 pF to 1.4 V.

Reference Standards

SMPTE 292M (May 7, 1996): Bit-Serial Digital Interface for HDTV
SMPTE RP184 (April 1, 1995): Measurement of Jitter.

Package Outline

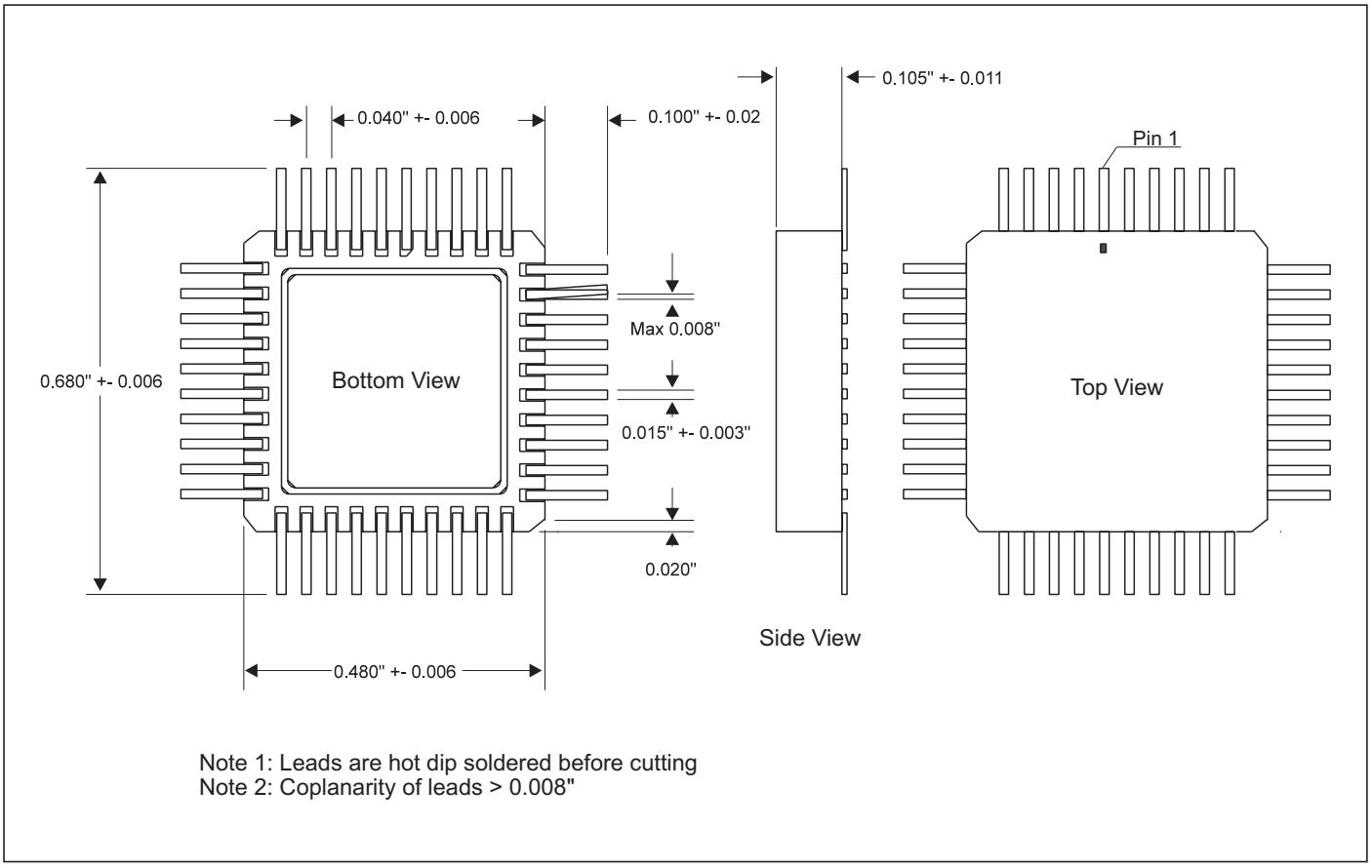


Figure 8. *Package 40 pin MLC - all dimensions are in inch.*

Ordering Information

To order, please specify as shown below:

Product Name:	**Package Type:**	**Case Temperature Range:**	**Option:**
GD14526-40BA	40 pin MLC	0..70°C	

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