

SRAM

1 MEG x 1 SRAM

LOW VOLTAGE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 17, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ± 0.3 power supply
- Easy memory expansion with \overline{CE} option
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

OPTIONS

- **Timing**
 - 15ns access -15
 - 17ns access -17
 - 20ns access -20
 - 25ns access -25
- **Packages**
 - Plastic DIP (400 mil) None
 - Plastic SOJ (400 mil) DJ
- 2V data retention (optional) L
- 2V data retention, low power (optional) LP
- **Temperature**
 - Commercial (0°C to +70°C) None
- Part Number Example: MT5LC1001DJ-20 L

MARKING

NOTE Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations

GENERAL DESCRIPTION

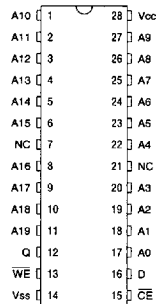
The MT5LC1001 is organized as a 1,048,576 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable (\overline{CE}) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

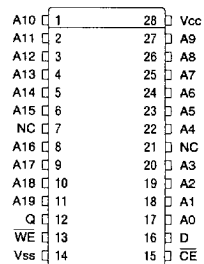
Writing to this device is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH while \overline{CE} goes LOW. The device offers a reduced power standby mode when dis-

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-5)



28-Pin SOJ (SD-3)



3.3V ASYNCHRONOUS SRAM

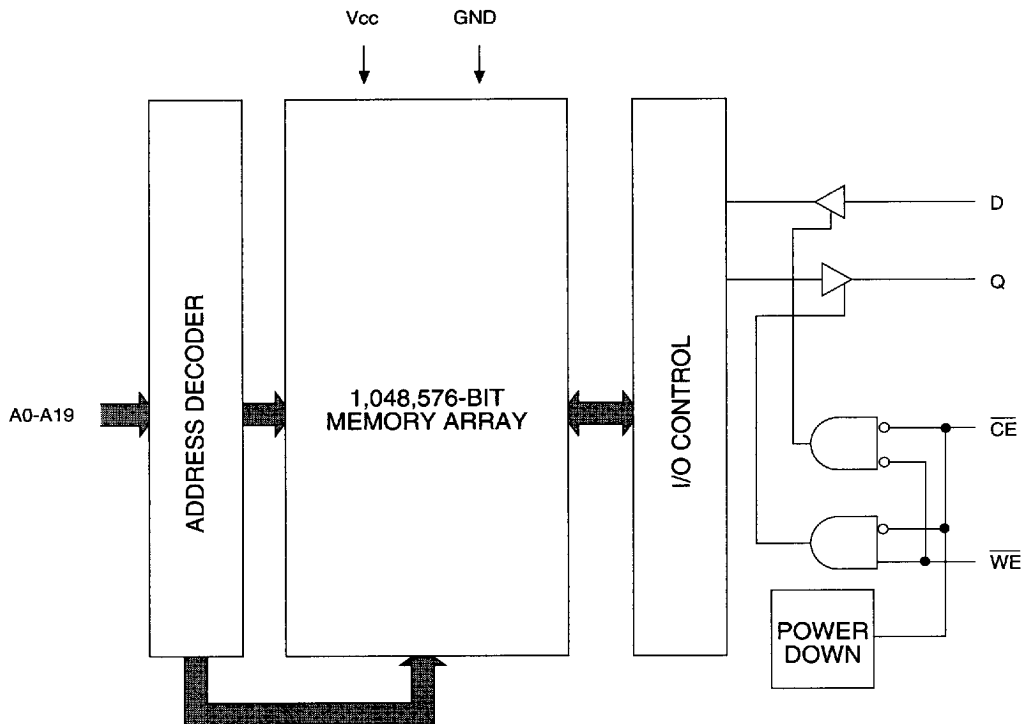
abled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the \overline{WE} and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM

3.3V ASYNCHRONOUS SRAM



TRUTH TABLE

MODE	\overline{CE}	\overline{WE}	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	-0.5V to +4.6V
V _{IN}	-0.5V to +6.0V
Storage Temperature (plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
 $(0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}; V_{CC} = 3.3\text{V} \pm 0.3\text{V})$

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V _{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$	I _{LI}	-1	1	μA	
Output Leakage Current	Output(s) disabled $0\text{V} \leq V_{OUT} \leq V_{CC}$	I _{LO}	-1	1	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{CC}	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYM	VER	TYP	MAX				UNITS	NOTES
					-15	-17	-20	-25		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ outputs open $f = \text{MAX} = 1/RC$	I _{CC}	ALL	70	155	145	135	125	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ outputs open $f = \text{MAX} = 1/RC$	I _{SB1}	STD, L	20	45	40	35	30	mA	13
			LP	1.5	3	3	3	3	mA	
	$\overline{CE} \geq V_{CC} - 0.2\text{V};$ $V_{CC} = \text{MAX}$ $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq V_{SS} + 0.2\text{V}$	I _{SB2}	STD, L	1.0	3	3	3	3	mA	13
			LP	0.7	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^{\circ}\text{C}; f = 1\text{ MHz}$	C _I	6	pF	4
Output Capacitance	$V_{CC} = 3.3\text{V}$	C _O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Note 5, 13, 15) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$)

DESCRIPTION	SYM	-15		-17		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	¹ RC	15		17		20		25		ns	
Address access time	¹ AA		15		17		20		25	ns	
Chip Enable access time	¹ ACE		15		17		20		25	ns	
Output hold from address change	¹ OH	3		3		3		5		ns	
Chip Enable to output in Low-Z	¹ LZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	¹ HZCE		6		7		8		10	ns	6, 7
Chip Enable to power-up time	¹ PU	0		0		0		0		ns	
Chip disable to power-down time	¹ PD		15		17		20		25	ns	
WRITE Cycle											
WRITE cycle time	¹ WC	15		17		20		25		ns	
Chip Enable to end of write	¹ CW	10		12		12		15		ns	
Address valid to end of write	¹ AW	10		12		12		15		ns	
Address setup time	¹ AS	0		0		0		0		ns	
Address hold from end of write	¹ AH	0		0		0		0		ns	
WRITE pulse width	¹ WP	9		12		12		15		ns	
Data setup time	¹ DS	7		8		8		10		ns	
Data hold time	¹ DH	0		0		0		0		ns	
Write disable to output in Low-Z	¹ LZWE	3		3		3		5		ns	7
Write Enable to output in High-Z	¹ HZWE		6		7		8		10	ns	6, 7

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AC TEST CONDITIONS

Input pulse levels	V _{SS} to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

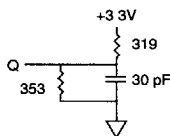


Fig. 1 OUTPUT LOAD EQUIVALENT

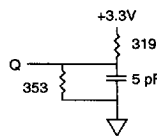


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

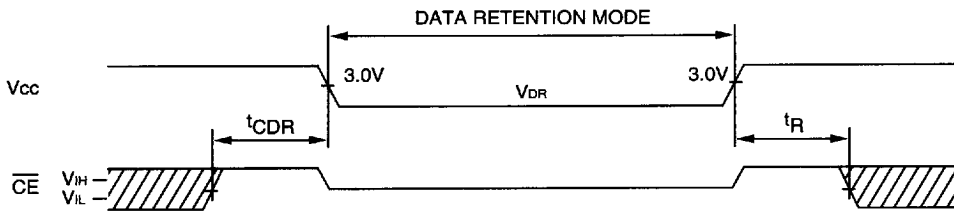
- All voltages referenced to V_{SS} (GND).
- Overshoot: V_{IH} ≤ +6.0V for t ≤ ¹RC/2
Undershoot: V_{IL} ≥ -2.0V for t ≤ ¹RC/2
Power-up: V_{IH} ≤ +6.0V and V_{CC} ≤ 3.1V for t ≤ 200msec.
- I_{CC} is dependent on output loading and cycle rates.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- ¹HZCE and ¹HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
- At any given temperature and voltage condition, ¹HZCE is less than ¹LZCE, and ¹HZWE is less than ¹LZWE.
- ¹WE is HIGH for READ cycle.
- Device is continuously selected. All chip enables and output enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- ¹RC = Read Cycle Time.
- Chip enable and write enable can initiate and terminate a WRITE cycle.
- Typical values are measured at 3.3V, 25°C and 20ns cycle time.
- Typical currents are measured at 25°C.
- Contact the factory for IT/AT/XT specifications.

3.3V ASYNCHRONOUS SRAM

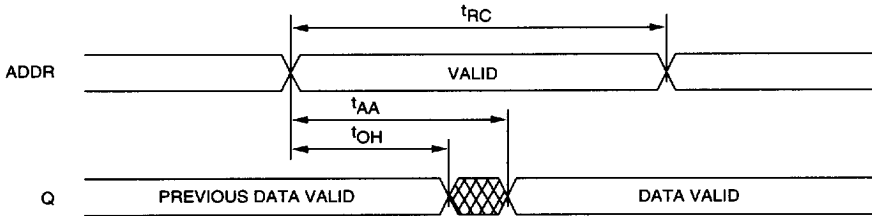
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{CC} for Retention Data		V _{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq V_{CC} - 0.2V$ Other inputs: V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V V _{CC} = 2V	I _{CCDR}		145	260	μA	14
Data Retention Current LP version	$\overline{CE} \geq V_{CC} - 0.2V$ V _{CC} = 2V	I _{CCDR}		145	260	μA	14
Chip Deselect to Data Retention Time		¹ CDR	0			ns	4
Operation Recovery Time		¹ R	¹ RC			ns	4, 11

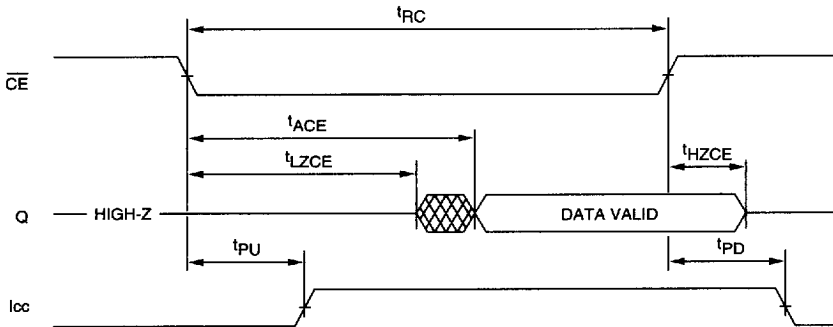
LOW V_{CC} DATA RETENTION WAVEFORM



READ CYCLE NO. 1 ^{8, 9}

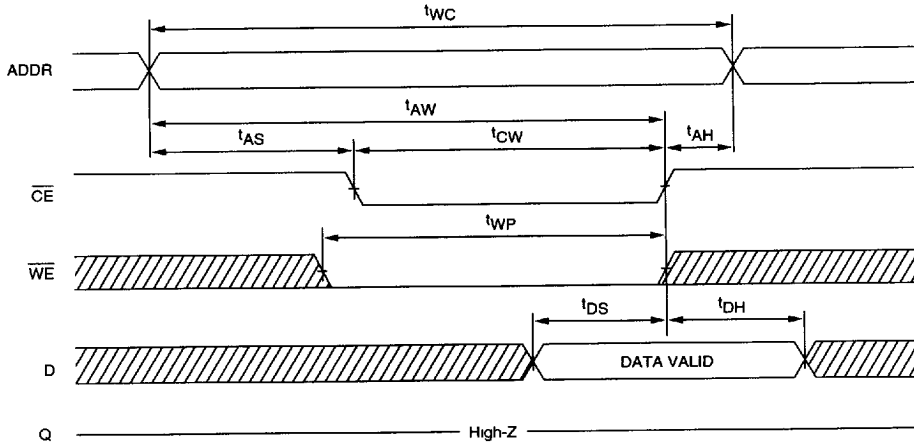


READ CYCLE NO. 2 ^{7, 8, 10}



 DON'T CARE
 UNDEFINED

WRITE CYCLE NO. 1¹²
(Chip Enable Controlled)



WRITE CYCLE NO. 2^{7, 12}
(Write Enable Controlled)

