

PJ4812

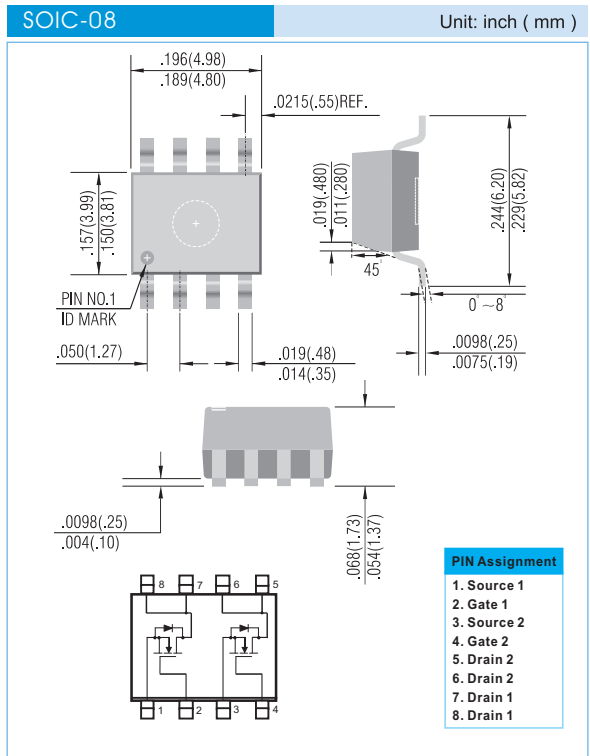
30V N-Channel Enhancement Mode MOSFET

FEATURES

- $R_{DS(ON)}$, $V_{GS}@10V, I_{DS}@8A=17m\Omega$
- $R_{DS(ON)}$, $V_{GS}@5.0V, I_{DS}@6A=34m\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for DC/DC Converters
- Fully Characterized Avalanche Voltage and Current
- Pb free product : 99% Sn above can meet RoHS environment substance directive request

MECHANICAL DATA

- Case: SOIC-08 Package
- Terminals : Solderable per MIL-STD-750D, Method 1036.3
- Marking : 4812



ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ C$ unless otherwise noted)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continous Drain Current	$T_C=25^\circ C$	I_D	8	A
Pulsed Drain Current ⁽¹⁾		I_{DM}	32	A
Avalanche Energy $L=0.1mH, I_D=8A, V_{DD}=25V$		E_{AS}	3.2	mJ
Power Dissipation	$T_C=25^\circ C$	P_D	2.4	W
	$T_C=75^\circ C$		1.2	
Operating Junction and Stroage Temperature Range		T_J, T_{STG}	-55 to +175	$^\circ C$
Junction-to-Ambient Thermal Resistance (PCB Mounted) ²		$R_{\theta JA}$	62.5	$^\circ C/W$

- Note :**
1. Maximum DC current limited by the package
 2. Surface mounted on FR4 board, $t \leq 10$ sec

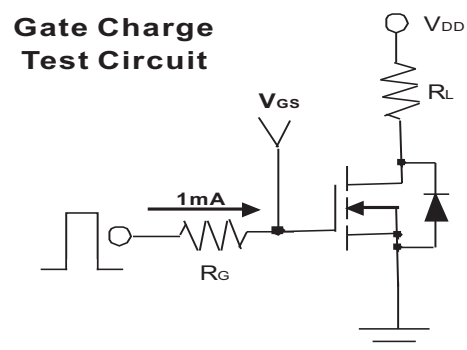
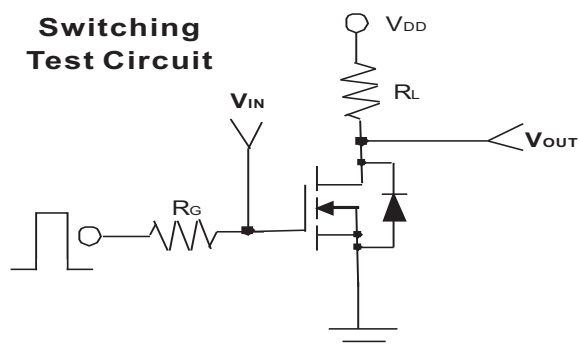
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ELECTRICAL CHARACTERISTICS (T_c=25°C, Unless Otherwise Noted)

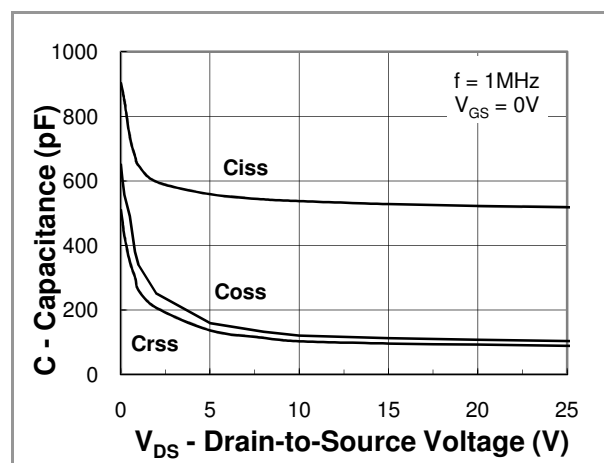
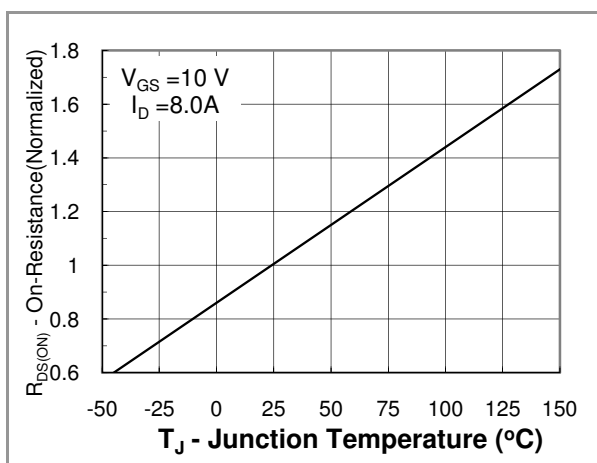
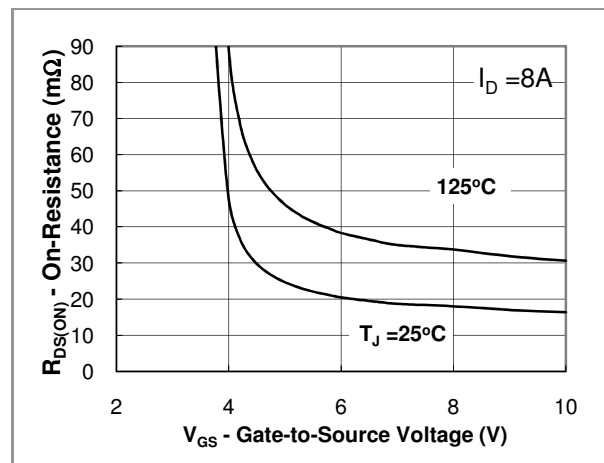
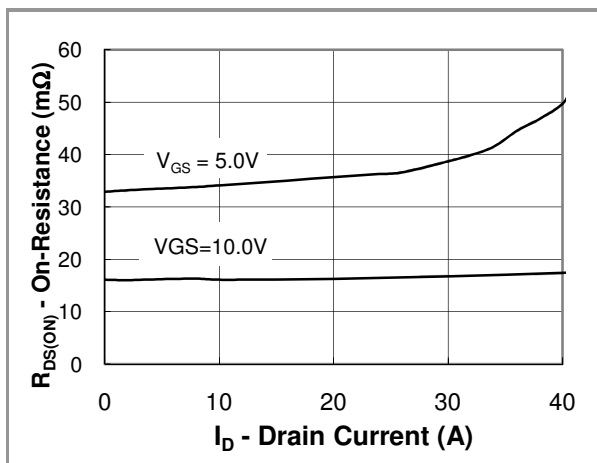
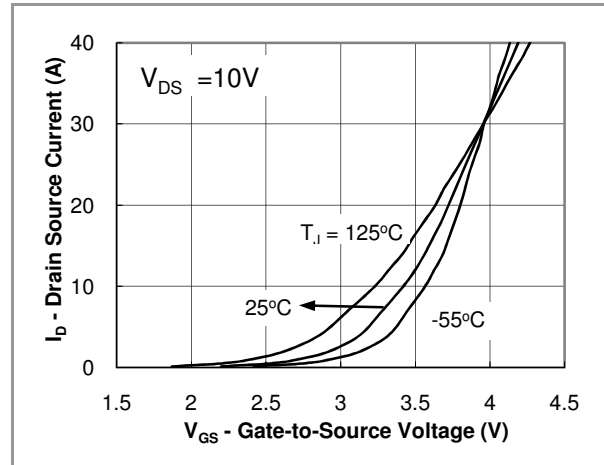
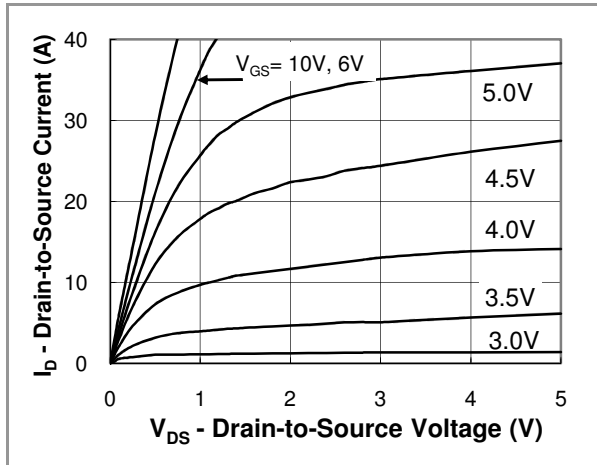
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	30	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	1	-	3	V
Drain-Source On-state Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =8A	-	15	17	mΩ
		V _{GS} =5V, I _D =6A	-	26	34	mΩ
Gate-Body Leakage	I _{GSS}	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V	-	-	1	μA
		V _{DS} =24V, V _{GS} =0V, T _J =125°C	-	-	25	μA
On-State Drain Current	I _{D(ON)}	V _{DS} =10V, V _{GS} =10V	8	-	-	A
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =8A	10	-	-	S
DYNAMIC						
Total Gate Charge	Q _G	V _{DS} =15V, V _{GS} =5V, I _D =8A	-	7.0	-	nC
		V _{DS} =15V, V _{GS} =10V I _D =8A	-	14.2	-	nC
Gate-Source Charge	Q _{GS}		-	1.22	-	nC
Gate-Drain Charge	Q _{GD}		-	3.44	-	nC
Turn-On Delay Time	t _{d(on)}	V _{DS} =15V, I _D =1A, V _{GS} =10V R _{GS} =6Ω	-	7.8	-	nS
Rise Time	t _r		-	11.6	-	nS
Turn-Off Delay Time	t _{d(off)}		-	28.8	-	nS
Fall Time	t _f		-	5.6	-	nS
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =15V f=1MHz	-	520	-	pF
Output Capacitance	C _{OSS}		-	112	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	98	-	pF
Gate Resistance	R _g	V _{GS} =15mV, V _{DS} =0V, f=1MHz	-	2.0	-	Ω
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S		-	-	2.3	A
Forward Voltage	V _{SD}	I _F =2.3A, V _{GS} =0V	-	-	1.2	V

NOTE : Plus Test: Pluse Width ≤ 300us, Duty Cycle ≤ 2%.



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Typical Characteristics Curves ($T_a=25^\circ\text{C}$, unless otherwise noted)





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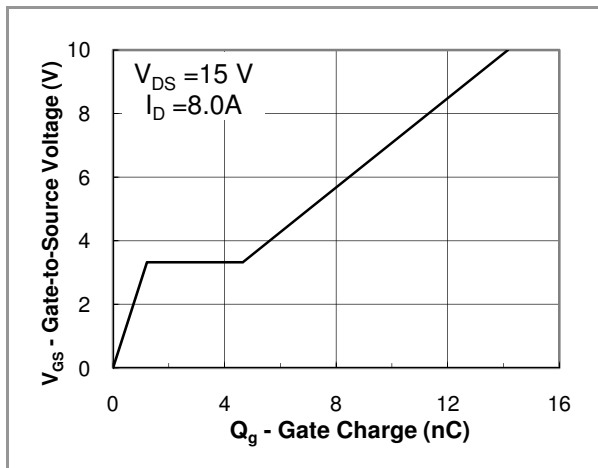


Fig. 7 Gate Charge Waveform

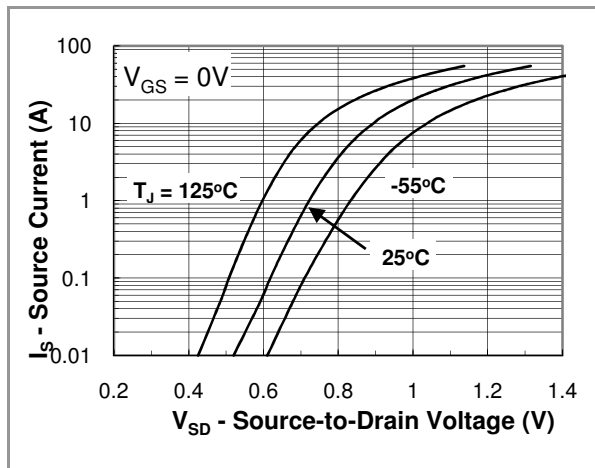


Fig.8 Source-Drain Diode Forward Voltage

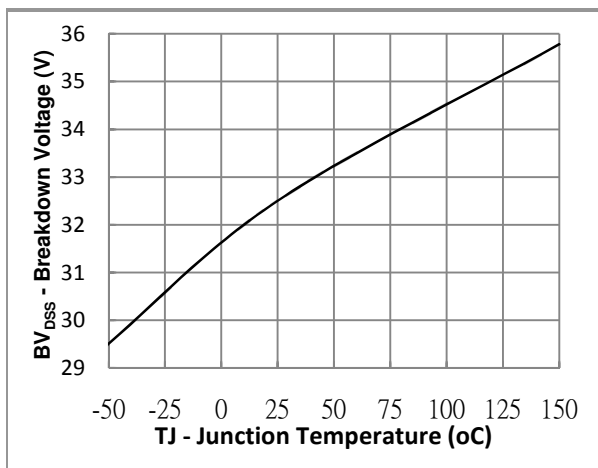


Fig.9 Breakdown Voltage vs Junction Temperature

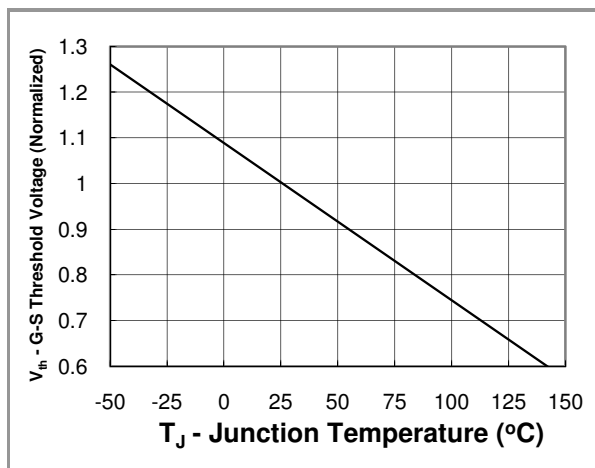
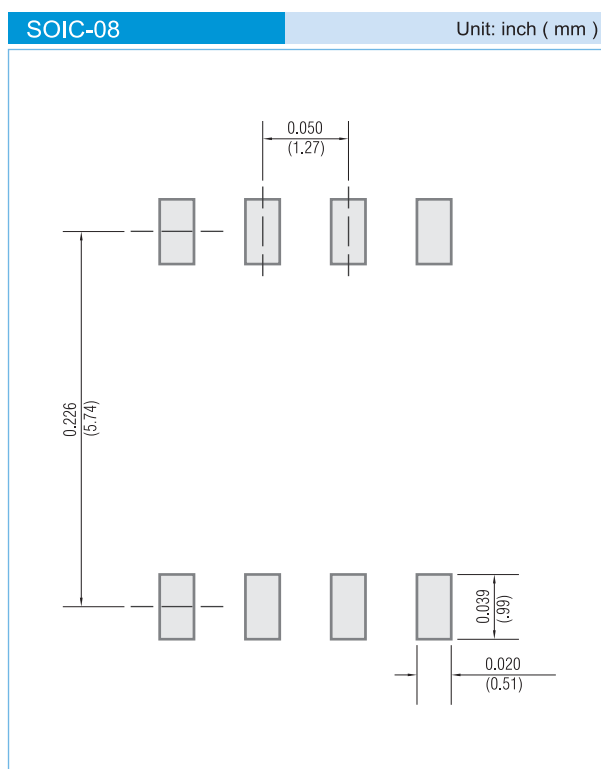


Fig.10 Threshold Voltage vs Junction Temperature

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MOUNTING PAD LAYOUT



ORDER INFORMATION

- Packing information
T/R - 3K per 13" plastic Reel

LEGAL STATEMENT

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