BiCMOS versatile PAL device — ABT22V10A/B

DESCRIPTION

The ABT22V10 is a versatile PAL[1] device fabricated with the Philips BiCMOS process known as QUBiC. The QUBiC process produces a very high speed device (10ns worst case) which has excellent noise immunity. The ground bounce, with 9 outputs switching and the 10th held low is, typically, less than 0.8V.

The ABT22V10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-product equations. This device has a programmable AND array which drives a fixed OR array. The AND array is programmed to create custom product terms while the fixed OR array sums selected terms at the output.

The OR sum of the products feeds the "Output Macro Cell" (OMC) which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. In other words, the architecture provides maximum design flexibility by allowing the Output Macro Cell to be configured by the user.

The ABT22V10 is designed so the outputs can never display a metastable state due to set up and hold time violations. If set up and hold times are violated, the outputs will not glitch or display a metastable state (the propagation delays may, however, be extended).

This device is pin and JEDEC file compatible with industry standard 22V10 and can be used in all standard applications where speed is to be maximized.

Order codes can be found in the Ordering Information table.

FEATURES

- Ultra fast 8.5ns t_{PD} and 7.5ns t_{CO} (for ABT22V10B)
- Pin and JEDEC file compatible to industry standard 22V10
- 10 input/output macro cells for architectural flexibility
- Metastable immune flip-flops
- Low ground bounce (<0.8V typical)
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Power-up reset on all registers
- Synchronous Preset/Asynchronous Reset
- Programmable on standard PAL-type device programmers
- Design support provided using SNAP software development package and other CAD tools for PLDs

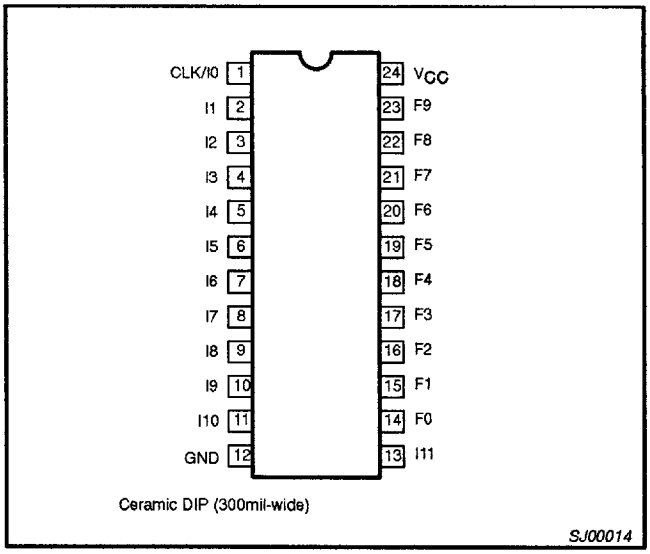
APPLICATIONS

- DMA control
- State machine implementation
- High speed graphics processing
- Counters/shift registers
- SSI/MSI random logic replacement
- High speed memory decoder

PIN LABEL DESCRIPTIONS

I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground

PIN CONFIGURATIONS



Ceramic DIP (300mil-wide)

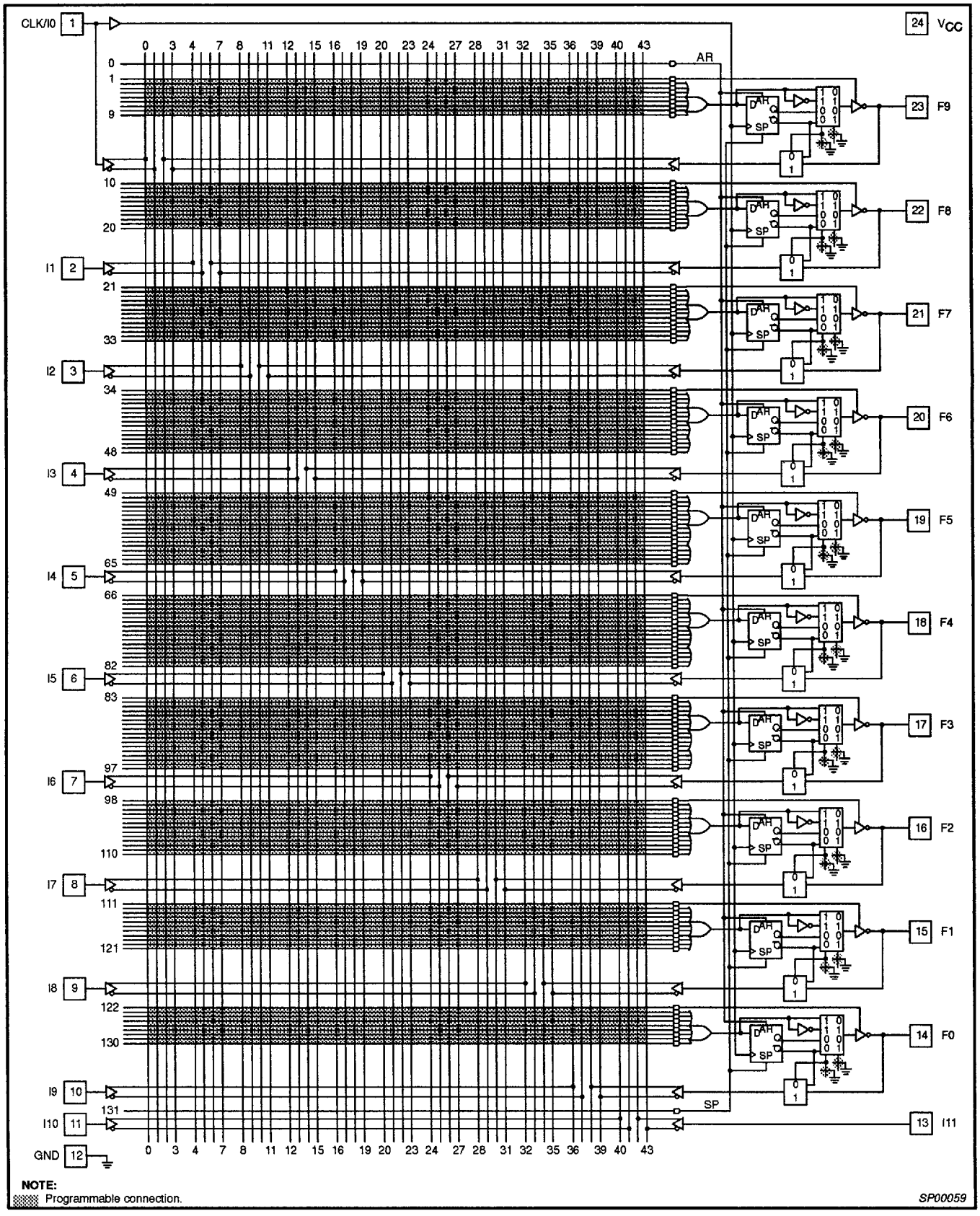
SJ00014

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	SMD NUMBER	t_{PD}	PACKAGE DESIGNATOR*
24-Pin Ceramic DIP 300 mil-wide	ABT22V10A/BLA	5962-91760	10ns	GDIP3-T24
24-Pin Ceramic DIP 300 mil-wide	ABT22V10B/BLA	5962-91760	8.5ns	GDIP3-T24

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

LOGIC DIAGRAM



NOTE:
▒▒ Programmable connection.

SP00059

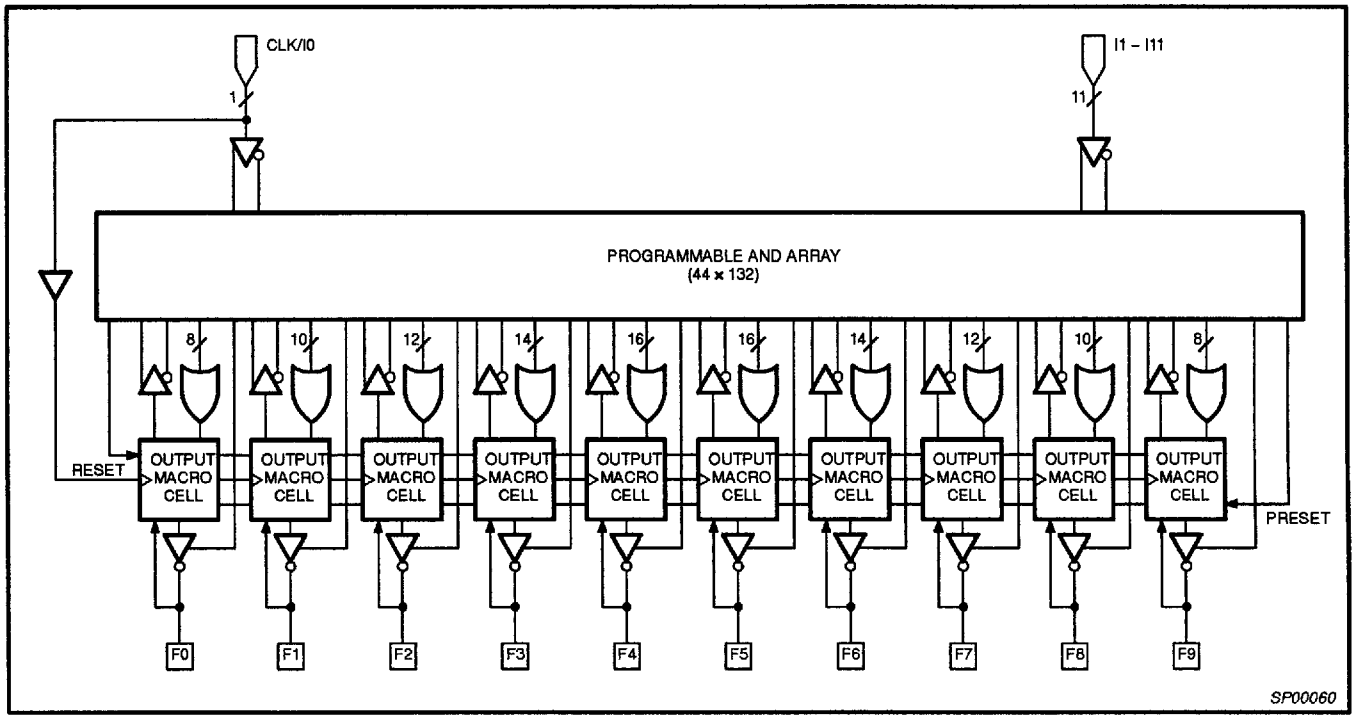


Figure 1. Functional Diagram

FUNCTIONAL DESCRIPTION

The ABT22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both True and Complement of any single input assume the logical LOW state.

The ABT22V10 has 12 inputs and 10 I/O Macro Cells (Figure 1). The Macro Cell allows one of four potential output configurations, registered output or combinatorial I/O, Active-HIGH or Active-LOW (see Figure 7). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 – S_1. Multiplexer controls are connected to ground (0) through a programmable fuse link, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test fuses are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Metastable Immune Characteristics

Philips Semiconductors uses the term 'metastable immune' to describe the output characteristics of registered logic devices. This term means that the outputs will not glitch or display an output anomaly under any circumstances, including set up and hold time violations. This claim is easily verified by following 74F5074 Synchronizing Dual flip-flop example. The ABT22V10 device has been designed using the same metastable immune flip-flop.

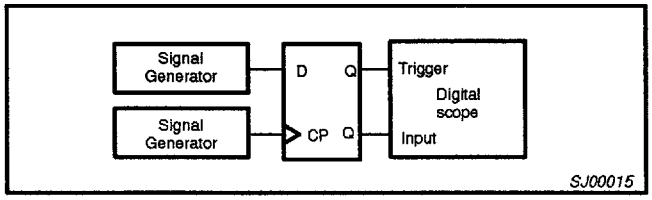


Figure 2. Test Set-up

By running two independent signal generators (see Figure 2) at nearly the same frequency (in this case 10MHz clock and 10.02MHz data) the device-under-test can be often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence, the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device-under-test is an 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Figure [3].

Figure 3 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

COMPARISON OF METASTABLE IMMUNE AND NON-IMMUNE CHARACTERISTICS

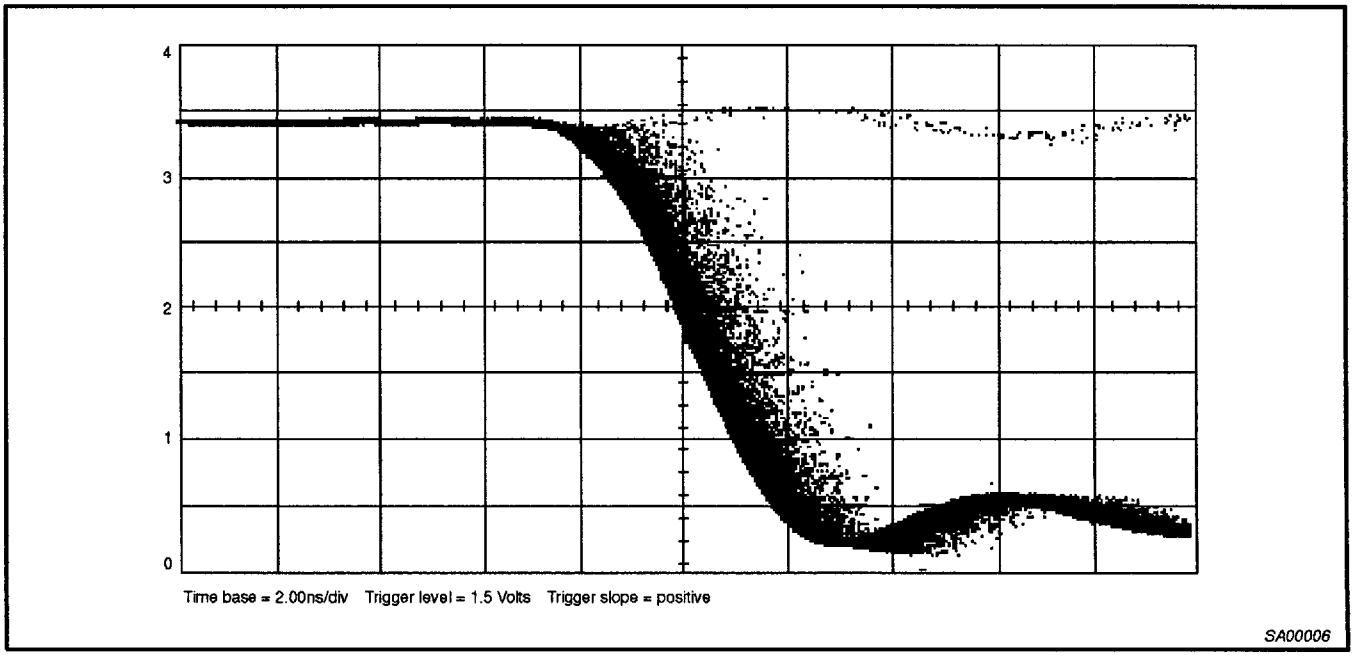


Figure 3. 74F74 $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

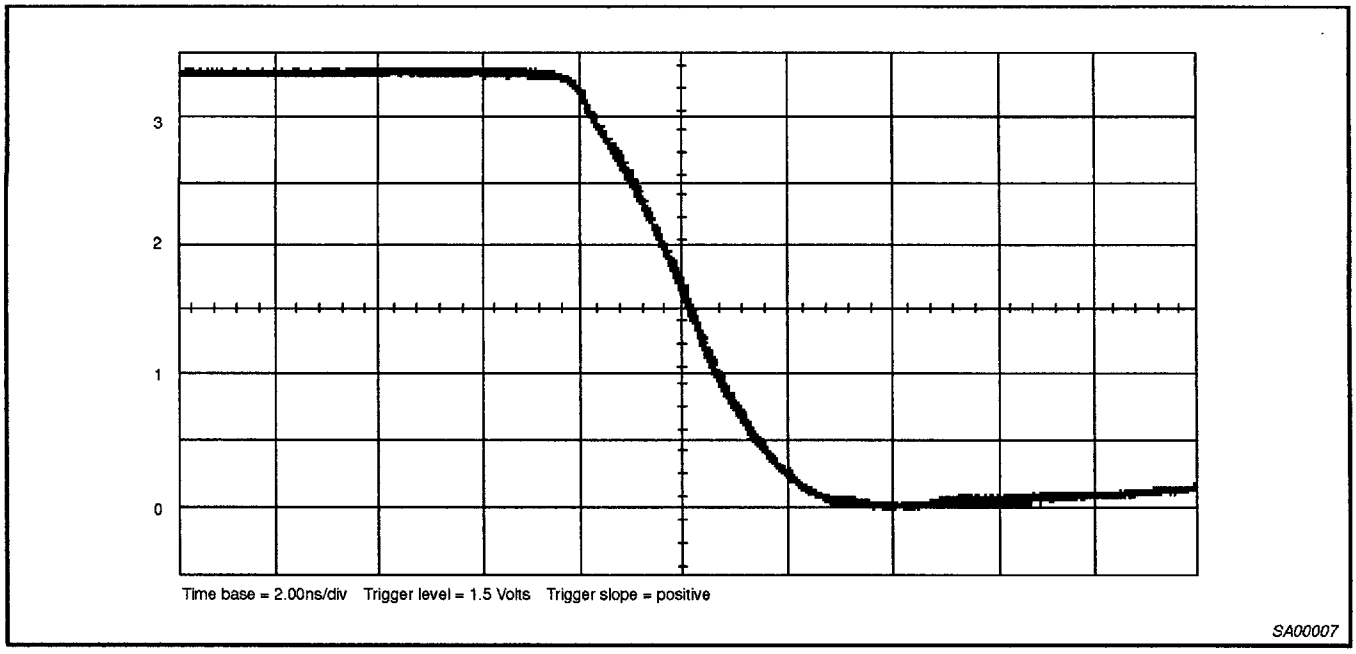


Figure 4. 74F5074 $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

When the device-under-test is a metastable immune part, such as the 74F5074, the waveform will appear as in Figure 4. The 74F5074 output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the ABT22V10A/B and related part types represent state-of-the-art BiCMOS technology.

After determining the T_0 and τ of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F5074 for synchronizing asynchronous data that is

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arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F5074 10ns after the clock edge. He simply plugs his number into the equation below:

$MTBF = e^{(t'/t)} / T_o f_C f_i$

In this formula, f_C is the frequency of the clock, f_i is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' < h, h being the normal propagation delay). In this situation the f_i will be twice the data frequency of (20 MHz) because input events consist of both of low and high transitions. Multiplying f_i by f_C gives an answer of 10^{15} Hz^2. From Figure 5 it is clear that the MTBF for the 74F5074 device is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51 X 10^{10} seconds or about 480 years. The MTBF for the ABT22V10A/B, under the same condition is 5.6 trillion years.

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'

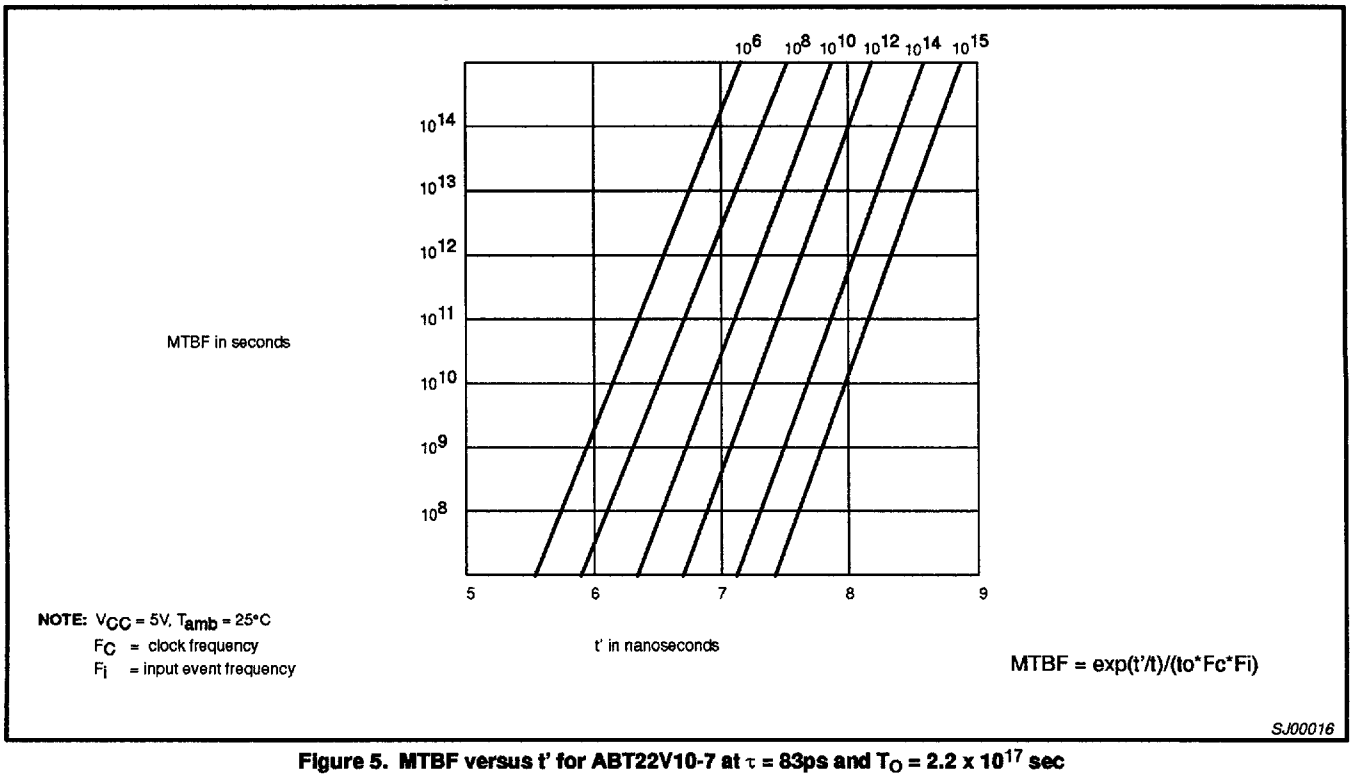

Figure 5. MTBF versus t' for ABT22V10-7 at τ = 83ps and T_O = 2.2 x 10^{17} sec

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.25V	83ps	8.1 X 10^{18} sec	82ps	7.5 X 10^{18} sec	101ps	3.0 X 10^{12} sec
5.0V	80ps	4.0 X 10^{18} sec	83ps	2.2 X 10^{17} sec	98ps	4.4 X 10^{11} sec
4.75V	85ps	3.4 X 10^{14} sec	91ps	2.5 X 10^{12} sec	106ps	1.1 X 10^{8} sec

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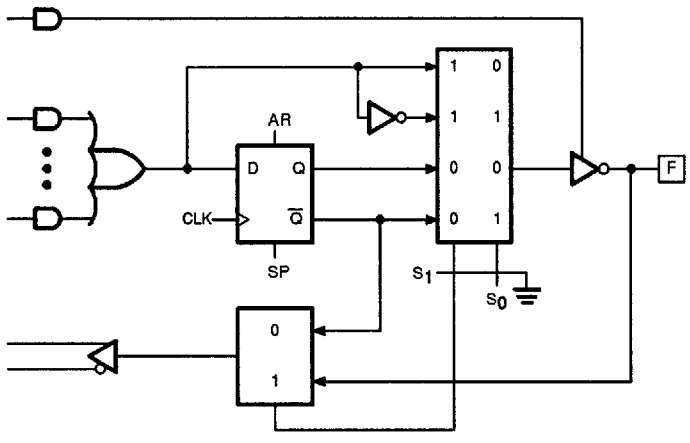
OUTPUT MACRO CELL



S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-LOW

0 = Unprogrammed fuse
1 = Programmed fuse

Figure 6. Output Macro Cell Logic Diagram

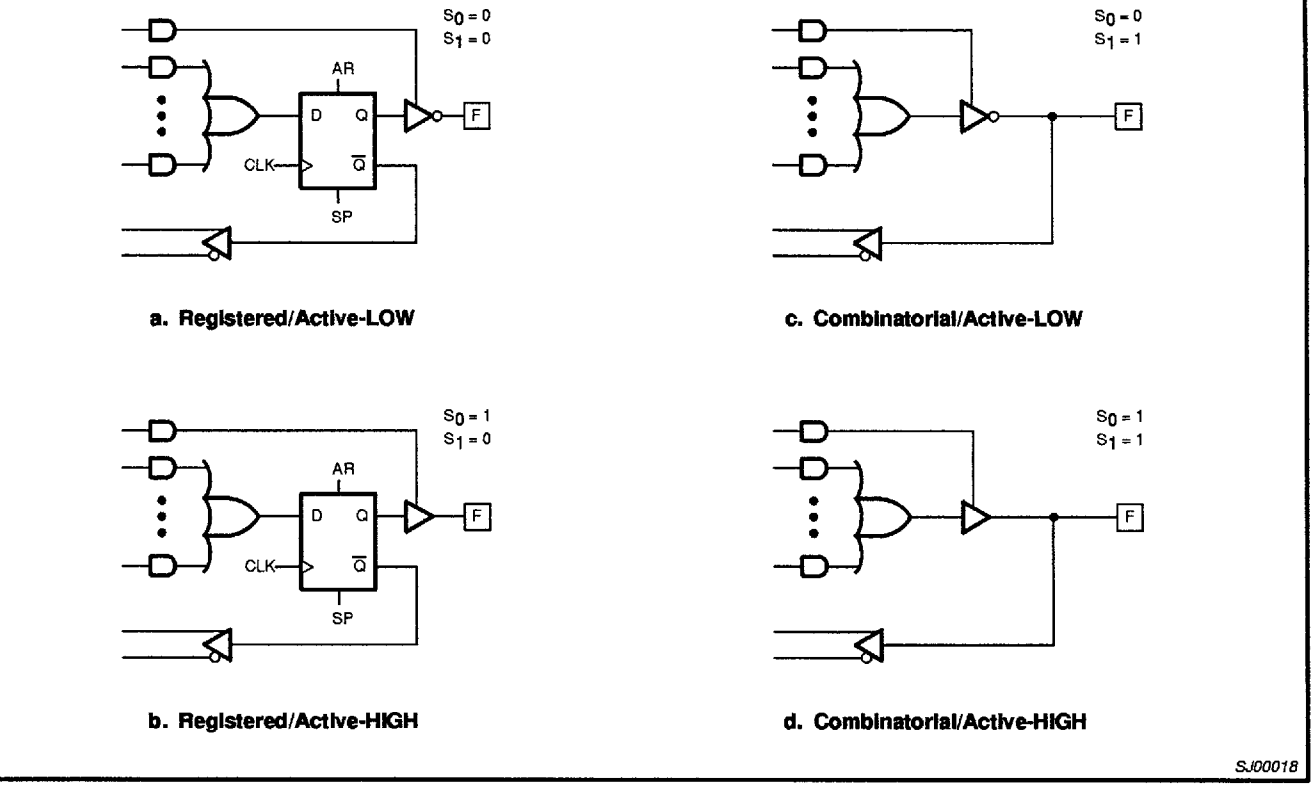


Figure 7. Output Macro Cell Configurations

Registered Output Configuration

Each Macro Cell of the ABT22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any Macro Cell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.

Variable Input/Output Pin Ratio

The ABT22V10 has twelve dedicated input lines, and each Macro Cell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	−0.5	+7.0	V_{DC}
V_{IN}	Input voltage	−1.2	V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	−0.5	V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	−65	+150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	175°C
Maximum ambient	125°C

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	−55	+125	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TA = −55°C to 125° C unless otherwise noted TEST CONDITIONS[1]	LIMITS		UNIT
			MIN	MAX	
Input voltage					
V_{IL}	Low	V_{CC} = MIN		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V
V_I	Clamp	V_{CC} = MIN, I_{IN} = −18mA		−1.2	V
Output voltage					
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}			
V_{OL}	Low	I_{OL} = 30mA		0.5	V
V_{OH}	High	I_{OH} = −16mA	2.4		V
Input current					
		V_{CC} = MAX			
I_{IL} (except Pin 1)	Low	V_{IN} = 0.40V		−25	µA
I_{IL} (Pin 1)	Low	V_{IN} = 0.40V		−50	µA
I_{IH}	High	V_{IN} = 2.7V		25	µA
I_I	Maximum input current	V_{IN} = 5.5V		30	µA
Output current					
		V_{CC} = MAX			
I_{OZH}	Output leakage[3]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 2.7V		100	µA
I_{OZL}	Output leakage[3]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 0.4V		−100	µA
I_{SC}	Short circuit[2]	V_{OUT} = 0.5V	−30	−200	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		190	mA

NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).

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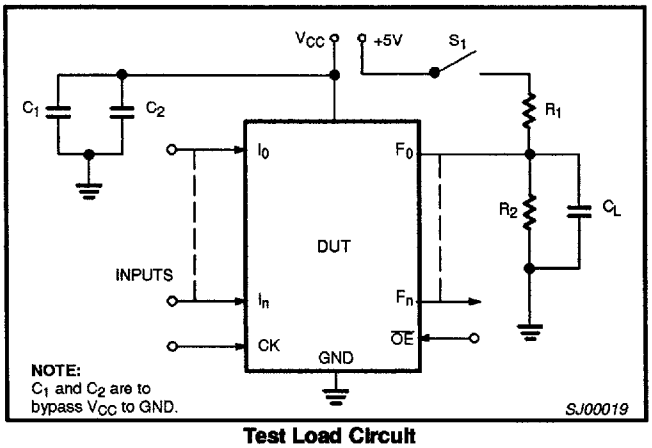
AC ELECTRICAL CHARACTERISTICS

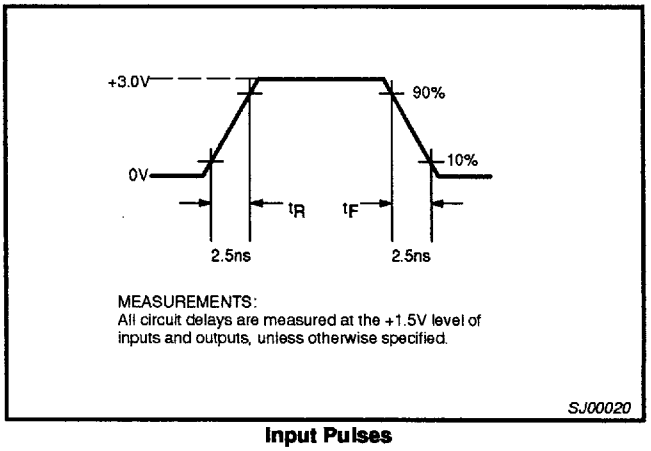
SYMBOL	PARAMETER	TEST CONDITIONS		TA = -55°C to 125° C LIMITS[1]		UNIT
				22V10/A MAX	22V10/B MAX	
t_{PD}	Input or feedback to non-registered output[2]	Active-LOW		10	8.5	ns
		Active-HIGH		10	8.5	
t_S	Setup time from input, feedback or SP to Clock			8.0 min.	6.5 min.	ns
t_H	Hold time[6]			0	0	ns
t_{CO}	Clock to output			10	7.5	ns
t_{CF}	Clock to feedback[3]			3.0	3.0	ns
t_{AR}	Asynchronous Reset to registered output[6]			12.5	12.5	ns
t_{ARW}	Asynchronous Reset width[6]			7.5 min	7.5 min.	ns
t_{ARR}	Asynchronous Reset recovery time[6]			6.0 min.	6.0 min.	ns
t_{SPR}	Synchronous Preset recovery time[6]			6.0 min.	6.0 min.	ns
t_{WL}	Width of Clock LOW[6]			4.0 min.	4.0 min.	ns
t_{WH}	Width of Clock HIGH[6]			4.0 min.	4.0 min.	ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})$[4]			55 min.	71 min.	MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})$[4]			90 min.	105 min.	MHz
t_{EA}	Input to Output Enable[5, 6]			9.0	9.0	ns
t_{ER}	Input to Output Disable[5, 6]			9.0	9.0	ns
Capacitance[6]						
C_{IN}	Input Capacitance (Pin 1) (Typical)	V_{IN} = 2.0V	V_{CC} = 5.0V	6	6	pF
	Input Capacitance (Others) (Typical)	V_{IN} = 2.0V	T_{amb} = 25°C	6	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V	f = 1MHz	8	8	pF

NOTES:

1. Test Conditions: $R_1 = 300\Omega$, $R_2 = 390\Omega$ (see Test Load Circuit).
2. t_{PD} is tested with switch S_1 closed and C_L = 50pF (including jig capacitance). V_{IH} = 3V, V_{IL} = 0V, V_T = 1.5V.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.



Test Load Circuit



Input Pulses

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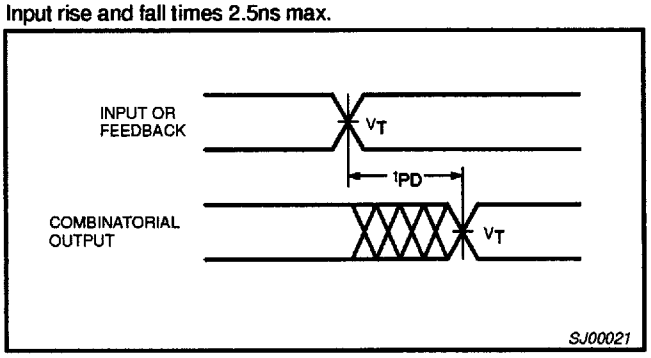
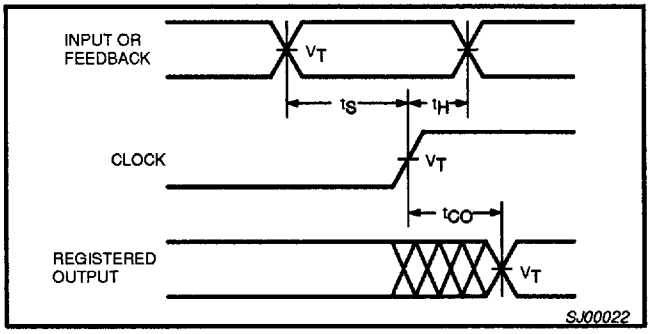
SWITCHING WAVEFORMS

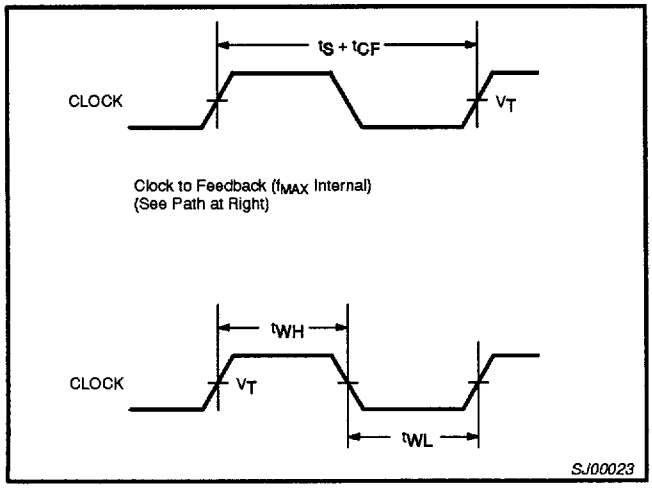
V_T = 1.5V
Input pulse amplitude 0V to 3.0V
Input rise and fall times 2.5ns max.



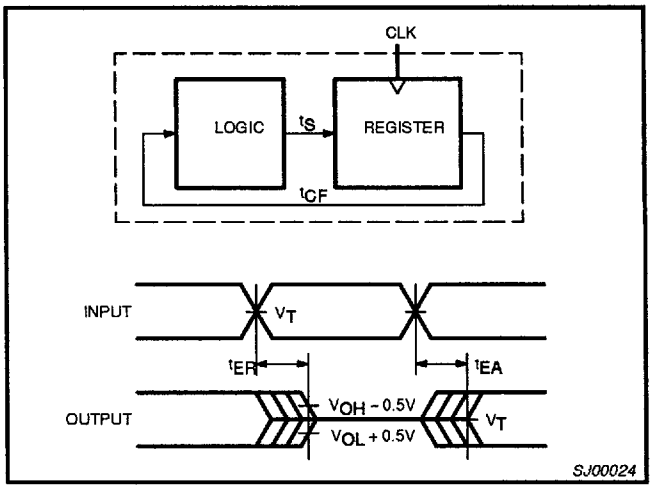
Combinatorial Output



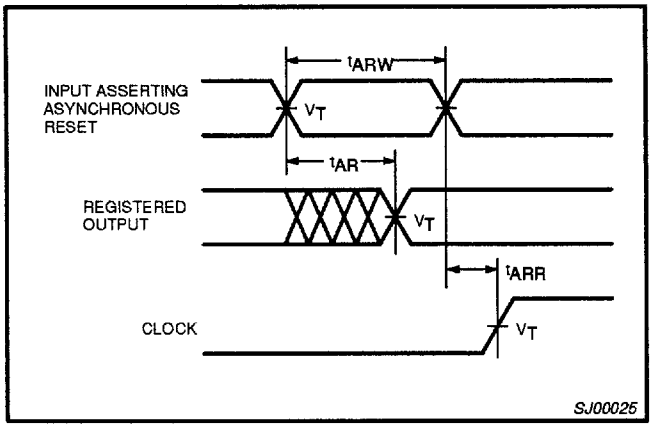
Registered Output



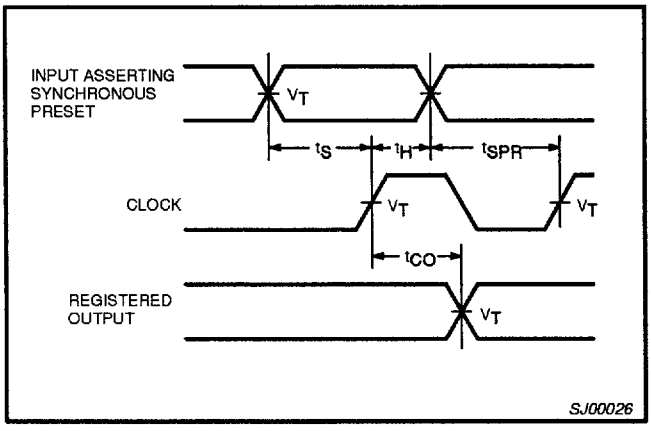
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

Programmable 3-State Outputs

Each output has a 3-State output buffer with 3-State control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macro cell output can be Active-HIGH or Active-LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "deMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the Output Macro Cell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be Active-HIGH ($S_0 = 1$).

Preset/Reset

For initialization, the ABT22V10 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW, independent of the clock.

Note that Preset and Reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Metastable Immune Flip-Flops

The D-type flip-flops have been designed such that the outputs will not glitch or display an output anomaly if the input set up or hold times are violated. Based on a τ of < 90 ps, and sampling the output 8ns after the clock edge, the typical MTBF is 170.3 years. If the sample is taken 10ns after the clock the MTBF is 5.6 trillion years.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the ABT22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10µs maximum.

Security Fuse

After programming and verification, a ABT22V10 design can be secured by programming the security fuse link. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The ABT22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies programmability and functionality of the device to provide the highest programming and post-programming functional yields.

Low Ground Bounce

The Philips Semiconductors BiCMOS QUBiC process produces exceptional noise immunity. The typical ground bounce, with 9 outputs simultaneously switching and the 10th output held low, is less than 0.8V.

Technology

The BiCMOS ABT22V10 is fabricated with the Philips Semiconductors process known as QUBiC. QUBiC combines an advanced, state-of-the-art 1.0µm (drawn feature size) CMOS process with an ultra fast bipolar process to achieve superior speed and drive capabilities. QUBiC incorporates three layers of Al/Cu interconnects for reduced chip size, and our proven Ti-W fuse technology ensures highest programming yields.

Programming

The ABT22V10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ CUPL™ and PALASM® 90 design software packages also support the ABT22V10 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Support Material)* of this data handbook for additional information.

OUTPUT REGISTER PRELOAD

The register on the ABT22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. The procedure for preloading follows:

1. Raise V_{CC} to 5.0V ± 0.25V.
2. Set Pin 2 or 3 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock Pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower Pin 2 or 3 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

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CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

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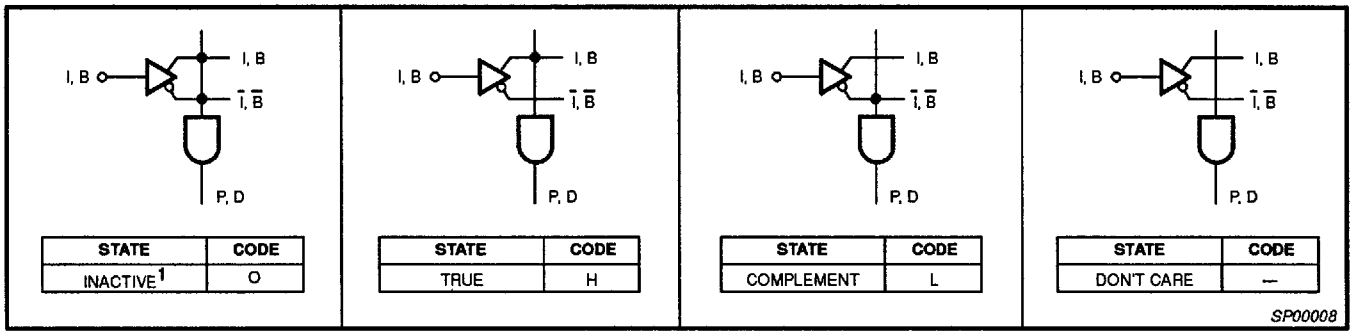
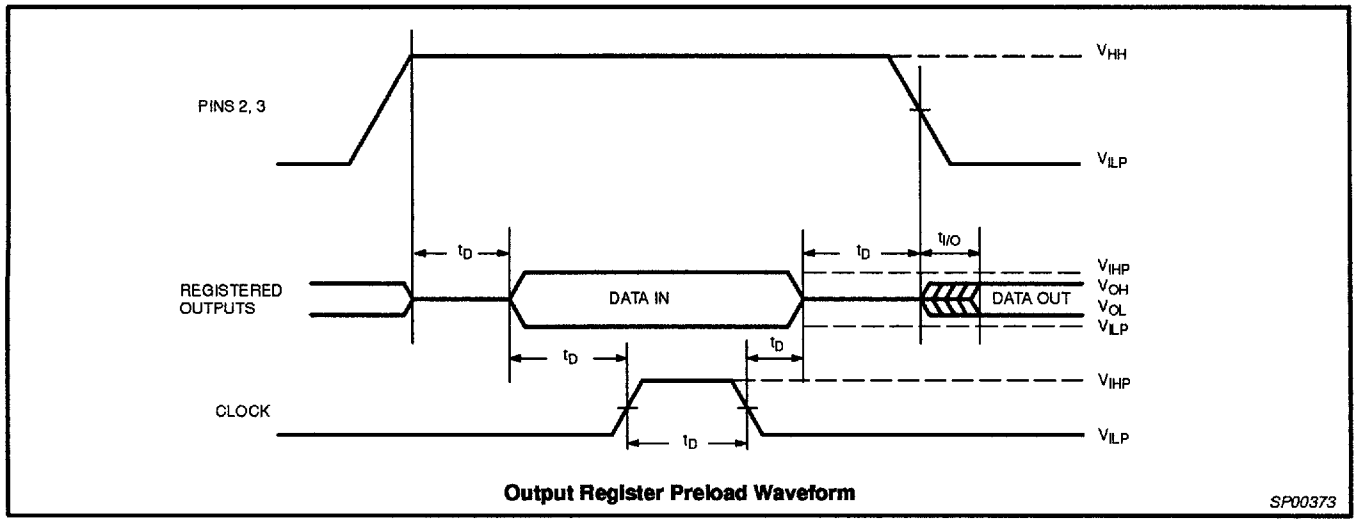
"AND" ARRAY – (I, B)

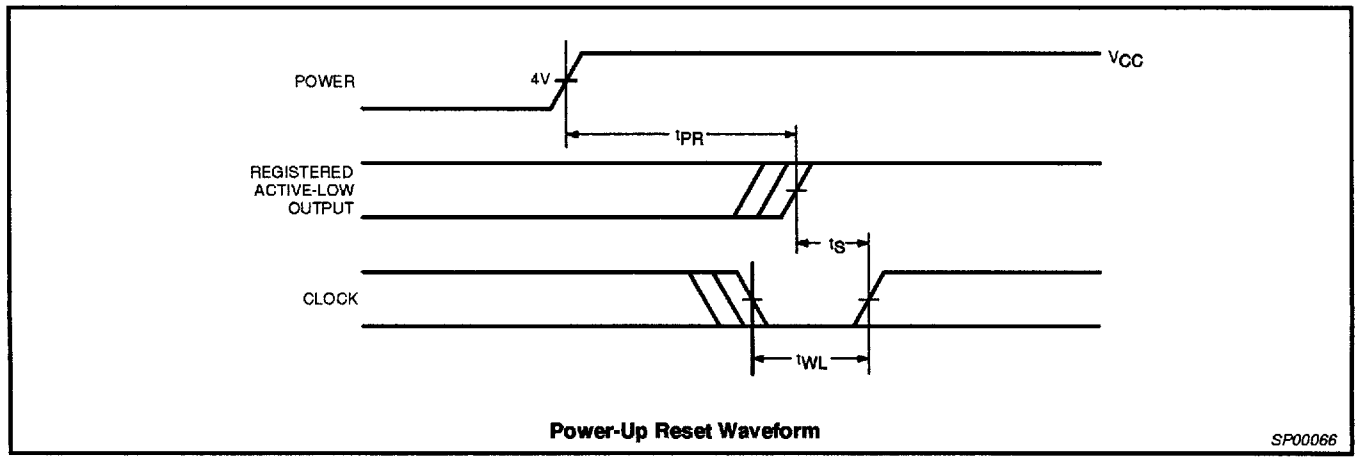


NOTE:
1. This is the initial state.

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	REC	MAX	
V_{HH}	Super-level input voltage	9.5	9.5	10	V
V_{ILP}	Low-level input voltage	0	0	0.8	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns
$t_{I/O}$	I/O valid after Pin 2 or 3 drops from V_{HH} to V_{ILP}	100			ns



Output Register Preload Waveform



Power-Up Reset Waveform

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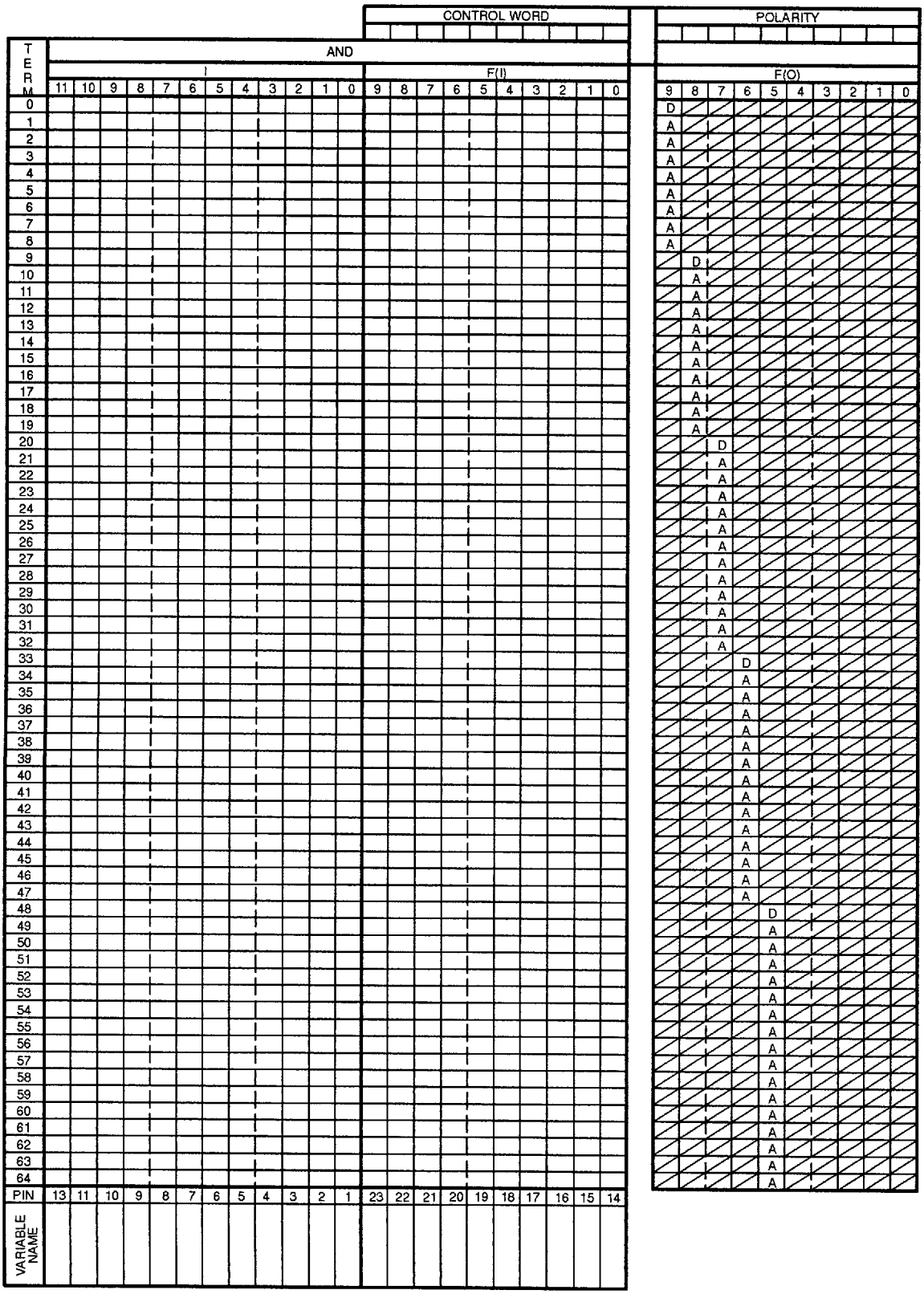
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

PROGRAM TABLE



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PROGRAM TABLE (Continued)

TERM	AND I 11	10	9	8	7	6	5	4	3	2	1	0	F(I) 9	8	7	6	5	4	3	2	1	0	F(O) 9	8	7	6	5	4	3	2	1	0
65																												D				
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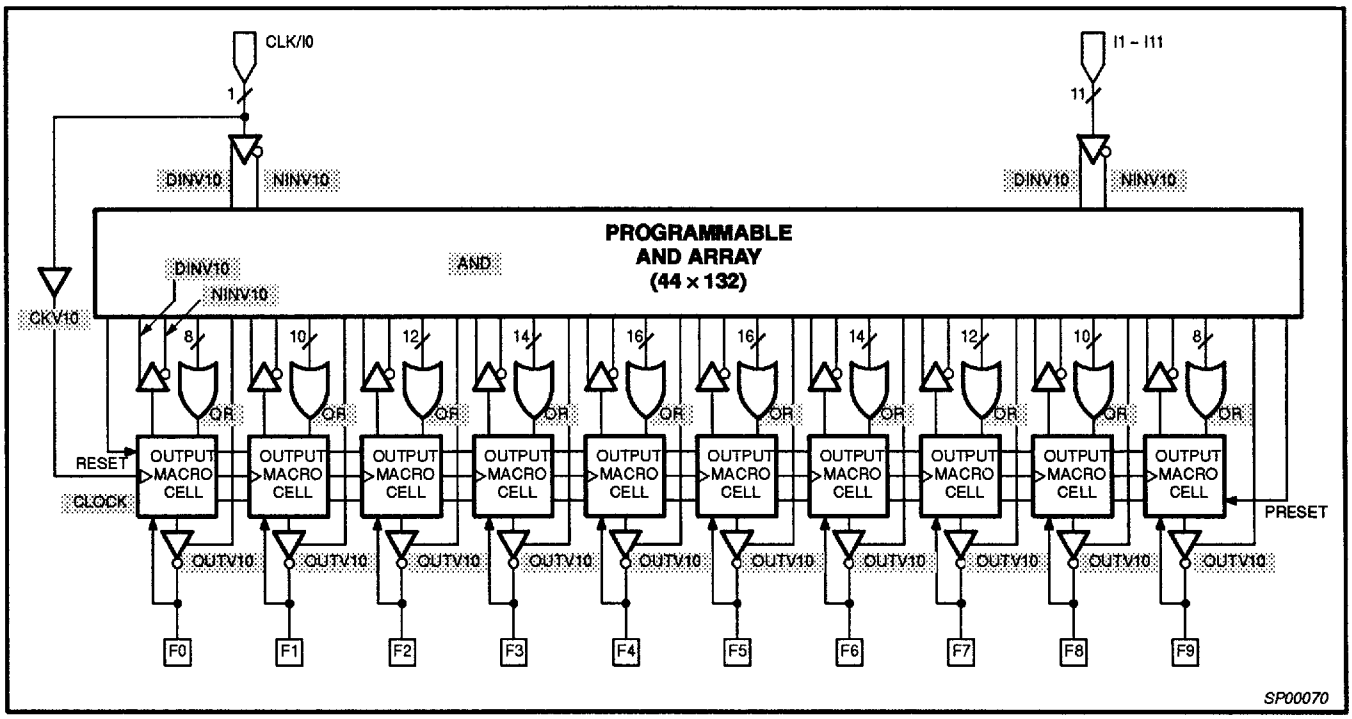
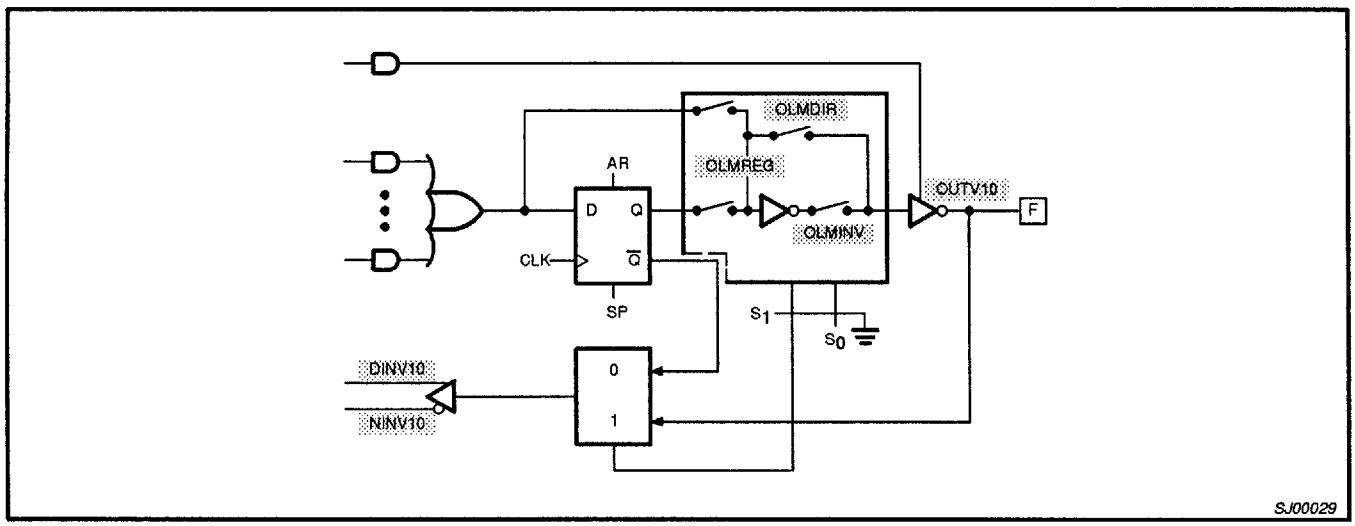
128																																A
129																																A
AR																																
SP																																
PIN	13	11	10	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	15	14										
VARIABLE NAME																																

SNAP RESOURCE SUMMARY DESIGNATIONS





Output Macro Cell