ANALOG DEVICES

8×8-Bit CMOS Multiplier

ADSP-1008A

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 8×8-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	ADSP-1008ASD/883B
−2	ADSP-1008ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-48A.

1.3 Absolute Maximum Ratings.

Supply Voltage	−0.3 V to 7 V
Input Voltage	−0.3 V to V_{DD}
Output Voltage	−0.3 V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}: see MIL-M-38510, Appendix C.

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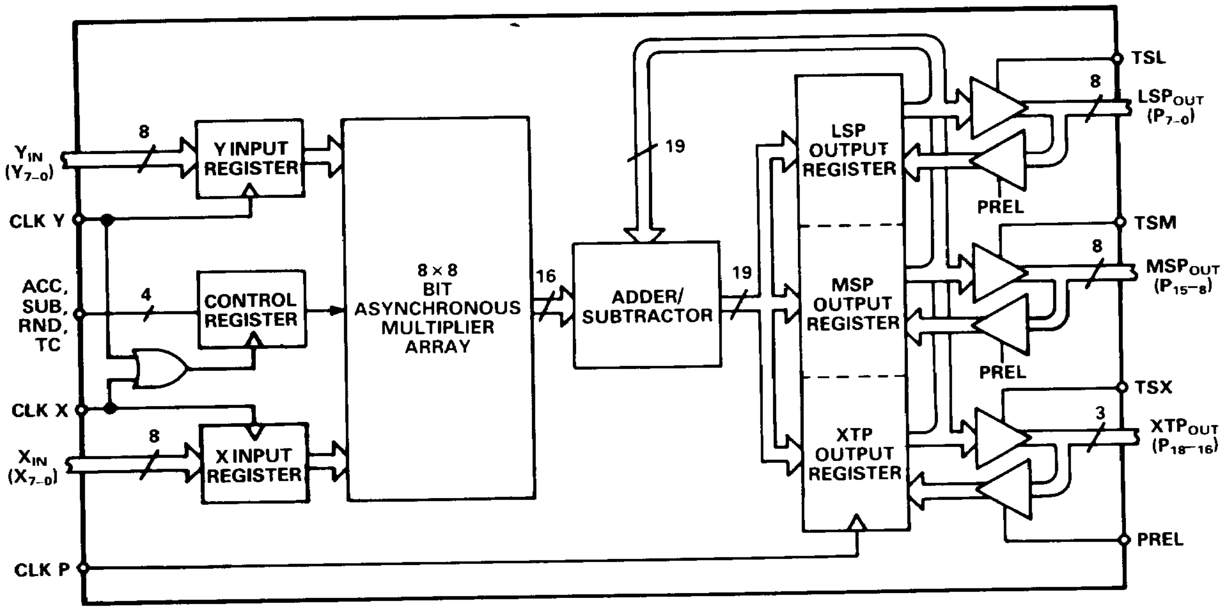
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Digital Input High Voltage	V_{IH}	−1, 2	2.0	2.0	2.0			V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	−1, 2	2.4	2.4	2.4			V_{DD} = min I_{OH} = −1 mA	V min
Digital Output Low Voltage*	V_{OL}	−1, 2	0.4	0.6	0.6			V_{DD} = min I_{OH} = +4 mA	V max
Digital Input High Current	I_{IH}	−1, 2	10	10	10			V_{DD} = max V_{IN} = +5.0 V	μA max
Digital Input Low Current	I_{IL}	−1, 2	10	10	10			V_{DD} = max V_{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I_{OZL}	−1, 2	50	50	50			V_{DD} = max V_{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I_{OZH}	−1, 2	50	50	50			V_{DD} = max V_{IH} = 0 V (High Z)	μA max
Supply Current*	I_{DD1}	−1, 2	40	55	55			V_{DD} = max; TTL Inputs; f = max	mA max
	I_{DD2}	−1, 2	25	30	30			V_{DD} = max All V_{IN} = 2.4 V	mA max
Output Delay*	t_D	−1, 2	25			35	35	Note 2	ns max
Three-State Enable* (High Z to High or Low)	t_{ENA}	−1, 2	25			35	35	Notes 2 and 3	ns max
Three-State Disable* (High or Low to High Z)	t_{DIS}	−1, 2	25			35	35	Notes 2 and 3	ns max
Clock Pulse Width*	t_{PW}	−1, 2	15			25	25	Note 2	ns min
Input Setup Time*	t_S	−1, 2	15			20	20	Note 2	ns min
Input Hold Time*	t_H	−1, 2	3			3	3	Note 2	ns min
Multiply/Accumulate Time*	t_{MAC}	−1	60			80	80	Note 2	ns max
		−2	50			65	65		

NOTES
*Indicates that a limit for this parameter has changed from REV. D.
[1]T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).
[2]TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).
[3]Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagrams and Terminal Assignments.



Pin Assignments

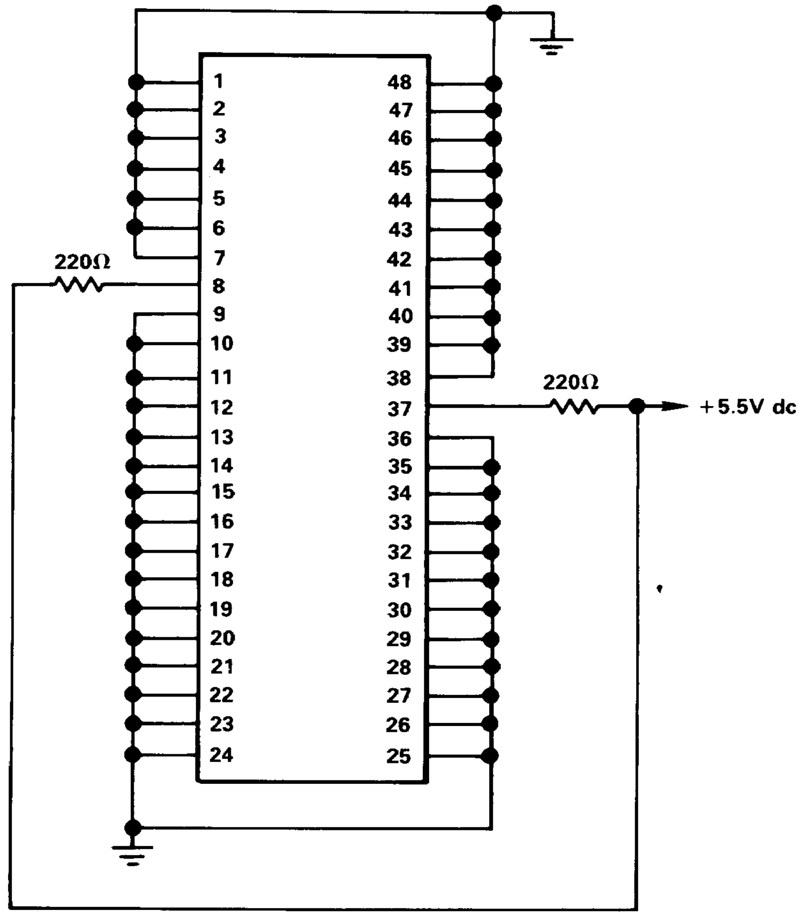
PIN	FUNCTION	PIN	FUNCTION
1	P12	25	X3
2	P11	26	X4
3	P10	27	X5
4	P9	28	X6
5	P8	29	X7
6	TSM	30	CLK X
7	CLK P	31	CLK Y
8	PREL	32	Y0
9	P7	33	Y1
10	P6	34	Y2
11	P5	35	Y3
12	GND	36	Y4
13	P4	37	V_{CC}
14	P3	38	Y5
15	P2	39	Y6
16	P1	40	Y7
17	P0	41	TC
18	TSL	42	TSX
19	SUB	43	P18
20	ACC	44	P17
21	RND	45	P16
22	X0	46	P15
23	X1	47	P14
24	X2	48	P13

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



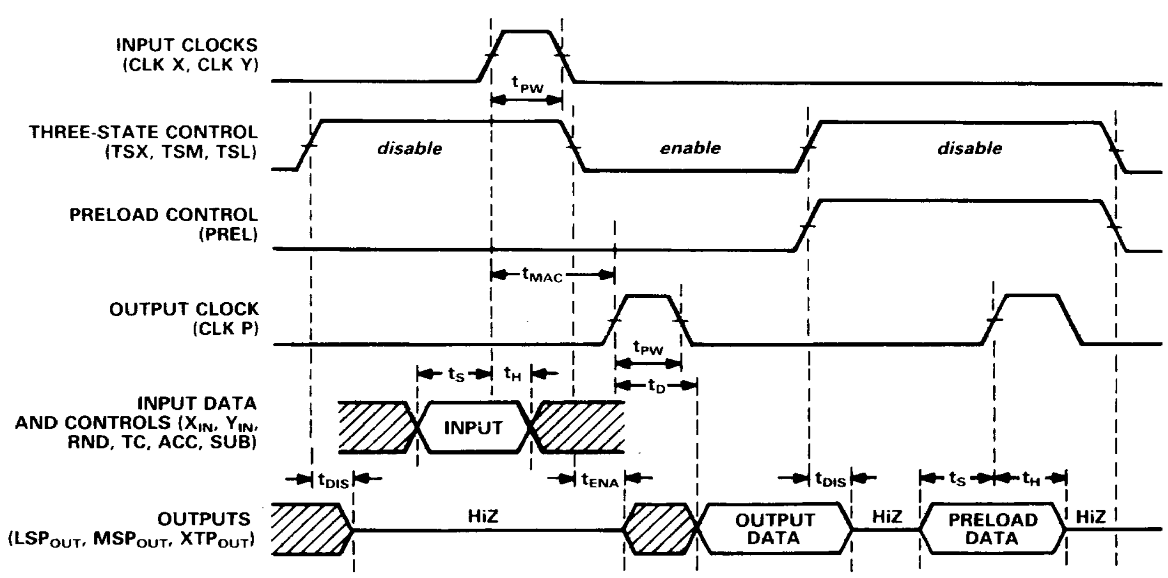


Figure 1. ADSP-1008A Timing Diagram

REV. E

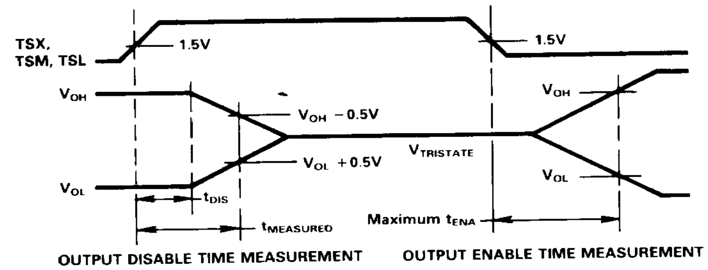


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS}, is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

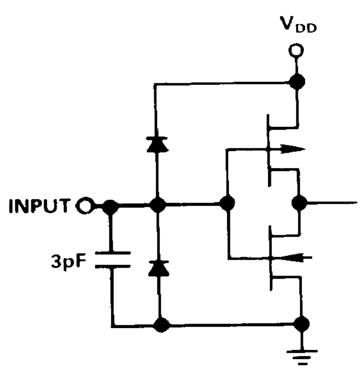


Figure 3. Equivalent Input Circuit

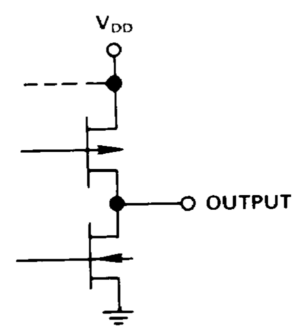


Figure 4. Equivalent Output Circuit

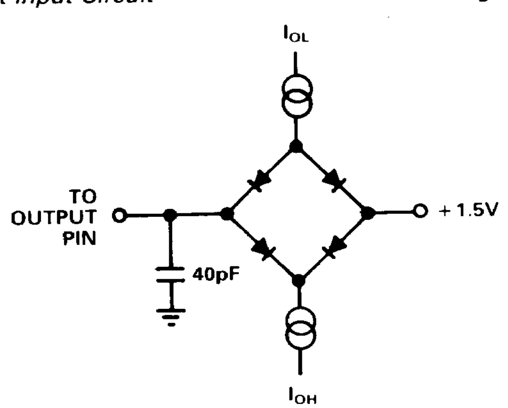


Figure 5. Normal Load Circuit for AC Measurements

ACC	SUB	Function
1	1	$Accumulator_t = X_t \cdot Y_t - Accumulator_{t-1}$
1	0	$Accumulator_t = X_t \cdot Y_t + Accumulator_{t-1}$
0	X	$Accumulator_t = X_t \cdot Y_t$

Table 2. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE:
Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
Preload = Output buffers at high impedance. Preload data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

Table 3. Preload Truth Table