Am29F200B
Known Good Die
Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **21257** Revision **D** Amendment **+4** Issue Date **June 27, 2001**

SUPPLEMENT

Am29F200B Known Good Die

2 Megabit (256 K x 8-Bit/128 K x 16-Bit) CMOS 5.0 Volt-only, Sectored Flash Memory—Die Revision 1

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% for read and write operations**
  - — Minimizes system level power requirements
- **Manufactured on 0.32 µm process technology**
  - — Compatible with 0.5 µm Am29F200A device
- **High performance**
  - — 70, 90, or 120 ns access time
- **Low power consumption**
  - — 20 mA typical active read current (byte mode)
  - — 28 mA typical active read current for (word mode)
  - — 30 mA typical program/erase current
  - — 1 µA typical standby current
- **Sector erase architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and three 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and three 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write/erase cycles guaranteed**
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash
  - — Superior inadvertent write protection
- **Data# Polling and Toggle Bit**
  - — Detects program or erase cycle completion
- **Ready/Busy# output (RY/BY#)**
  - — Hardware method for detection of program or erase cycle completion
- **Erase Suspend/Resume**
  - — Supports reading data from a sector not being erased
- **Hardware RESET# pin**
  - — Resets internal state machine to the reading array data
- **20-year data retention at 125°C**
- **Tested to datasheet specifications at temperature**
  - — Contact AMD for higher temperature range devices
- **Quality and reliability levels equivalent to standard packaged components**
- **Shipped in waffle pack, surftape, and unsawn wafer**
- **500 µm die/wafer thickness**

Publication# **21257** Rev: **D** Amendment/**+4**
Issue Date: **June 27, 2001**

GENERAL DESCRIPTION

The Am29F200B in Known Good Die (KGD) form is a 2 Mbit, 5.0 Volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29F200B Features

The Am29F200B is organized as 262,144 bytes of 8 bits each or 131,072 words of 16 bits each. The 8-bit data appears on DQ0-DQ7; the 16-bit data appears on DQ0-DQ15. This device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations.

The standard Am29F200B in KGD form offers an access time of 70, 90, or 120 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#), and output enable (OE#) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6/DQ2 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

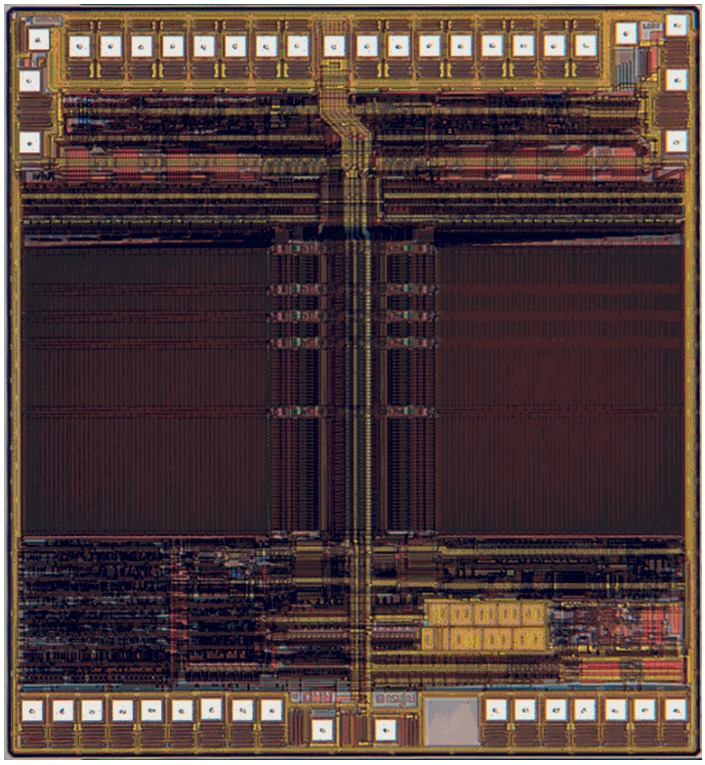
Electrical Specifications

Refer to the Am29F200B data sheet, publication number 21526, for full electrical specifications on the Am29F200B.

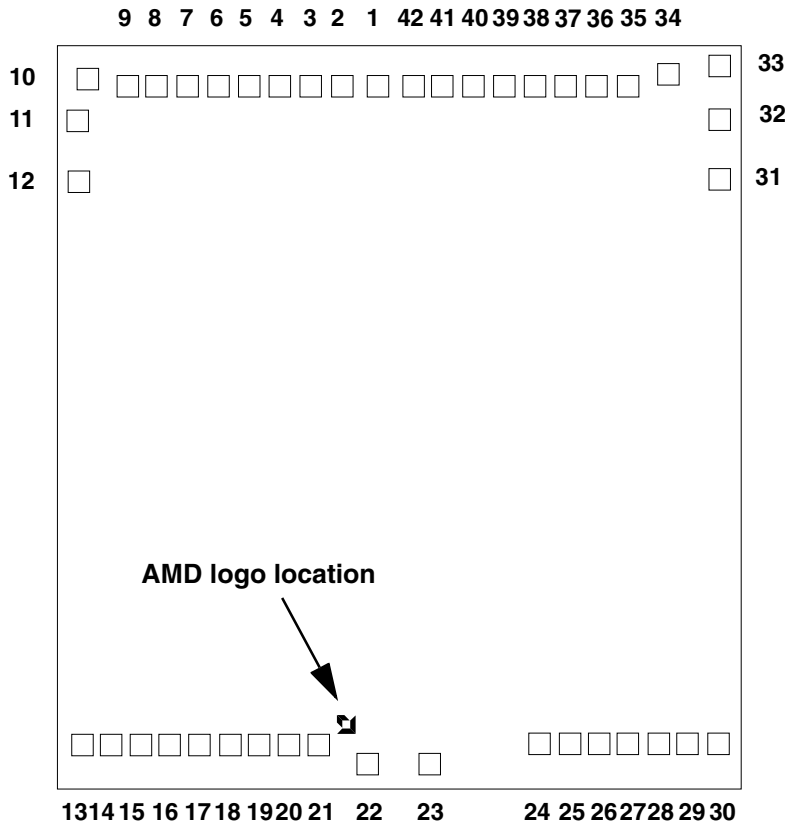
PRODUCT SELECTOR GUIDE

Family Part Number	**Am29F200B KGD**		
Speed Option (V_{CC} = 5.0 V ± 10%)	**-75** (V_{CC} = 5.0 V ± 5%)	**-90**	**-120**
Max access time, ns (t_{ACC})	70	90	120
Max CE# access time, ns (t_{CE})	70	90	120
Max OE# access time, ns (t_{OE})	30	35	50

DIE PHOTOGRAPH



DIE PAD LOCATIONS



PAD DESCRIPTION

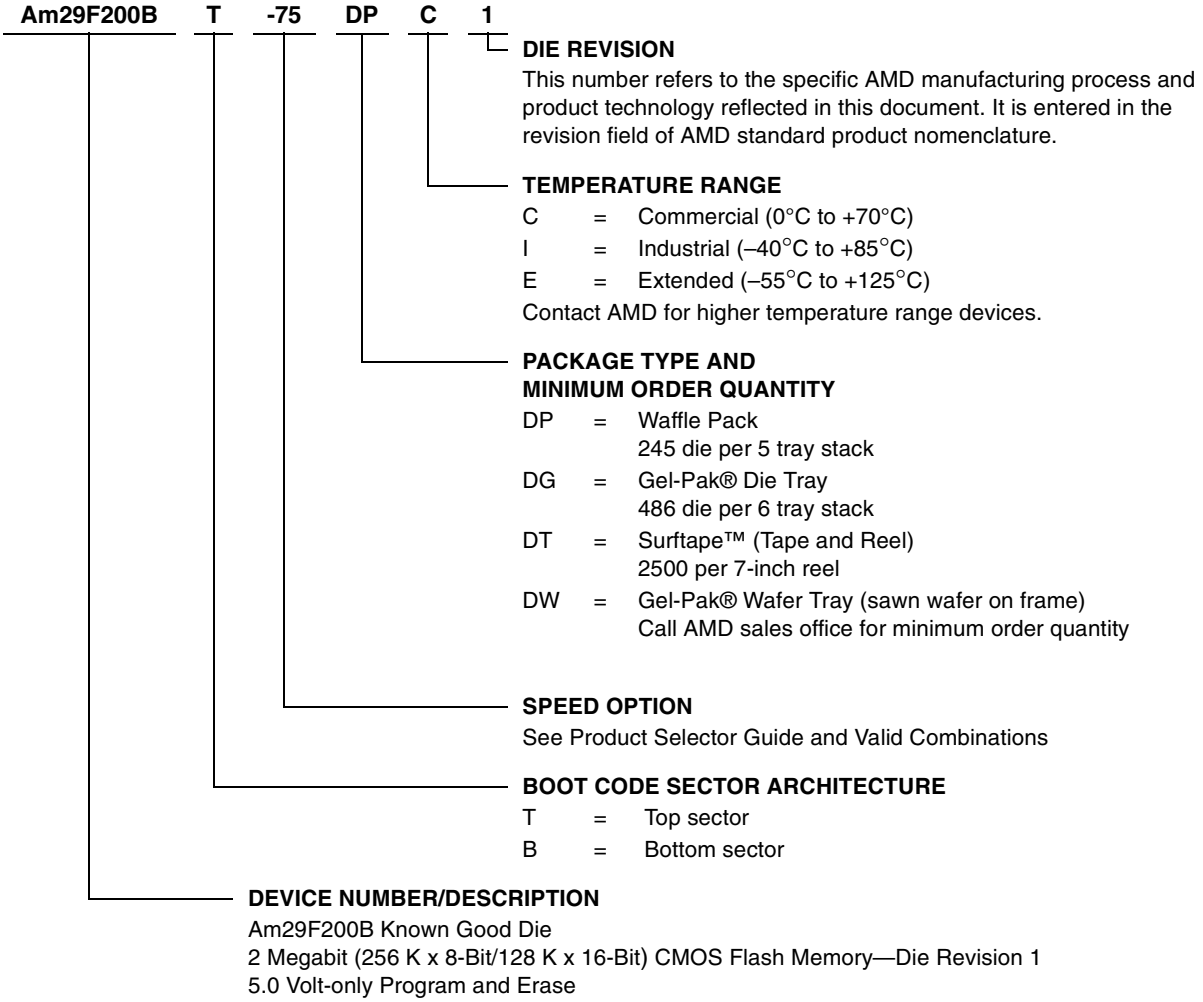
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.00	0.00	0.0000	0.0000
2	DQ4	–6.80	0.00	–0.1727	0.0000
3	DQ12	–12.80	0.00	–0.3251	0.0000
4	DQ5	–18.60	0.00	–0.4724	0.0000
5	DQ13	–24.50	0.00	–0.6223	0.0000
6	DQ6	–30.30	0.00	–0.7696	0.0000
7	DQ14	–36.30	0.00	–0.9220	0.0000
8	DQ7	–42.10	0.00	–1.0693	0.0000
9	DQ15/A-1	–48.00	0.00	–1.2192	0.0000
10	V_{SS}	–55.70	1.40	–1.4148	0.0356
11	BYTE#	–57.50	–6.50	–1.4605	–0.1651
12	A16	–57.50	–18.00	–1.4605	–0.4572
13	A15	–57.10	–124.90	–1.4503	–3.1725
14	A14	–51.30	–124.90	–1.3030	–3.1725
15	A13	–45.90	–124.90	–1.1659	–3.1725
16	A12	–40.00	–124.90	–1.0160	–3.1725
17	A11	–34.60	–124.90	–0.8788	–3.1725
18	A10	–28.80	–124.90	–0.7315	–3.1725
19	A9	–23.30	–124.60	–0.5918	–3.1648
20	A8	–17.40	–124.90	–0.4420	–3.1725
21	WE#	–12.00	–124.90	–0.3048	–3.1725
22	RESET#	–2.40	–128.60	–0.0610	–3.2664
23	RY/BY#	9.50	–128.60	0.2413	–3.2664
24	A7	30.30	–124.90	0.7696	–3.1725
25	A6	35.80	–124.90	0.9093	–3.1725
26	A5	41.60	–124.90	1.0566	–3.1725
27	A4	47.00	–124.90	1.1938	–3.1725
28	A3	52.90	–124.90	1.3437	–3.1725
29	A2	58.30	–124.90	1.4808	–3.1725
30	A1	64.10	–124.90	1.6281	–3.1725
31	A0	64.50	–18.00	1.6383	–0.4572
32	CE#	64.50	–6.50	1.6383	–0.1651
33	V_{SS}	64.50	3.80	1.6383	0.0965
34	OE#	55.00	2.30	1.3970	0.0584
35	DQ0	47.40	0.00	1.2040	0.0000
36	DQ8	41.50	0.00	1.0541	0.0000
37	DQ1	35.60	0.00	0.9042	0.0000
38	DQ9	29.70	0.00	0.7544	0.0000
39	DQ2	23.90	0.00	0.6071	0.0000
40	DQ10	18.00	0.00	0.4572	0.0000
41	DQ3	12.10	0.00	0.3073	0.0000
42	DQ11	6.20	0.00	0.1575	0.0000

Note: *The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



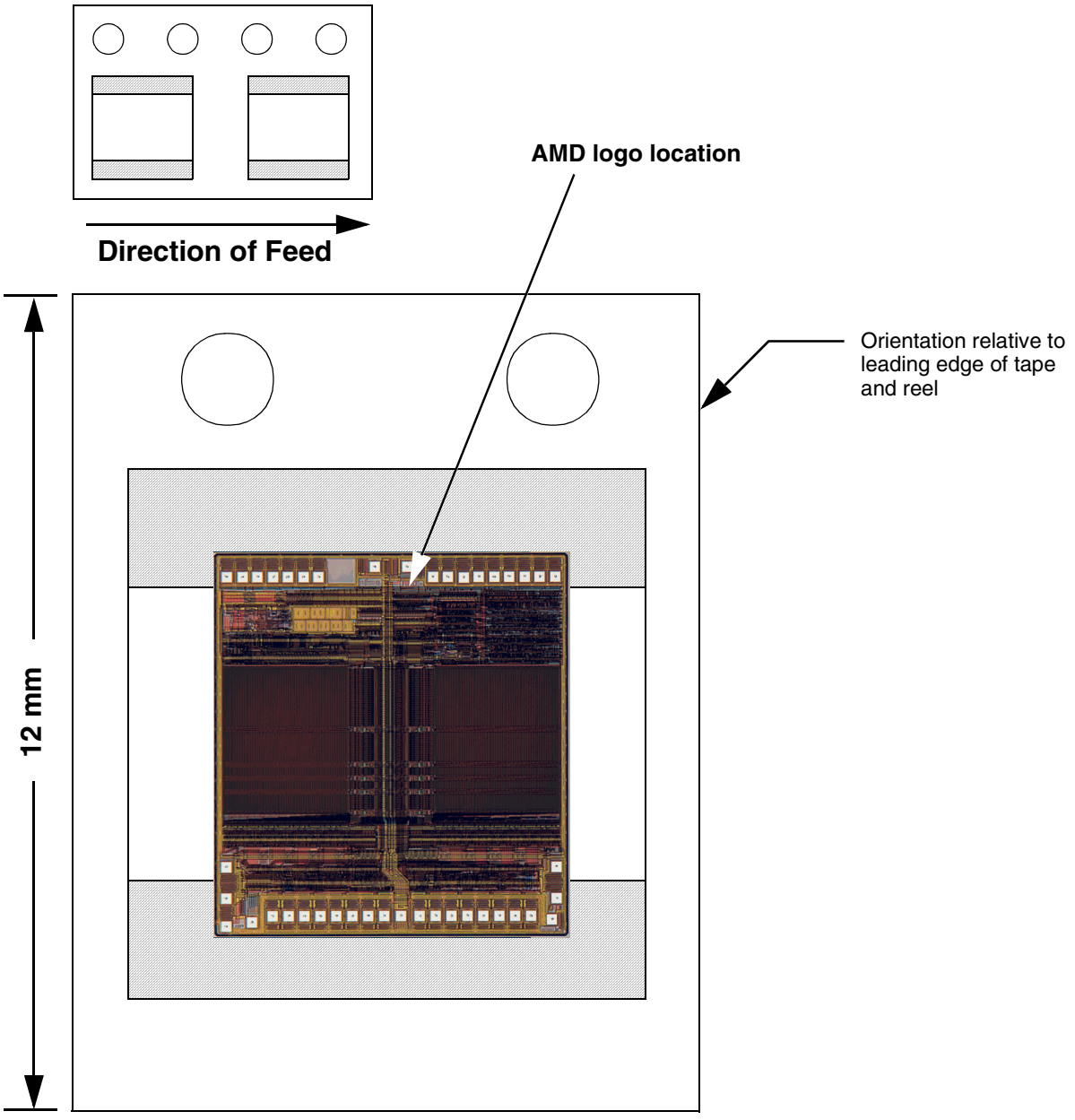
Valid Combinations	
AM29F200BT-75, AM29F200BB-75 (70 ns, V_{CC} = 5.0 V ±5%)	DPC 1, DPI 1, DPE 1, DGC 1, DGI 1, DGE 1, DTC 1, DTI 1, DTE 1, DWC 1, DWI 1, DWE 1
AM29F200BT-90, AM29F200BB-90	
AM29F200BT-120, AM29F200BB-120	

Valid Combinations

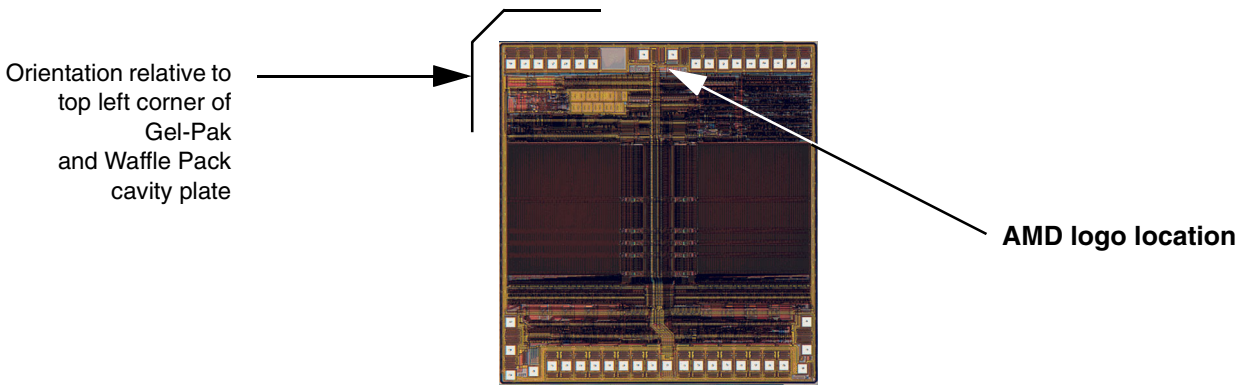
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PACKAGING INFORMATION

Surftape Packaging



Gel-Pak and Waffle Pack Packaging



PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29F200B product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test flow. In addition, an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.

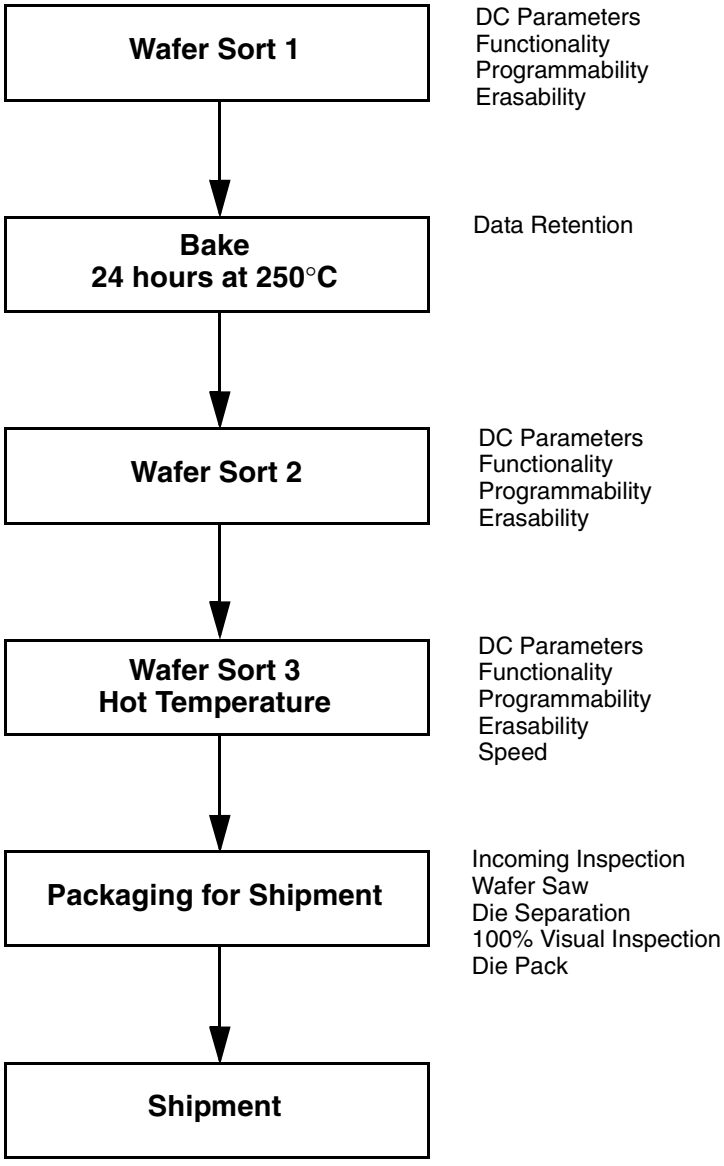


Figure 1. AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

Die dimensions . . . . . 135 mils x 150 mils
. . . . . 3.43 mm x 3.81 mm

Die Thickness . . . . . 19.7 mils
. . . . . 500 µm

Bond Pad Size . . . . . 4.69 mils x 4.69 mils
. . . . . 115.9 µm x 115.9 µm

Pad Area Free of Passivation . . . . . 13.99 mils^2
. . . . . $9{,}025 \ \mu m^2$

Pads Per Die 42

Bond Pad Metalization . . . . . Al/Cu

Die Backside . . . . . No metal, may be grounded (optional)

Passivation . . . . . Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . . 4.5 V to 5.5 V

Junction Temperature Under Bias:
Commercial, Industrial, and
Extended Temperature Range . . . . . T_J (max) = 130°C

Operating Temperature
- Commercial . . . . . 0°C to +70°C
- Industrial . . . . . –40°C to +85°C
- Extended . . . . . –55°C to +125°C

Contact AMD for higher temperature range devices.

MANUFACTURING INFORMATION

Manufacturing . . . . . FASL

Test . . . . . Sunnyvale, CA, USA, and Penang, Malaysia

Manufacturing ID (Top Boot) 98480AK
(Bottom Boot) 98480ABK

Preparation for Shipment . . . . . Penang, Malaysia

Fabrication Process CS39S

Die Revision 1

SPECIAL HANDLING INSTRUCTIONS

Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to unpackaged die or unpackaged wafer(s) under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

AMD warrants unpackaged die or unpackaged wafer(s) of its manufacture ("Known Good Die," "Die," or Wafer(s)) against defective materials or workmanship for a period of one (1) year from date of shipment. This warranty does not extend beyond the first purchaser of said Die or Wafer(s). Buyer assumes full responsibility to ensure compliance with the appropriate handling, assembly and processing of Known Good Die or Wafer(s) (including but not limited to proper Die preparation, Die attach, backgrinding, wire bonding and related assembly and test activities), and compliance with all guidelines set forth in AMD's specifications for Known Good Die or Wafer(s), and AMD assumes no responsibility for environmental effects on Known Good Die or Wafer(s) or for any activity of Buyer or a third party that damages the Die or Wafer(s) due to improper use, abuse, negligence, improper installation, improper backgrinding, accident, loss, damage in transit, or unauthorized repair or alteration by a person or entity other than AMD ("Warranty Exclusions").

The liability of AMD under this warranty is limited, at AMD's option, solely to repair the Die or Wafer(s), to send replacement Die or Wafer(s), or to make an appropriate credit adjustment or refund in an amount not to exceed the original purchase price actually paid for the Die or Wafer(s) returned to AMD, provided that: (a) AMD is promptly notified by Buyer in writing during the applicable warranty period of any defect or nonconformity in the Known Good Die or Wafer(s); (b) Buyer obtains authorization from AMD to return the defective Die or Wafer(s); (c) the defective Die or Wafer(s) is returned to AMD by Buyer in accordance with AMD's shipping instructions set forth below; and (d) Buyer shows to AMD's satisfaction that such alleged defect or nonconformity actually exists and was not caused by any of the above-referenced Warranty Exclusions. Buyer shall ship such defective Die or Wafer(s) to AMD via AMD's carrier, collect. Risk of loss will transfer to AMD when the defective Die or Wafer(s) is provided to AMD's carrier. If Buyer fails to adhere to these warranty returns guidelines, Buyer shall assume all risk of loss and shall pay for all freight to AMD's specified location. The aforementioned provisions do not extend the original warranty period of any Known Good Die or Wafer(s) that has either been repaired or replaced by AMD.

THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THE IMPLIED WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THE IMPLIED WARRANTY OF MERCHANTABILITY AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON AMD's PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR AMD ANY OTHER LIABILITIES. THE FOREGOING CONSTITUTES THE BUYER'S SOLE AND EXCLUSIVE REMEDY FOR THE FURNISHING OF DEFECTIVE OR NON CONFORMING KNOWN GOOD DIEOR WAFER(S) AND AMD SHALL NOT IN ANY EVENT BE LIABLE FOR INCREASED MANUFACTURING COSTS, DOWNTIME COSTS, DAMAGES RELATING TO BUYER'S PROCUREMENT OF SUBSTITUTE DIE OR WAFER(S) (i.e., "COST OF COVER"), LOSS OF PROFITS, REVENUES OR GOODWILL, LOSS OF USE OF OR DAMAGE TO ANY ASSOCIATED EQUIPMENT, OR ANY OTHER INDIRECT, INCIDENTAL, SPECIAL OR CONSEQUENTIAL DAMAGES BY REASON OF THE FACT THAT SUCH KNOWN GOOD DIE OR WAFER(S) SHALL HAVE BEEN DETERMINED TO BE DEFECTIVE OR NON CONFORMING.

Buyer agrees that it will make no warranty representations to its customers which exceed those given by AMD to Buyer unless and until Buyer shall agree to indemnify AMD in writing for any claims which exceed AMD's warranty.

REVISION SUMMARY

Revision A (1997)

Initial release.

Revision B (December 1997)

Formatted for 1998 flash data book.

Revision C (November 1998)

Global

Formatted to match current template. Modified Am29F200A data sheet for CS39S process technology.

Terms and Conditions

Replaced warranty with new version.

Revision D (December 1998)

Global

Added -75 speed option.

Ordering Information

Changed Gel-Pak quantity to 486. Corrected Surftape reel size to 7 inches.

Packaging Information

Added section. Moved orientation information from die photograph section into this section.

Revision D+1 (June 14, 1999)

Physical Specifications

Corrected bond pad dimensions and deleted Si from the bond pad metalization specification.

Revision D+2 (July 12, 1999)

Global

The device is now available in the high temperature range (–55°C to +140°C). T_J (max) for this range is +145°C.

Revision D+3 (November 17, 1999)

Global

Replaced references to high temperature ratings with a note to contact AMD for such devices.

Revision D+4 (June 27, 2001)

Manufacturing Information

Added Penang, Malaysia as a test facility (ACN2016).