

FEATURES

- Fast Access Times: 17/20/25 ns
- Two Chip Enable Controls
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Packages:
 - 32-Pin, 300-mil SOJ (Preliminary)
 - 32-Pin, 400-mil SOJ

FUNCTIONAL DESCRIPTION

The LH521007C is a high-speed 1,048,576-bit static RAM organized as 128K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enables ($\bar{E}_1$, E_2) permit Read and Write operations when active ($\bar{E}_1 = \text{LOW}$ and $E_2 = \text{HIGH}$) or place the RAM in a low-power standby mode when inactive ($\bar{E}_1 = \text{HIGH}$ or $E_2 = \text{LOW}$). Standby power drops to its lowest level when all inputs are stable and are at CMOS levels, while the chip is in standby mode.

Write cycles occur when both Chip Enables and Write Enable are active. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable control ($\bar{G}$) can prevent bus contention.

When both Chip Enables are active and $\bar{W}$ is inactive, a static Read will occur at the memory location specified by the address lines. $\bar{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

The 'L' version will retain data down to a supply voltage of 2 V. A significantly lower current can be obtained (I_{DR}) under this Data Retention condition. CMOS Standby Current (I_{SB2}) is reduced on the 'L' version with respect to the standard version for those applications needing reduced power consumption.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

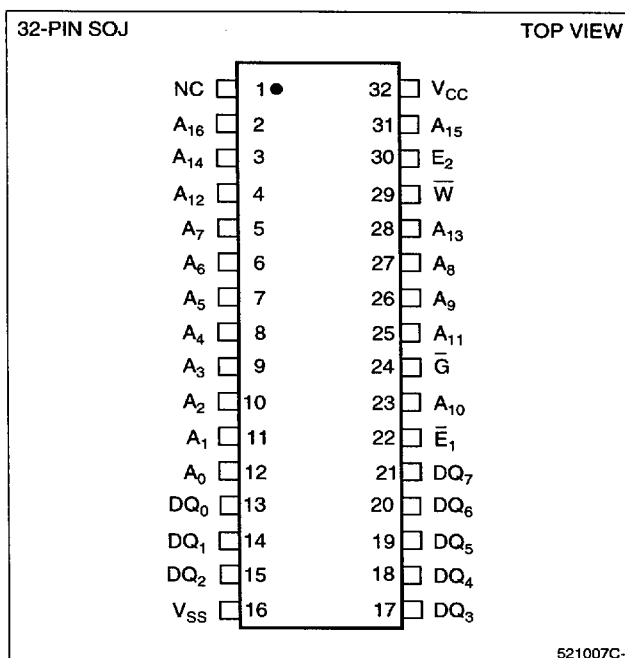


Figure 1. Pin Connections for SOJ Package

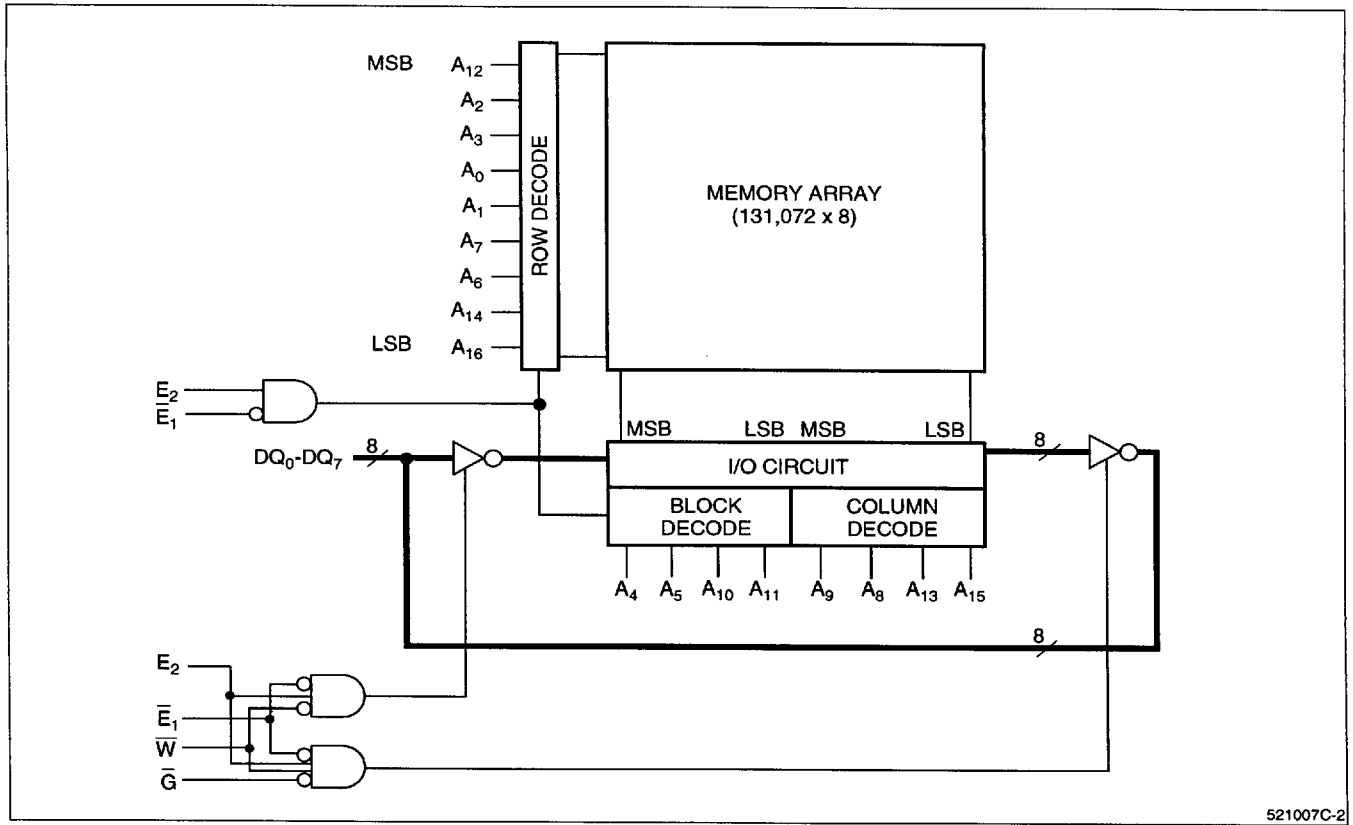


Figure 2. LH521007C Block Diagram

TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{cc}
H	X	X	X	Standby	High-Z	Standby
X	L	X	X	Standby	High-Z	Standby
L	H	H	H	Read	High-Z	Active
L	H	L	H	Read	Data Out	Active
L	H	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
A0 – A16	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
$\overline{E}_1$, E_2	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
Vcc	Positive Power Supply
Vss	Ground

ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING
V _{CC} to V _{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V _{CC} + 0.5 V
DC Output Current ²	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T _A	Temperature, Ambient	0		70	°C
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Supply Voltage	0	0	0	V
V _{IL}	Logic '0' Input Voltage ¹	−0.5		0.8	V
V _{IH}	Logic '1' Input Voltage	2.2		V _{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP ¹	MAX	UNIT
I _{CC1}	Operating Current ²	t _{CYCLE} = 17 ns		105	155	mA
I _{CC1}	Operating Current ²	t _{CYCLE} = 20 ns		95	140	mA
I _{CC1}	Operating Current ²	t _{CYCLE} = 25 ns		85	125	mA
I _{SB1}	Standby Current	$\bar{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$ t _{CYC} = 17 ns, I _{OUT} = 0			50	mA
I _{SB1}	Standby Current	$\bar{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$ t _{CYC} = 20 ns, I _{OUT} = 0			45	mA
I _{SB1}	Standby Current	$\bar{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$ t _{CYC} = 25 ns, I _{OUT} = 0			40	mA
I _{SB2}	Standby Current	$\bar{E}_1 \geq V_{CC} - 0.2$ V or $E_2 \leq 0.2$ V, t _{CYC} = 0, I _{OUT} = 0			10	mA
I _{LI}	Input Leakage Current	V _{IN} = 0 V to V _{CC}	−2		2	μA
I _{LO}	I/O Leakage Current	V _{IN} = 0 V to V _{CC}	−2		2	μA
V _{OH}	Output High Voltage	I _{OH} = −4.0 mA	2.4			V
V _{OL}	Output Low Voltage	I _{OL} = 8.0 mA			0.4	V

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.

2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

3. Preliminary Information.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE ^{1,2}

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1.Capacitances are maximum values at 25°C measured at 1.0MHz with $V_{Bias} = 0$ V and $V_{CC} = 5.0$ V.

2.Sample tested only.

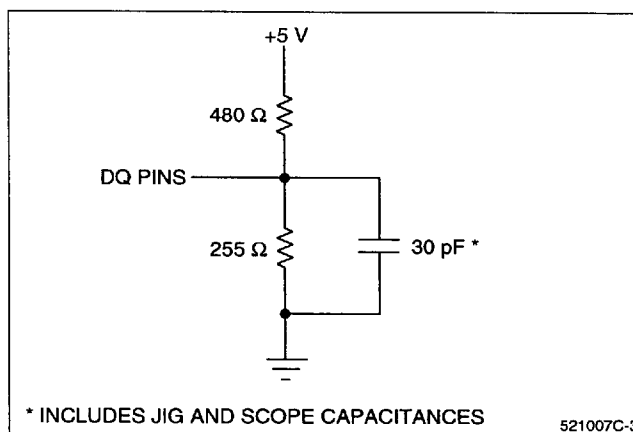


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS¹ (Over Operating Range)

SYMBOL	DESCRIPTION	-17		-20		-25		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
tRC	Read Cycle Timing	17		20		25		ns
tAA	Address Access Time		17		20		25	ns
tOH	Output Hold from Address Change	3		3		3		ns
tEA	$\overline{E}$ Low to Valid Data		17		20		25	ns
tELZ	$\overline{E}$ Low to Output Active ^{2,3}	5		5		5		ns
tEHZ	$\overline{E}$ High to Output High-Z ^{2,3}		8		8		10	ns
tGA	$\overline{G}$ Low to Valid Data		7		7		8	ns
tGLZ	$\overline{G}$ Low to Output Active ^{2,3}	0		0		0		ns
tGHZ	$\overline{G}$ High to Output High-Z ^{2,3}		6		6		10	ns
tPU	$\overline{E}$ Low to Power Up Time ⁴	0		0		0		ns
tPD	$\overline{E}$ High to Power Down Time ⁴		17		20		25	ns
WRITE CYCLE								
tWC	Write Cycle Time	17		20		25		ns
tEW	$\overline{E}$ Low to End of Write	12		12		15		ns
tAW	Address Valid to End of Write	12		12		15		ns
tAS	Address Setup	0		0		0		ns
tAH	Address Hold from End of Write	0		0		0		ns
tWP	$\overline{W}$ Pulse Width	12		12		15		ns
tDW	Input Data Setup Time	9		9		10		ns
tDH	Input Data Hold Time	0		0		0		ns
tWHZ	$\overline{W}$ Low to Output High-Z ^{2,3}	0	7	0	8	0	10	ns
tWLZ	$\overline{W}$ High to Output Active ^{2,3}	3		3		3		ns

NOTES:

1.AC Electrical Characteristics specified at 'AC Test Conditions' levels.

2.Active output to High-Z and High-Z to output active tests specified for a ± 200 mV transition from steady state levels into the test load.
C_{Load} = 5 pF.

3.Sample tested only.

4.Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ and E_2 are HIGH, $\overline{E}_1$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA} .

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}_1$ and E_2 are both active. Data Out is not specified to be valid until t_{EA} or t_{GA} , but may become valid as soon as t_{ELZ} or t_{GLZ} . Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

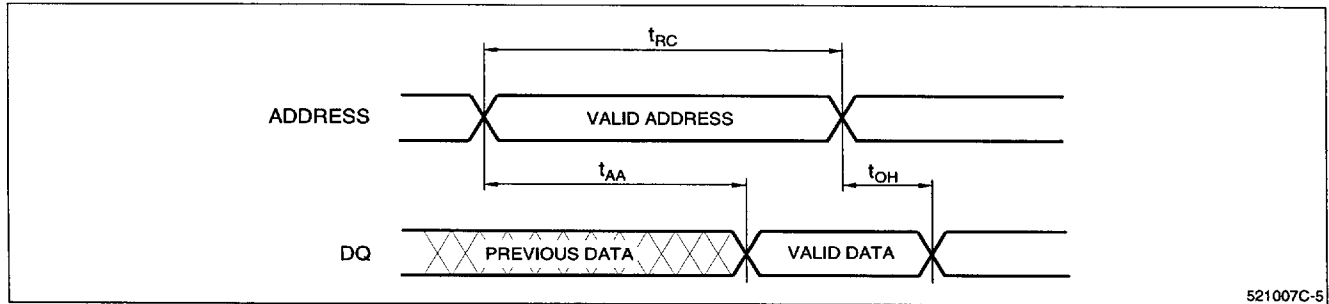


Figure 4. Read Cycle No. 1

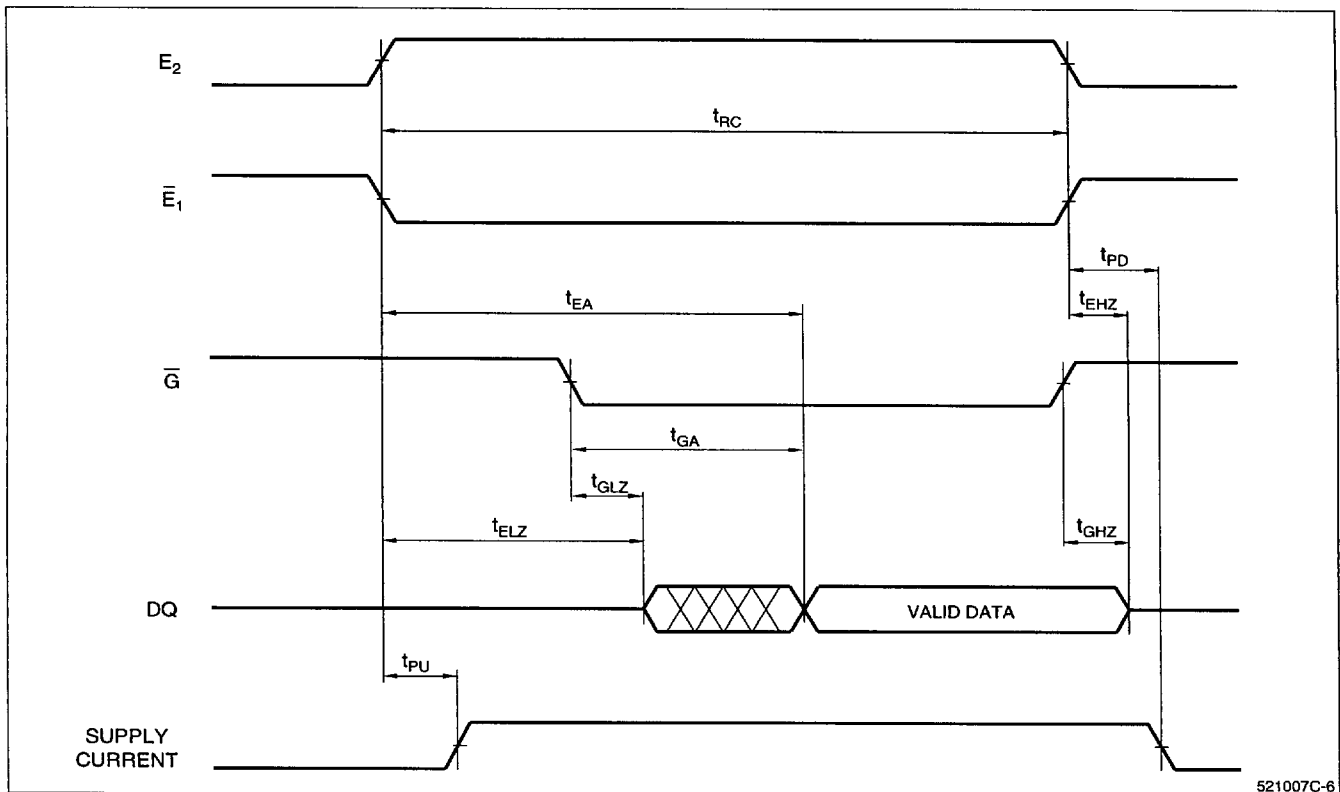


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when both $\overline{E}_1$ and E_2 are active. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}_1$ and $\overline{G}$ are LOW, E_2 is HIGH. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

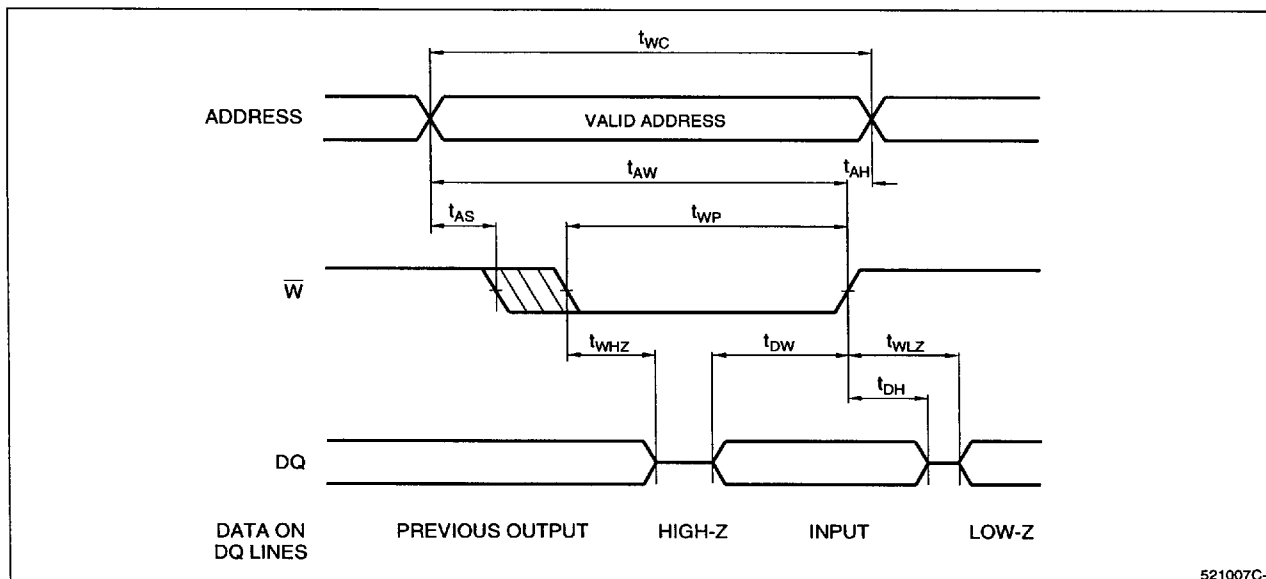


Figure 6. Write Cycle No. 1

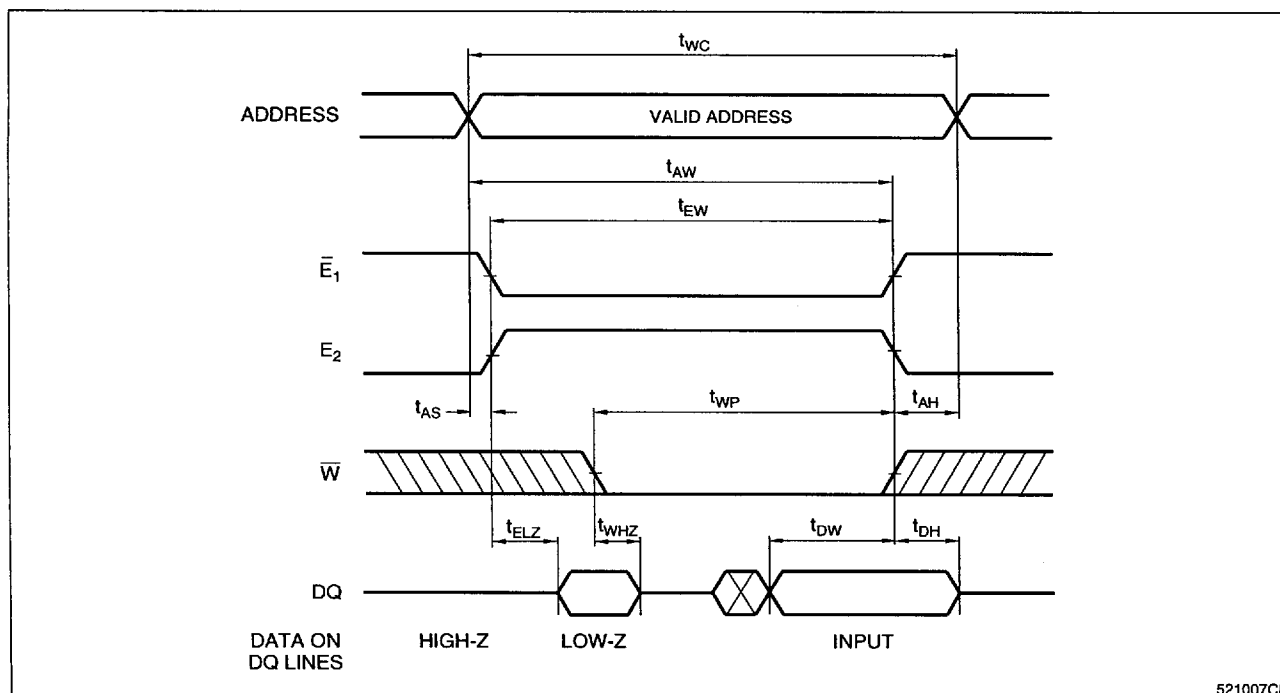
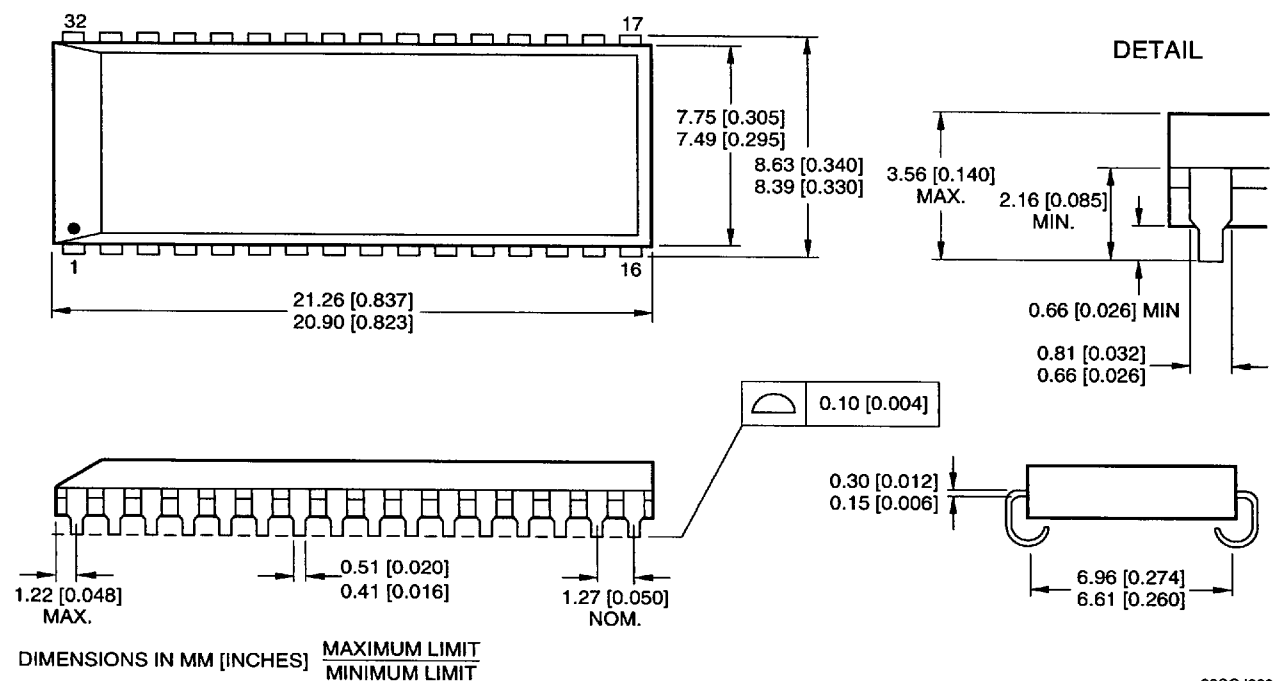


Figure 7. Write Cycle No. 2

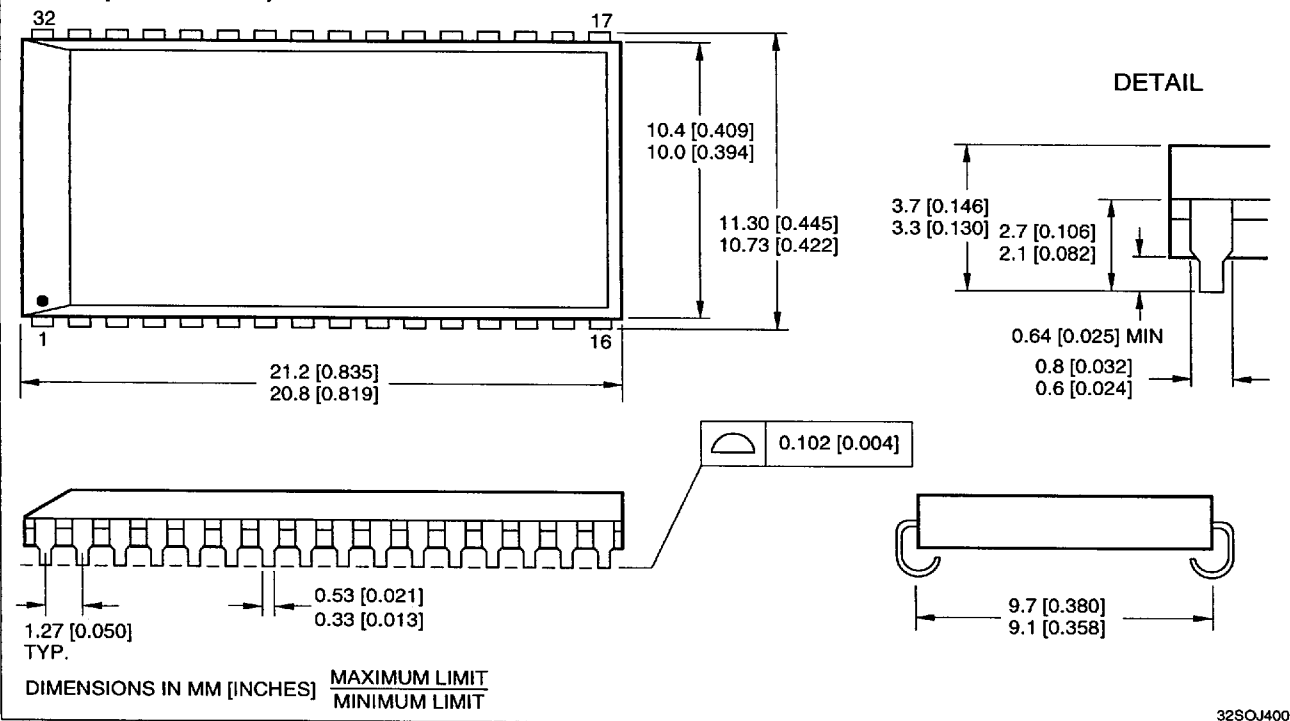
PACKAGE DIAGRAMS

32SOJ (SOJ32-P-300-SPL)



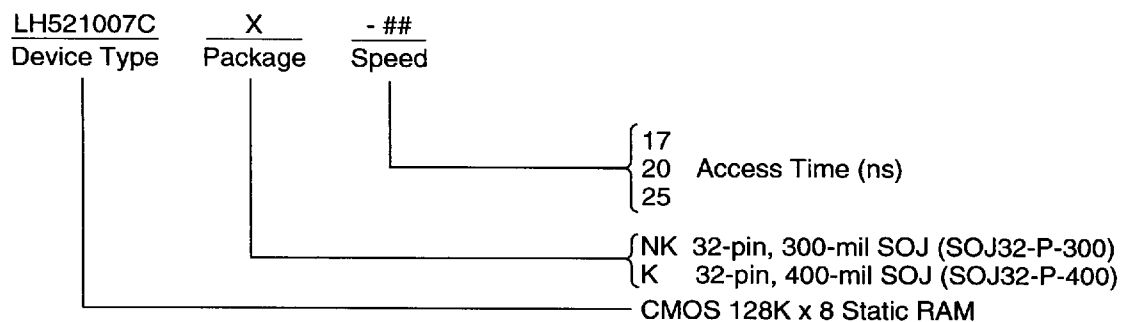
32-pin, 300-mil SOJ

32SOJ (SOJ32-P-400)



32-pin, 400-mil SOJ

ORDERING INFORMATION



Example: LH521007CK-25 (CMOS 128K x 8 Static RAM, 25 ns, 32-pin, 400-mil SOJ)

521007C-9

Sharp Microelectronics Technology, Inc.

RELIABILITY TEST REPORT

For Surface Mount Packaging

Device	LH521007CK - 128Kx8 SRAM	Report Date	September, 1995	Rev.	1
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Technology	0.85μm	Package	32p, 300 or 400 mil SOJ
Wafer Fab	TSMC, Taiwan	Die Coat	wafer-level polyimide
Assembly	Amkor, Korea, or SPIL, Taiwan	Resin	EME9300H
		Lead Frame	copper

Test	Conditions	Sample	Duration	Results	Comments
Life Test	125°C, 5.5V, dynamic	153	1000 Hrs.	0/152 @2K hrs.	FIT Rate = 67 FITs Ea = 0.5eV, Derated 55°C, 60% C.L.
ESD	1000V, Human Body Model, Method 3015.7	10	--	0/10 @ 2800V	
ESD	250V, Machine Model, EIAJ standard	12	--	0/12 @ 250V	
Latch-Up	150mA, Current Forcing, JEDEC JC40.2	8	--	0/8 @150mA	
Latch-Up	10V, Voltage Forcing, JEDEC JC40.2	8	--	0/8 @10V	
Latch-Up	10V, Vcc Bump, JEDEC JC40.2	8	--	0/8 @10V	
85/85	85°C, 85% R.H., static	74	1000 Hrs.	0/74	
Pressure Cooker	121°C, 100% R.H., 2 Atm.	45	300 Hrs.	0/45	
Temperature Cycling	-65°C~+150°C Air-to-Air	45	300 Cyc.	0/45	
Thermal Shock	-65°C~+150°C Liquid-to-Liquid	45	300 Cyc.	0/45	
High Temp. Storage	+150°C, no bias	11	1000 Hrs.	0/11	
Low Temp. Storage	-65°C, no bias	11	1000 Hrs.	0/11	
Solderability	230°C, after pre-conditioning	11	5 Sec.	0/11	
Resistance to Solder Heat	260°C immersion	11	10 Sec.	0/11	
Mechanical Shock	1500G, ±3 axes	11	15mS, net	0/11	
Variable Freq. Vibration	20g, 100~2000Hz, ±3 axes	11	48 Min., Total	0/11	
Dry Pack	4 sequences with pre-conditioning	44	--	0/44	
Mark Permanency	3 solutions, 1 solution/group	9	--	0/9	

Comments:

1. The LH521002CK (256Kx4) and this device are bond-out options of the same die. The ESD testing reported here was performed on units with the x4 bond-out option.

FRCRE002.00