LSI LOGIC

LR33300 and LR33310 Enhanced Self-Embedding™ Processors User's Manual Addendum

Addendum Number A000379

Order Number for Manual J14028

Introduction

This addendum to the *LR33300 and LR33310 Self-Embedding™ Processors User's Manual* specifies the LR333x0's electrical and mechanical characteristics. This addendum is divided into three sections:

The descriptions of AC timing and electrical requirements are intended for hardware designers who are judging the LR333x0's compatibility with other components. The packaging information is intended for designers who are incorporating the LR333x0 in printed-circuit-board assemblies.

All specifications are preliminary and subject to change.

AC Timing

This section describes the AC timing characteristics of the LR333x0's memory interface. The timing relationships between SYSCLK and various LR333x0 signals that comprise its memory interface are depicted in Figures 1 through 16. The figures depict:

- Clock Timing (SYSCLK) (Figure 1)
- Cold Reset Timing (Figure 2)
- Warm Reset Timing (Figure 3)
- 3-State Timing (Figure 4)

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- Read Transaction Timing (Figure 5)
- Write Transaction Timing (Figure 6)
- Block-Fetch Transaction Timing (Figure 7)
- Synchronous Bus Arbitration Timing (Figure 8)
- DRAM Read Timing (Figure 9)
- DRAM Write Timing (Figure 10)
- DRAM Block Fetch Timing (Figure 11)
- DRAM Page-Mode Write Timing (Figure 12)
- DRAM Refresh Timing (Figure 13)
- DMA Access Timing Using BGNT (Figure 14)
- DMA Access Timing Using $\overline{\text{DMAR}}$ (Figure 15)
- Timing for Miscellaneous Input and Output Signals (Figure 16)

Table 1 and Table 2 (pages 14-21) list the AC timing values for the LR33300 and LR33310, respectively. The numbers in Figures 1 through 16 refer to the timing parameters listed in column 1 of both tables. All parameters are valid for a temperature range from 0 to 50 °C for the 50 MHz LR33310 and from 0 to 70 °C for the remaining chip versions. The load is 55 pF.

Figure 1
Clock Timing
(SYSCLK)

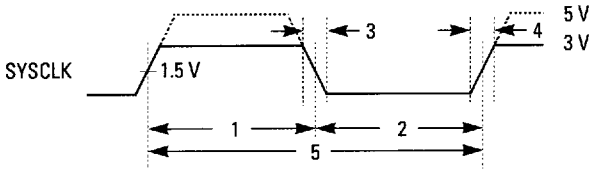


Figure 2
Cold Reset Timing

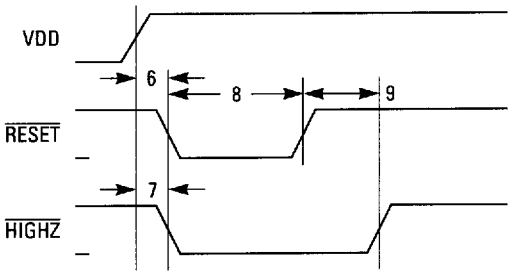
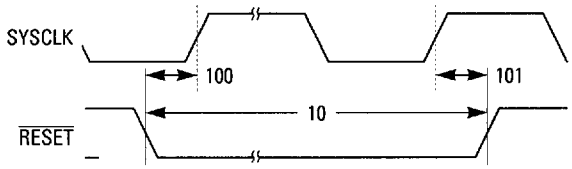
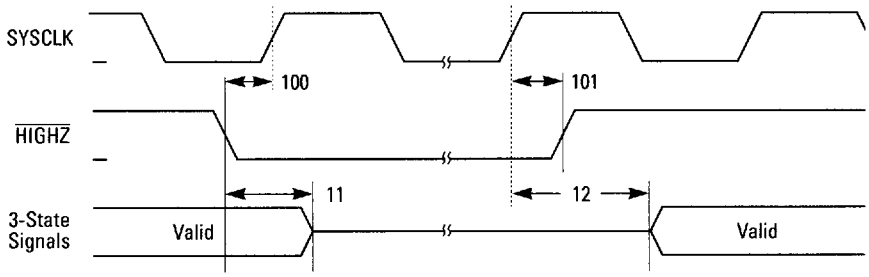


Figure 3
Warm Reset Timing



Note:
1. Parameters 100 and 101 are provided for designers who need to synchronize the LR33310's $\overline{\text{RESET}}$ or $\overline{\text{HIGHZ}}$ state with other devices. These parameters can be ignored for asynchronous applications.

Figure 4
3-State Timing



Note:
1. Parameters 100 and 101 are provided for designers who need to synchronize the LR33310's $\overline{\text{RESET}}$ or $\overline{\text{HIGHZ}}$ state with other devices. These parameters can be ignored for asynchronous applications.

Figure 5
Read Transaction Timing

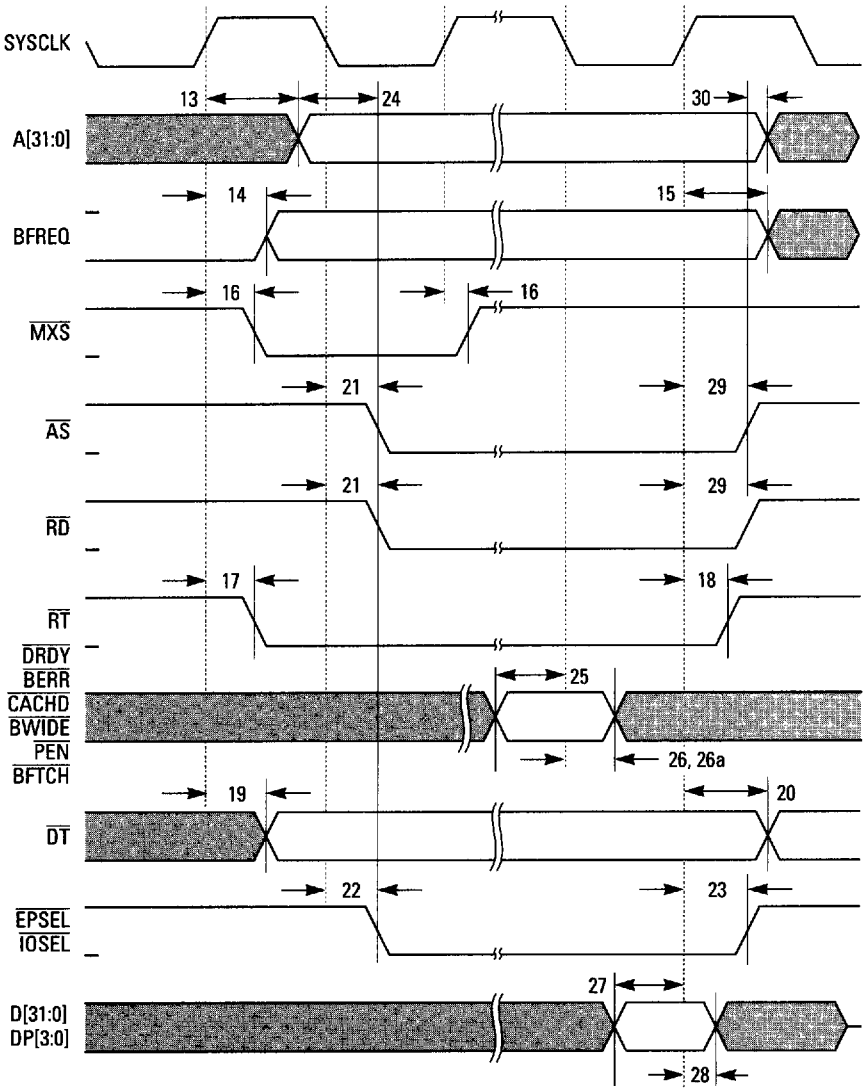


Figure 6
Write Transaction Timing

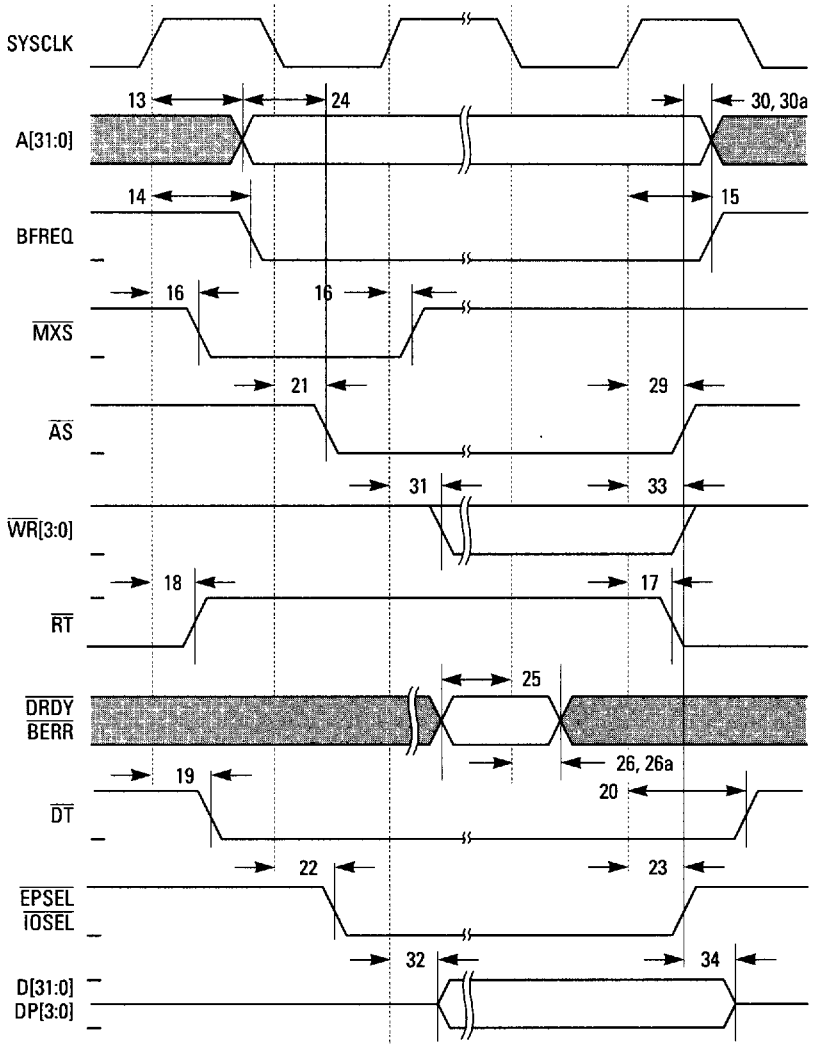
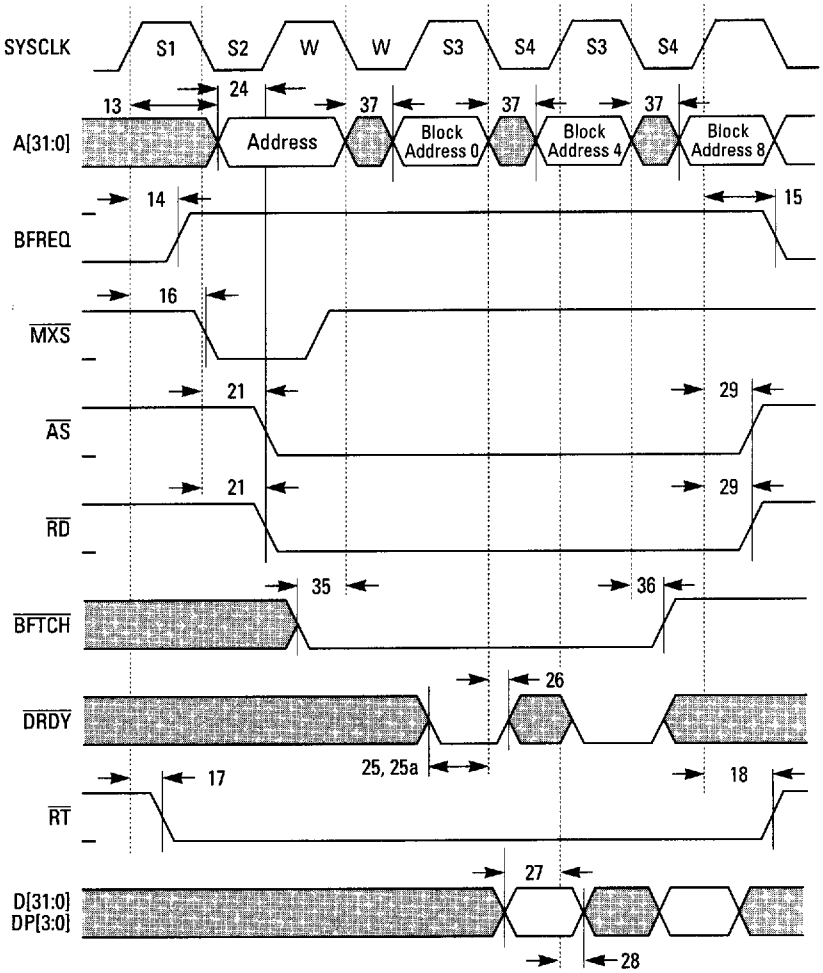


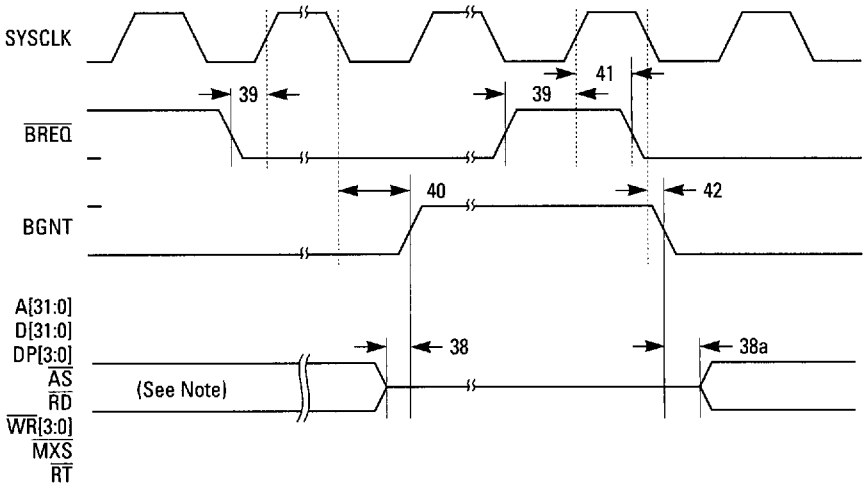
Figure 7
Block-Fetch
Transaction Timing



Note:

1. This waveform depicts a two-word block fetch. As shown in the waveform, the address increments three times for this two-word fetch. The memory system should ignore the final address in a block fetch of any length. For larger block fetches, States 3 and 4 repeat until the fetch is complete. The memory system may insert wait states in between States 4 and 3.

Figure 8
Synchronous Bus Arbitration Timing



Note:
1. AS, RD, RT, MXS, and WR[3:0] are driven inactive before 3-state.

Figure 9
DRAM Read
Timing

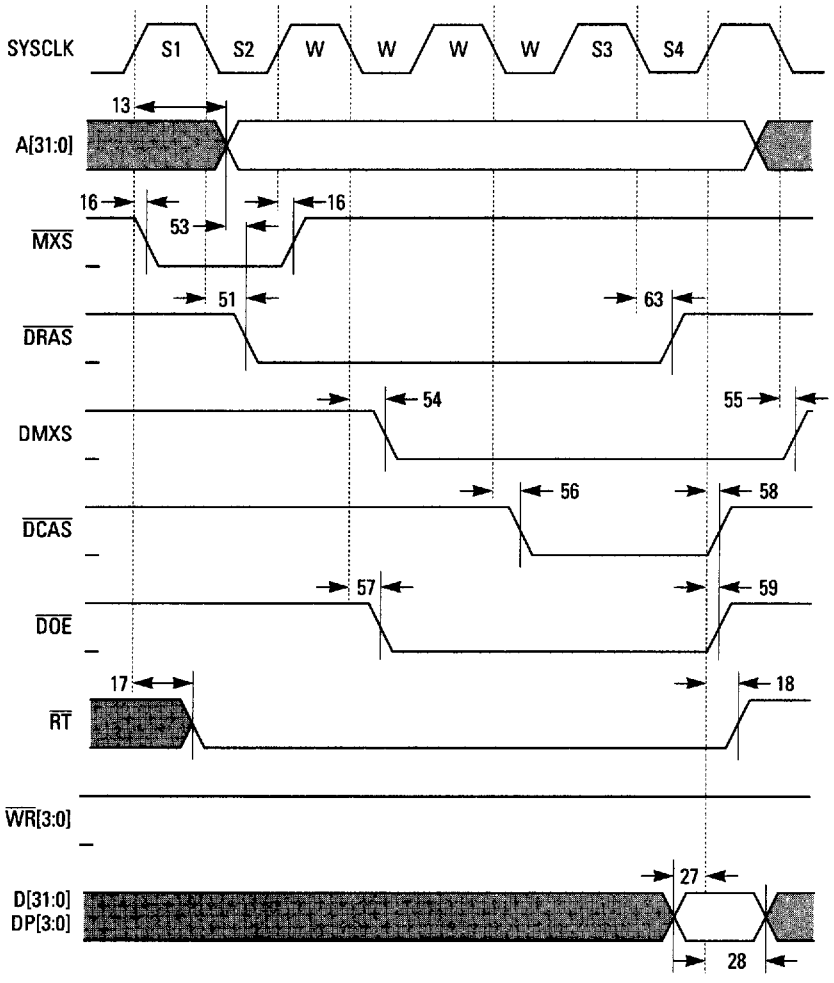


Figure 10
DRAM Write Timing

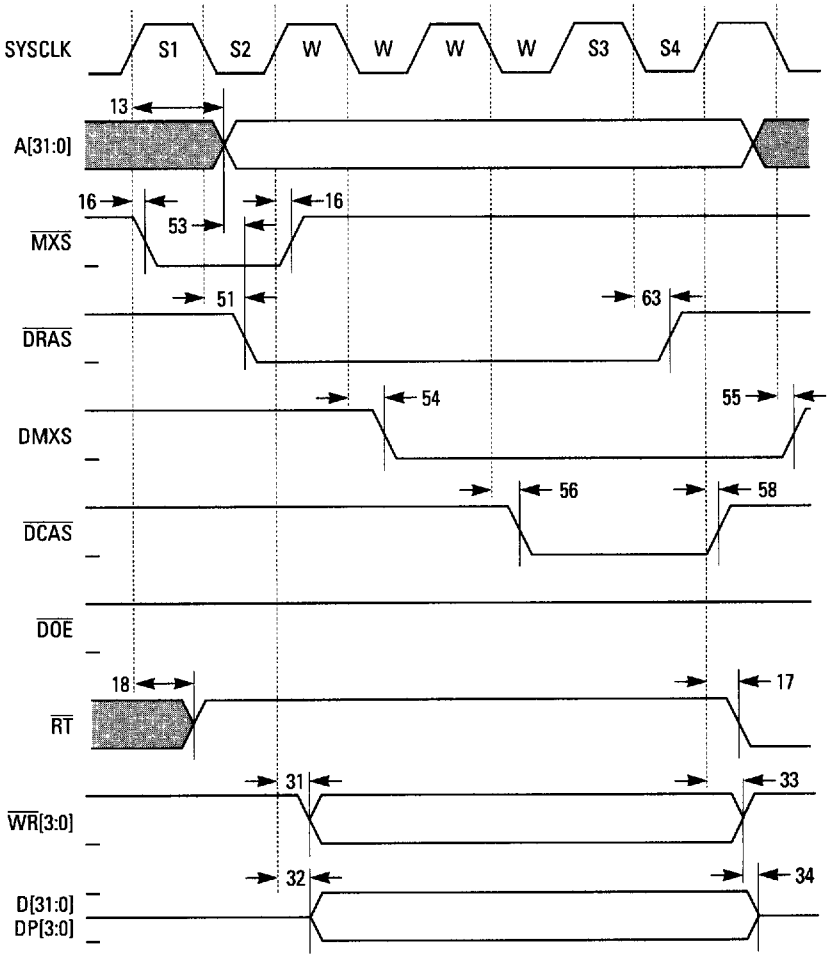
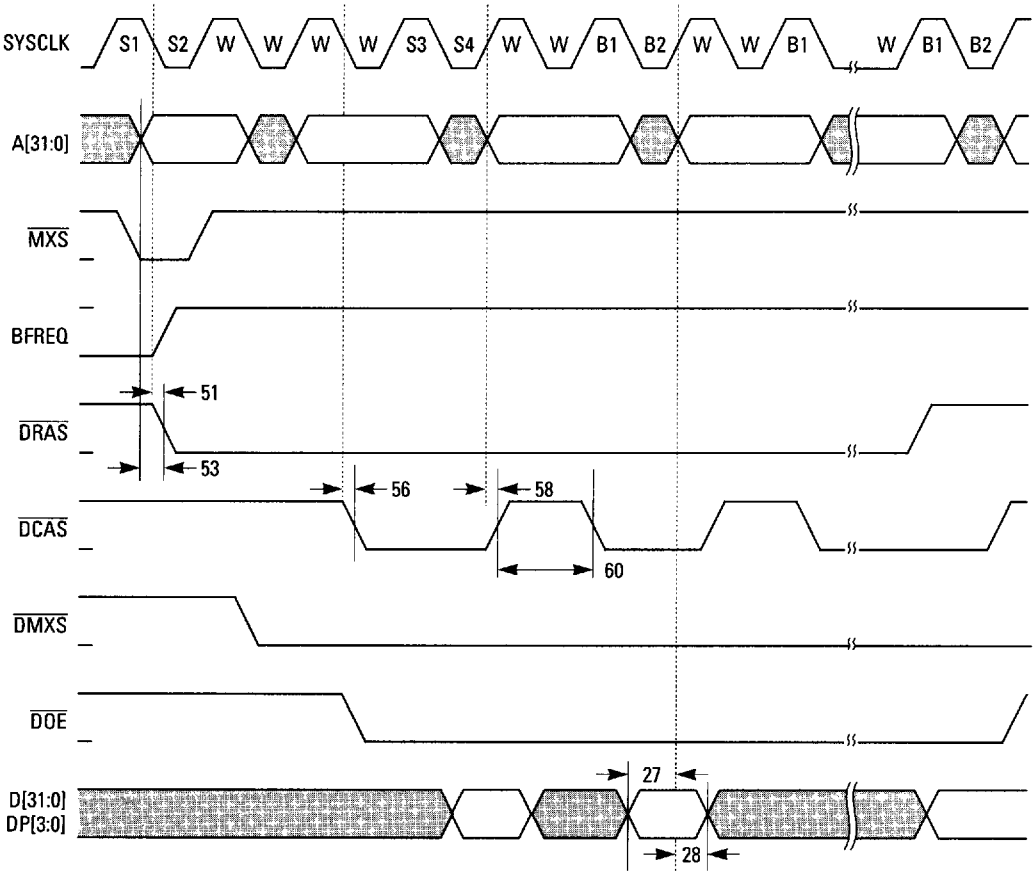


Figure 11
DRAM Block Fetch Timing



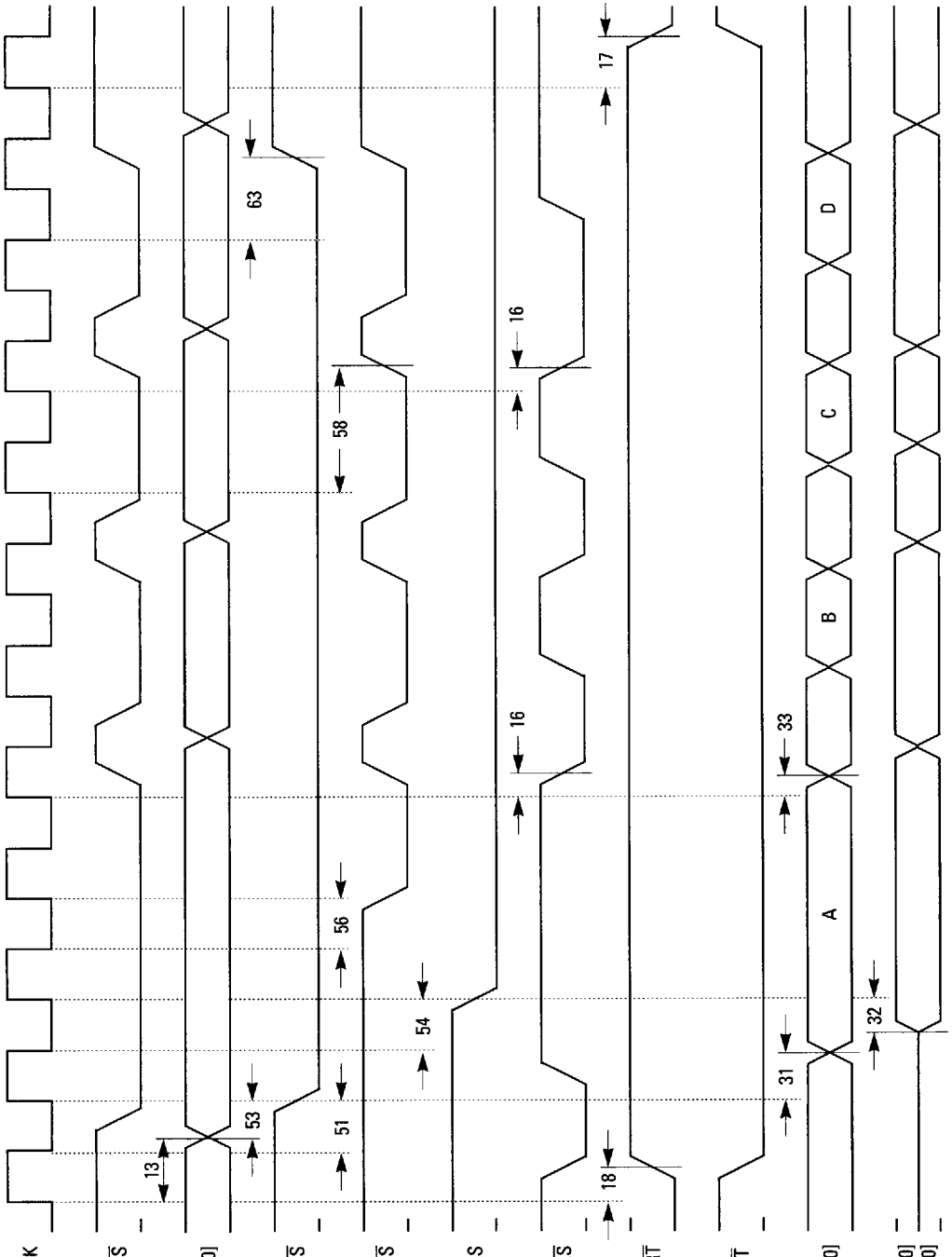


Figure 12
DRAM Page-Mode Write Timing

Figure 13
DRAM Refresh Timing

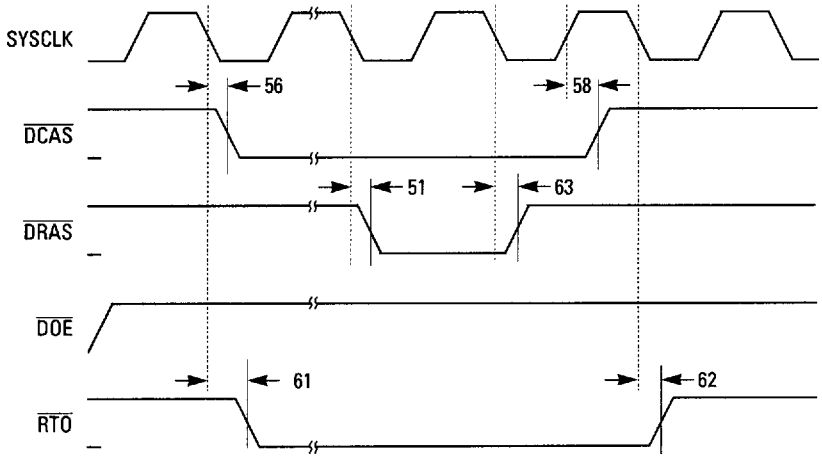
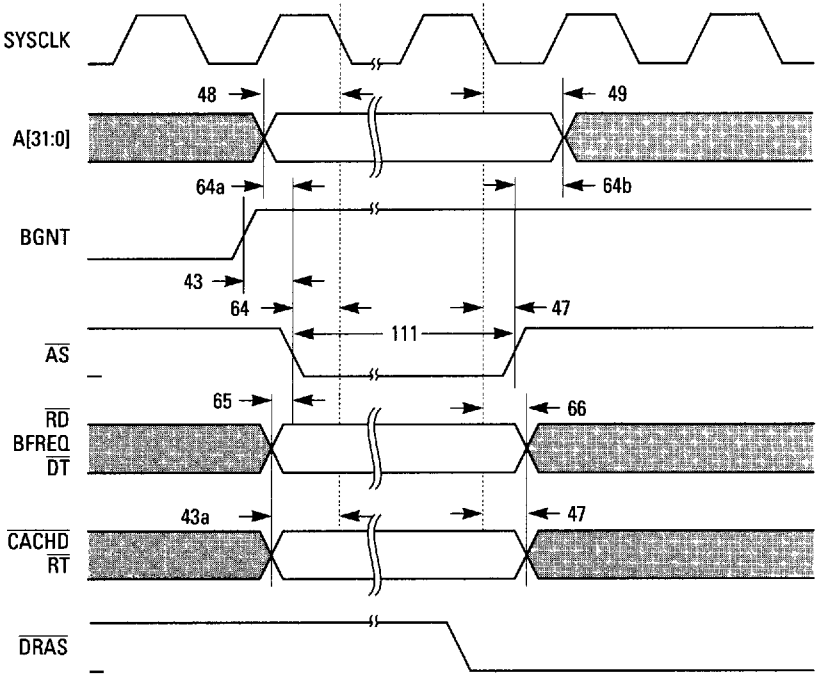
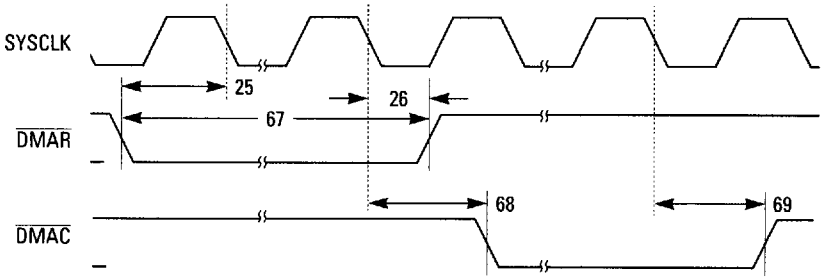


Figure 14
DMA Access Timing Using BGNT



Notes:
1. The external master must assert $\overline{AS}$ until the Controller asserts $\overline{DRAS}$ (but not $\overline{RTO}$).
2. When an *n*-word block fetch takes place, the $\overline{DCAS}$ which corresponds to the *n*th word (page-mode DRAM access) marks the end of the transaction.
3. There may be any number of cycles between the assertion of BGNT and the assertion of $\overline{AS}$ for the purpose of starting the DRAM Controller's access.

Figure 15
DMA Access Timing Using $\overline{DMAR}$



Note:
1. $\overline{DMAR}$ is an asynchronous signal. $\overline{DMAR}$ may be deasserted at any time, once the pulse width is satisfied. $\overline{DMAR}$ must be deasserted and then reasserted to initiate another $\overline{DMAC}$ sequence.

Figure 16
Timing for Miscellaneous Input and Output Signals

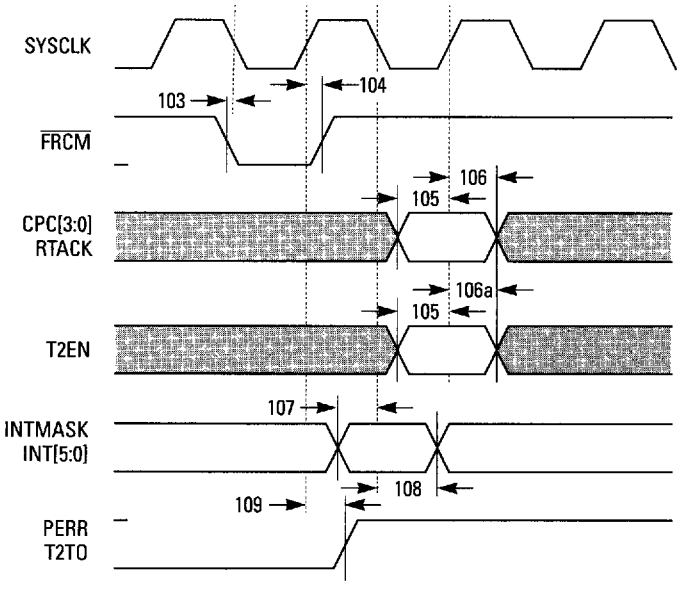


Table 1
LR33300 AC Timing Values

Parameter	Description	25 MHz Min	25 MHz Max	20 MHz Min	20 MHz Max	Units
1. t_{SH}	SYSCLK High (> 1.5 V)	16	–	20	–	ns
2. t_{SL}	SYSCLK Low (< 1.5 V)	16	–	20	–	ns
3. t_{SF}[1]	SYSCLK Fall (transition)	–	2.5	–	2.5	ns
4. t_{SR}[1]	SYSCLK Rise (transition)	–	2.5	–	2.5	ns
5. t_{SCYC}	SYSCLK Cycle	40	–	50	–	ns
6. t_{VRL}[1]	VDD (≥ 3.0 V) to $\overline{\text{RESET}}$ Low	–	5	–	5	ns
7. t_{VHZL}[1]	VDD (≥ 3.0 V) to $\overline{\text{HIGHZ}}$ Low	–	5	–	5	ns
8. t_{RLC}[1]	$\overline{\text{RESET}}$ Low (Cold)[2]	9	–	9	–	Cycles
9. t_{RHZH}[1]	$\overline{\text{RESET}}$ High to $\overline{\text{HIGHZ}}$ High (Cold)[2, 3]	0	–	0	–	ns
10. t_{RLW}[1]	$\overline{\text{RESET}}$ Low (Warm)[2]	4	–	4	–	Cycles
11. t_{HZLZ}[1]	$\overline{\text{HIGHZ}}$ Low to Output 3-State	0	30	0	30	ns
12. t_{HZOV}[1]	SYSCLK+ to Output Valid[4]	30	–	30	–	ns
13. t_{SHAV}	SYSCLK+ to Address Valid	–	26	–	28	ns
14. t_{SHBRV}	SYSCLK+ to BFREQ Valid[5]	–	20	–	22	ns
15. t_{SHBRI}	SYSCLK+ to BFREQ Invalid	–	20	–	22	ns
16. t_{SHML}	SYSCLK+ to $\overline{\text{MXS}}$ Valid	–	20	–	22	ns
17. t_{SHRTL}	SYSCLK+ to $\overline{\text{RT}}$ Low	–	20	–	22	ns
18. t_{SHRTH}	SYSCLK+ to $\overline{\text{RT}}$ High	–	18	–	20	ns
19. t_{SHDTV}	SYSCLK+ to $\overline{\text{DT}}$ Valid	–	20	–	22	ns
20. t_{SHDTI}	SYSCLK+ to $\overline{\text{DT}}$ Invalid	–	20	–	22	ns
21. t_{SLAL}	SYSCLK- to $\overline{\text{AS}}$, $\overline{\text{RD}}$ Low	–	23	–	25	ns
22. t_{SLSL}	SYSCLK- to $\overline{\text{IOSEL}}$ or $\overline{\text{EPSEL}}$ Low	–	18	–	20	ns
23. t_{SLSH}	SYSCLK+ to $\overline{\text{IOSEL}}$ or $\overline{\text{EPSEL}}$ High	–	18	–	20	ns
24. t_{AVASL}	Address Valid to $\overline{\text{AS}}$, $\overline{\text{RD}}$, $\overline{\text{IOSEL}}$, $\overline{\text{EPSEL}}$ Low	5	–	5	–	ns
25. t_{CSSL}	Control[6, 7] Setup to SYSCLK-	6	–	6	–	ns
25a. t_{DRSSL}	$\overline{\text{DRDY}}$ Setup to SYSCLK-[8]	10	–	10	–	ns
26. t_{CHSL}	Control[7, 9] Hold from SYSCLK-	5	–	5	–	ns
26a. t_{BEHSL}	$\overline{\text{BERR}}$ Hold from SYSCLK-	7	–	7	–	ns
27. t_{DSSH}	Data and Parity Setup before SYSCLK+	0	–	0	–	ns

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Table 1
LR33300 AC Timing Values

Parameter	*Description*	*25 MHz*		*20 MHz*		*Units*
		Min	*Max*	*Min*	*Max*	
28. t_{DHSH}	Data and Parity Hold from SYSCLK+	9	–	9	–	ns
29. t_{SHASH}	SYSCLK+ to $\overline{AS}$, $\overline{RD}$ High	–	15	–	15	ns
30. t_{AHSH}[1]	Address Hold from $\overline{AS}$, $\overline{RD}$, $\overline{IOSEL}$, $\overline{EPSEL}$ High	0	–	0	–	ns
30a. t_{AHWH}[1]	Address Hold from $\overline{WR}$[3:0] High	0	–	0	–	ns
31. t_{SHWRV}	SYSCLK+ to $\overline{WR}$[3:0] Valid	–	20	–	22	ns
32. t_{SHDV}	SYSCLK+ to Data and Parity Valid	–	26	–	28	ns
33. t_{SHWRH}	SYSCLK+ to $\overline{WR}$[3:0] High	–	16	–	18	ns
34. t_{WRHDI}[1]	$\overline{WR}$[3:0] High to Data and Parity 3-State	10	–	10	–	ns
35. t_{BFSSL}	$\overline{BFTCH}$ Setup to SYSCLK-	5	–	5	–	ns
36. t_{BFHSL}	$\overline{BFTCH}$ Hold from SYSCLK-	5	–	5	–	ns
37. t_{SLBAV}	SYSCLK- to Block Address[10]	–	25	–	27	ns
38. t_{BHZBGH}[1]	Bus Signals 3-State before BGNT High	-2	–	-2	–	ns
38a. t_{BABGL}[1]	Bus Signals active after BGNT Low	0	–	0	–	ns
39. t_{BSSH}	$\overline{BREQ}$ Setup before SYSCLK+	0	–	0	–	ns
40. t_{SLBGH}	SYSCLK- to BGNT High	–	20	–	22	ns
41. t_{BHSH}	$\overline{BREQ}$ Hold after SYSCLK+	7	–	7	–	ns
42. t_{SLBGL}	SYSCLK- to BGNT Low	–	20	–	22	ns
43. t_{BGHSL}[1]	BGNT High to $\overline{AS}$ Low	10	–	10	–	ns
43a. t_{RTVASL}[1]	$\overline{RT}$, $\overline{CACHD}$ Setup before SYSCLK-	10	–	10	–	ns
47. t_{ASHSL}[1]	$\overline{AS}$, $\overline{RT}$, $\overline{CACHD}$ Hold from SYSCLK-	5	–	5	–	ns
48. t_{ASSL}[1]	Address Setup before SYSCLK-	5	–	5	–	ns
49. t_{AHSL}[1]	Address Hold after SYSCLK-	5	–	5	–	ns
51. t_{SLRL}	SYSCLK- to $\overline{DRAS}$ Low	–	17	–	19	ns
53. t_{ASRL}	Address Setup before $\overline{DRAS}$ Low	8	–	8	–	ns
54. t_{SLMSL}	SYSCLK- to $\overline{DMXS}$ Low	–	16	–	18	ns
55. t_{SLMSH}	SYSCLK- to $\overline{DMXS}$ High	–	16	–	18	ns
56. t_{SLCAL}	SYSCLK+/- to $\overline{DCAS}$ Low	–	17	–	19	ns
57. t_{SLOEL}	SYSCLK- to $\overline{DOE}$ Low	–	17	–	19	ns
58. t_{SHCAH}	SYSCLK+ to $\overline{DCAS}$ High	–	17	–	19	ns
59. t_{SHOEH}	SYSCLK+ to $\overline{DOE}$ High	–	20	–	22	ns

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Table 1
LR33300 AC Timing Values

Parameter	Description	25 MHz Min	25 MHz Max	20 MHz Min	20 MHz Max	Units
60. t_{CAPW}	$\overline{DCAS}$ Precharge Time	17	–	17	–	ns
61. t_{SLRTOV}	SYSCLK- to $\overline{RTO}$ Valid	–	17	–	19	ns
62. t_{SLRTOI}	SYSCLK- to $\overline{RTO}$ Invalid	–	17	–	19	ns
63. t_{SLRAH}	SYSCLK- to $\overline{DRAS}$ High	–	15	–	17	ns
64. t_{ASSSL}[1]	$\overline{AS}$ Setup before SYSCLK-	10	–	10	–	ns
64a. t_{ASASL}[1]	Address Setup before $\overline{AS}$ Low	5	–	5	–	ns
64b. t_{AHASH}[1]	Address Hold after $\overline{AS}$ High	5	–	5	–	ns
65. t_{CSAL}[1]	$\overline{RD}$, BFREQ, and $\overline{DT}$ Setup to $\overline{AS}$ Low	0	–	0	–	ns
66. t_{CHSH}[1]	$\overline{RD}$, BFREQ, and $\overline{DT}$ Hold from SYSCLK-	5	–	5	–	ns
67. t_{DMAPW}[1]	$\overline{DMAR}$ Pulse Width[11]	40	–	50	–	ns
68. t_{SLDMCV}	SYSCLK- to $\overline{DMAC}$ Valid	–	16	–	18	ns
69. t_{SLDMCI}	SYSCLK- to $\overline{DMAC}$ Invalid	–	16	–	18	ns
100. t_{RSAH}	Miscellaneous Asynchronous[12] Setup to SYSCLK+	6	–	6	–	ns
101. t_{RHAH}[1]	Miscellaneous Asynchronous[12] Hold from SYSCLK+	5	–	5	–	ns
103. t_{FSSL}	$\overline{FRCM}$ Setup to SYSCLK-	0	–	0	–	ns
104. t_{FHSH}	$\overline{FRCM}$ Hold from SYSCLK+	4	–	4	–	ns
105. t_{RSSH}	Miscellaneous Synchronous[13] Setup to SYSCLK+	6	–	6	–	ns

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Table 1
LR33300 AC Timing Values

Parameter	Description	25 MHz Min	25 MHz Max	20 MHz Min	20 MHz Max	Units
106. t_{RHSH}	Miscellaneous Synchronous[14] Hold from SYSCLK+	5	–	5	–	ns
106a. t_{THSH}	T2EN Hold from SYSCLK+	7	–	7	–	ns
107. t_{ISSL}	INTMASK, INT[5:0] Setup to SYSCLK-	7	–	7	–	ns
108. t_{IHSH}	INTMASK, INT[5:0] Hold from SYSCLK-	7	–	7	–	ns
109. t_{SHPTV}	SYSCLK+ to PERR, T2TO Valid	–	20	–	22	ns
111. t_{ASPW}[1]	$\overline{AS}$ Pulse Width[11]	40	–	50	–	ns

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1. *This specification is guaranteed by design and is not tested.*
2. *SYSCLK must be active for $\overline{RESET}$ to take effect.*
3. *$\overline{HIGHZ}$ may go HIGH before or after $\overline{RESET}$ goes HIGH by a period of time equal to one clock cycle.*
4. *Two cycles after $\overline{HIGHZ}$ High.*
5. *Block-fetch transactions must have one wait-state in the first word of a block fetch. A block-fetch transaction is requested on any read access to cacheable memory after a cache miss.*
6. *Includes $\overline{BERR}$, $\overline{CACHD}$, $\overline{BWIDE}$, $\overline{PEN}$, and $\overline{DMAR}$. Also includes $\overline{DRDY}$ only for non-DRAM cycles.*
7. *Once sampled at SYSCLK-, $\overline{BWIDE}$ is ignored until four bytes have been fetched or a bus error has been detected. $\overline{PEN}$ is ignored if $\overline{BWIDE}$ is sampled at SYSCLK-.*
8. *This parameter is applicable only when an external controller asserts $\overline{DRDY}$ to terminate a DRAM read or write transaction.*
9. *Includes $\overline{DRDY}$, $\overline{CACHD}$, $\overline{BWIDE}$, $\overline{PEN}$, and $\overline{DMAR}$.*
10. *Block address 0 is placed on the address bus in response to $\overline{BFTCH}$ LOW. Each subsequent address is issued in response to $\overline{DRDY}$ LOW. $\overline{AS}$ and $\overline{RD}$ are deasserted after all data in a block has been fetched or there is a bus error.*
11. *The one-cycle pulse width for these asynchronous signals guarantees that the LR333x0 will latch the signals when they are asserted.*
12. *Miscellaneous asynchronous signals include $\overline{RESET}$ and $\overline{HIGHZ}$. These setup and hold times can be ignored for designs that do not require the synchronization of the LR333x0 with other parts such as additional processors.*
13. *Miscellaneous synchronous signals include CPC[3:0], RTACK, and T2EN.*
14. *Miscellaneous synchronous signals include CPC[3:0] and RTACK.*

Table 2
LR33310 AC Timing Values

Parameter	Description	50 MHz Min	50 MHz Max	40 MHz Min	40 MHz Max	33 MHz Min	33 MHz Max	Units
1. t_{SH}	SYSCLK High (> 1.5 V)	9.5	–	12	–	14	–	ns
2. t_{SL}	SYSCLK Low (< 1.5 V)	9.5	–	12	–	14	–	ns
3. t_{SF}[1]	SYSCLK Fall (transition)	–	2.0	–	2.0	–	2.5	ns
4. t_{SR}[1]	SYSCLK Rise (transition)	–	2.0	–	2.0	–	2.5	ns
5. t_{SCYC}	SYSCLK Cycle	20	–	25	–	30	–	ns
6. t_{VRL}[1]	VDD (≥ 3.0 V) to $\overline{\text{RESET}}$ Low	–	5	–	5	–	5	ns
7. t_{VHZL}[1]	VDD (≥ 3.0 V) to $\overline{\text{HIGHZ}}$ Low	–	5	–	5	–	5	ns
8. t_{RLC}[1]	$\overline{\text{RESET}}$ Low (Cold)[2]	9	–	9	–	9	–	Cycles
9. t_{RHZH}[1]	$\overline{\text{RESET}}$ High to $\overline{\text{HIGHZ}}$ High (Cold)[2, 3]	0	–	0	–	0	–	ns
10. t_{RLW}[1]	$\overline{\text{RESET}}$ Low (Warm)[2]	4	–	4	–	4	–	Cycles
11. t_{HZLZ}[1]	$\overline{\text{HIGHZ}}$ Low to Output 3-State	0	25	0	25	0	25	ns
12. t_{HZOV}[1]	SYSCLK+ to Output Valid[4]	25	–	25	–	25	–	ns
13. t_{SHAV}	SYSCLK+ to Address Valid	–	14	–	17	–	20	ns
14. t_{SHBRV}	SYSCLK+ to BFREQ Valid[5]	–	14	–	15	–	16	ns
15. t_{SHBRI}	SYSCLK+ to BFREQ Invalid	–	14	–	15	–	16	ns
16. t_{SHML}	SYSCLK+ to $\overline{\text{MXS}}$ Valid	–	14	–	15	–	16	ns
17. t_{SHRTL}	SYSCLK+ to $\overline{\text{RT}}$ Low	–	14	–	15	–	16	ns
18. t_{SHRTH}	SYSCLK+ to $\overline{\text{RT}}$ High	–	13	–	14	–	15	ns
19. t_{SHDTV}	SYSCLK+ to $\overline{\text{DT}}$ Valid	–	14	–	15	–	16	ns
20. t_{SHDTI}	SYSCLK+ to $\overline{\text{DT}}$ Invalid	–	14	–	15	–	16	ns
21. t_{SLAL}	SYSCLK- to $\overline{\text{AS}}$, $\overline{\text{RD}}$ Low	–	14	–	17	–	20	ns
22. t_{SLSL}	SYSCLK- to $\overline{\text{IOSEL}}$ or $\overline{\text{EPSEL}}$ Low	–	13	–	14	–	15	ns
23. t_{SLSH}	SYSCLK+ to $\overline{\text{IOSEL}}$ or $\overline{\text{EPSEL}}$ High	–	13	–	14	–	15	ns
24. t_{AVASL}	Address Valid to $\overline{\text{AS}}$, $\overline{\text{RD}}$, $\overline{\text{IOSEL}}$, $\overline{\text{EPSEL}}$ Low	5	–	5	–	5	–	ns
25. t_{CSSL}	Control[6, 7] Setup to SYSCLK-	3	–	4	–	5	–	ns
25a. t_{DRSSL}	$\overline{\text{DRDY}}$ Setup to SYSCLK-[8]	7	–	8	–	9	–	ns
26. t_{CHSL}	Control[7, 9] Hold from SYSCLK-	2	–	3	–	4	–	ns
26a. t_{BEHSL}	$\overline{\text{BERR}}$ Hold from SYSCLK-	4	–	5	–	6	–	ns
27. t_{DSSH}	Data and Parity Setup before SYSCLK+	0	–	0	–	0	–	ns

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Table 2 (Cont.)
LR33310 AC Timing Values

Parameter	*Description*	*50 MHz*		*40 MHz*		*33 MHz*		*Units*
		Min	*Max*	*Min*	*Max*	*Min*	*Max*	
28. t_{DHSH}	Data and Parity Hold from SYSCLK+	5	–	6	–	7	–	ns
29. t_{SHASH}	SYSCLK+ to $\overline{AS}$, $\overline{RD}$ High	–	11	–	12	–	13	ns
30. t_{AHSH}[1]	Address Hold from $\overline{AS}$, $\overline{RD}$, $\overline{IOSEL}$, $\overline{EPSEL}$ High	0	–	0	–	0	–	ns
30a. t_{AHWH}[1]	Address Hold from $\overline{WR}$[3:0] High	0	–	0	–	0	–	ns
31. t_{SHWRV}	SYSCLK+ to $\overline{WR}$[3:0] Valid	–	14	–	15	–	16	ns
32. t_{SHDV}	SYSCLK+ to Data and Parity Valid	–	17	–	19	–	21	ns
33. t_{SHWRH}	SYSCLK+ to $\overline{WR}$[3:0] High	–	12	–	13	–	14	ns
34. t_{WRHDI}[1]	$\overline{WR}$[3:0] High to Data and Parity 3-State	10	–	10	–	10	–	ns
35. t_{BFSSL}	$\overline{BFTCH}$ Setup to SYSCLK-	2	–	3	–	4	–	ns
36. t_{BFHSL}	$\overline{BFTCH}$ Hold from SYSCLK-	2	–	3	–	4	–	ns
37. t_{SLBAV}	SYSCLK- to Block Address[10]	–	14	–	17	–	20	ns
38. t_{BHZBGH}[1]	Bus Signals 3-State before BGNT High	-2	–	-2	–	-2	–	ns
38a. t_{BABGL}[1]	Bus Signals active after BGNT Low	0	–	0	–	0	–	ns
39. t_{BSSH}	$\overline{BREQ}$ Setup before SYSCLK+	0	–	0	–	0	–	ns
40. t_{SLBGH}	SYSCLK- to BGNT High	–	14	–	15	–	16	ns
41. t_{BHSH}	$\overline{BREQ}$ Hold after SYSCLK+	5	–	5	–	5	–	ns
42. t_{SLBGL}	SYSCLK- to BGNT Low	–	13	–	14	–	15	ns
43. t_{BGHSL}[1]	BGNT High to $\overline{AS}$ Low	8	–	8	–	8	–	ns
43a. t_{RTVASL}[1]	$\overline{RT}$, $\overline{CACHD}$ Setup before SYSCLK-	8	–	8	–	8	–	ns
47. t_{ASHSH}[1]	$\overline{AS}$, $\overline{RT}$, $\overline{CACHD}$ Hold from SYSCLK-	4	–	4	–	4	–	ns
48. t_{ASSL}[1]	Address Setup before SYSCLK-	4	–	4	–	4	–	ns
49. t_{AHSL}[1]	Address Hold after SYSCLK-	4	–	4	–	4	–	ns
51. t_{SLRL}	SYSCLK- to $\overline{DRAS}$ Low	–	12	–	13	–	14	ns
53. t_{ASRL}	Address Setup before $\overline{DRAS}$ Low	5	–	5	–	5	–	ns
54. t_{SLMSL}	SYSCLK- to $\overline{DMXS}$ Low	–	12	–	13	–	14	ns
55. t_{SLMSH}	SYSCLK- to $\overline{DMXS}$ High	–	12	–	13	–	14	ns
56. t_{SLCAL}	SYSCLK+/- to $\overline{DCAS}$ Low	–	12	–	13	–	14	ns
57. t_{SLOEL}	SYSCLK- to $\overline{DOE}$ Low	–	12	–	13	–	14	ns
58. t_{SHCAH}	SYSCLK+ to $\overline{DCAS}$ High	–	12	–	13	–	14	ns
59. t_{SHOEH}	SYSCLK+ to $\overline{DOE}$ High	–	17	–	18	–	19	ns

(Sheet 2 of 4)

Table 2 (Cont.)
LR33310 AC Timing Values

Parameter	Description	50 MHz Min	50 MHz Max	40 MHz Min	40 MHz Max	33 MHz Min	33 MHz Max	Units
60. t_{CAPW}	$\overline{DCAS}$ Precharge Time	9	–	11	–	13	–	ns
61. t_{SLRTOV}	SYSCLK- to $\overline{RTO}$ Valid	–	11	–	13	–	15	ns
62. t_{SLRTOI}	SYSCLK- to $\overline{RTO}$ Invalid	–	11	–	13	–	15	ns
63. t_{SLRAH}	SYSCLK- to $\overline{DRAS}$ High	–	10	–	12	–	14	ns
64. t_{ASSSL}[1]	$\overline{AS}$ Setup before SYSCLK-	6	–	7	–	8	–	ns
64a. t_{ASASL}[1]	Address Setup before $\overline{AS}$ Low	5	–	5	–	5	–	ns
64b. t_{AHASH}[1]	Address Hold after $\overline{AS}$ High	5	–	5	–	5	–	ns
65. t_{CSAL}[1]	$\overline{RD}$, BFREQ, and $\overline{DT}$ Setup to $\overline{AS}$ Low	0	–	0	–	0	–	ns
66. t_{CHSH}[1]	$\overline{RD}$, BFREQ, and $\overline{DT}$ Hold from SYSCLK-	5	–	5	–	5	–	ns
67. t_{DMAPW}[1]	$\overline{DMAR}$ Pulse Width[11]	20	–	25	–	30	–	ns
68. t_{SLDMCV}	SYSCLK- to $\overline{DMAC}$ Valid	–	12	–	13	–	14	ns
69. t_{SLDMCI}	SYSCLK- to $\overline{DMAC}$ Invalid	–	12	–	13	–	14	ns
100. t_{RSAH}	Miscellaneous Asynchronous[12] Setup to SYSCLK+	3	–	4	–	5	–	ns
101. t_{RHAH}[1]	Miscellaneous Asynchronous[12] Hold from SYSCLK+	3	–	4	–	5	–	ns
103. t_{FSSL}	$\overline{FRCM}$ Setup to SYSCLK-	0	–	0	–	0	–	ns
104. t_{FHSH}	$\overline{FRCM}$ Hold from SYSCLK+	4	–	4	–	4	–	ns
105. t_{RSSH}	Miscellaneous Synchronous[13] Setup to SYSCLK+	3	–	4	–	5	–	ns

(Sheet 3 of 4)

Table 2 (Cont.)
LR33310 AC Timing Values

Parameter	Description	50 MHz Min	50 MHz Max	40 MHz Min	40 MHz Max	33 MHz Min	33 MHz Max	Units
106. t_{RHSH}	Miscellaneous Synchronous[14] Hold from SYSCLK+	3	–	4	–	5	–	ns
106a. t_{THSH}	T2EN Hold from SYSCLK+	4	–	5	–	6	–	ns
107. t_{ISSL}	INTMASK, INT[5:0] Setup to SYSCLK-	4	–	5	–	6	–	ns
108. t_{IHSH}	INTMASK, INT[5:0] Hold from SYSCLK-	4	–	5	–	6	–	ns
109. t_{SHPTV}	SYSCLK+ to PERR, T2TO Valid	–	14	–	15	–	16	ns
111. t_{ASPW}[1]	$\overline{AS}$ Pulse Width[11]	20	–	25	–	30	–	ns

(Sheet 4 of 4)

1. *This specification is guaranteed by design and is not tested.*
2. *SYSCLK must be active for $\overline{RESET}$ to take effect.*
3. *$\overline{HIGHZ}$ may go HIGH before or after $\overline{RESET}$ goes HIGH by a period of time equal to one clock cycle.*
4. *Two cycles after $\overline{HIGHZ}$ High.*
5. *Block-fetch transactions must have one wait-state in the first word of a block fetch. A block-fetch transaction is requested on any read access to cacheable memory after a cache miss.*
6. *Includes $\overline{BERR}$, $\overline{CACHD}$, $\overline{BWIDE}$, $\overline{PEN}$, and $\overline{DMAR}$. Also includes $\overline{DRDY}$ only for non-DRAM cycles.*
7. *Once sampled at SYSCLK-, $\overline{BWIDE}$ is ignored until four bytes have been fetched or a bus error has been detected. $\overline{PEN}$ is ignored if $\overline{BWIDE}$ is sampled at SYSCLK-.*
8. *This parameter is applicable only when an external controller asserts $\overline{DRDY}$ to terminate a DRAM read or write transaction.*
9. *Includes $\overline{DRDY}$, $\overline{CACHD}$, $\overline{BWIDE}$, $\overline{PEN}$, and $\overline{DMAR}$.*
10. *Block address 0 is placed on the address bus in response to $\overline{BFTCH}$ LOW. Each subsequent address is issued in response to $\overline{DRDY}$ LOW. $\overline{AS}$ and $\overline{RD}$ are deasserted after all data in a block has been fetched or there is a bus error.*
11. *The one-cycle pulse width for these asynchronous signals guarantees that the LR333x0 will latch the signals when they are asserted.*
12. *Miscellaneous asynchronous signals include $\overline{RESET}$ and $\overline{HIGHZ}$. These setup and hold times can be ignored for designs that do not require the synchronization of the LR333x0 with other parts such as additional processors.*
13. *Miscellaneous synchronous signals include CPC[3:0], RTACK, and T2EN.*
14. *Miscellaneous synchronous signals include CPC[3:0] and RTACK.*

Electrical Requirements

This section specifies the electrical requirements for the LR333x0. Five tables list electrical data in the following categories:

- Absolute Maximum Ratings (Table 3)
- Recommended Operating Conditions (Table 4)
- Capacitance (Table 5)
- DC Characteristics (Table 6)
- Pin Description Summary (Table 7)

Table 3 Absolute Maximum Ratings

Symbol	*Parameter*	*Limits*[1]	*Unit*
V_{DD}	DC Supply	-0.3 to +7	V
V_{IN}	Input Voltage	-0.3 to V_{DD} + 0.3	V
I_{IN}	DC Input Current	±10	mA
T_{STG}	Storage Temperature Range, Metal	0 to +125	°C
T_{STG}	Storage Temperature Range, Plastic	-40 to +125	°C

1. Referenced to V_{SS}.

The values listed in Table 4 are based on zero airflow with no external heat sink.

Table 4 Recommended Operating Conditions

Symbol	*Parameter*	*Limits*	*Unit*
V_{DD}	DC Supply, Commercial	+4.75 to +5.25	V
T_A	Ambient Temperature, LR33300 (20 and 25 MHz) and LR33310 (33 and 40 MHz)	0 to +70	°C
T_A	Ambient Temperature, LR33310 (50 MHz)	0 to +50	°C

Table 5 Capacitance

Symbol	*Parameter*[1]	*Min*	*Typ*	*Max*	*Unit*
C_{IN}	Input Capacitance			5	pF
C_{OUT}	Output Capacitance			10	pF
C_{IO}	I/O Bus Capacitance			15	pF

1. Measurement conditions are V_{IN} = 5.0 V, T_A = 25 °C, and clock frequency = 1 MHz.

Table 6
DC Characteristics

Symbol	*Parameter*	*Condition*[1]	*Min*	*Typ*	*Max*	*Units*
V_{IL}	Voltage Input Low		–	–	0.8	V
V_{IH}	Voltage Input High		2.0	–	–	V
V_{OH}	Voltage Output High	I_{OH} = -4.0 mA	2.4	4.5	–	V
		I_{OH} = -8.0 mA	2.4	4.5	–	V
V_{OL}	Voltage Output Low	I_{OL} = 4.0 mA	–	0.2	0.4	V
		I_{OL} = 8.0 mA	–	0.2	0.4	V
I_{IL}	Current Input Leakage	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	-10	±1	10	µA
I_{OZ}	Current 3-State Output Leakage	V_{DD} = Max, V_{OUT} = V_{SS} or V_{DD}	-10	±1	10	µA
I_{IPU}	Current Input Pull-up	V_{IN} = V_{SS}	-35	-115	-350	µA
I_{OZU}	Current 3-State Output w/Pull-up	V_{IN} = V_{SS}	-2	–	-175	µA
I_{OSP4}	Current P-Channel Output Short Circuit (4 mA Output Buffers)[2]	V_{DD} = Max, V_{OUT} = V_{SS}	-25	-70	-140	mA
I_{OSP8}	Current P-Channel Output Short Circuit (8 mA Output Buffers)[2]	V_{DD} = Max, V_{OUT} = V_{SS}	-50	-140	-280	mA
I_{OSN4}	Current N-Channel Output Short Circuit (4 mA Output Buffers)[2]	V_{DD} = Max, V_{OUT} = V_{DD}	30	75	140	mA
I_{OSN8}	Current N-Channel Output Short Circuit (8 mA Output Buffers)[2]	V_{DD} = Max, V_{OUT} = V_{DD}	60	150	280	mA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}	–	–	2	mA
I_{CC}	Dynamic Supply Current	V_{DD} = Max, f = 20 MHz			275	mA
		V_{DD} = Max, f = 25 MHz			345	mA
		V_{DD} = Max, f = 33 MHz		450	510	mA
		V_{DD} = Max, f = 40 MHz		550	620	mA
		V_{DD} = Max, f = 50 MHz		600	765	mA

1. Specified at V_{DD} equals 5 V ± 5% at ambient temperature over the specified range.
2. Not more than one output may be shorted at a time for a maximum duration of one second.

Table 7
Pin Description Summary

Mnemonic	*Description*	*Type*[1]	*Drive (mA)*	*Active*
A[31:0]	Address Bus	3-State Bidirectional	4	High
$\overline{AS}$	Address Strobe	3-State Bidirectional, PU	8	Low
BENDN	Big Endian	Input	–	High
$\overline{BERR}$	Bus Error	Input, PU	–	Low
BFREQ	Block Fetch Request	3-State Bidirectional	8	High
$\overline{BFTCH}$	Block Fetch	Input, PU	–	Low
BGNT	Bus Grant	3-State Output	8	High
$\overline{BREQ}$	Bus Request	Input	–	Low
BRTKN	Branch Taken	3-State Bidirectional, PU	8	High
$\overline{BWIDE}$	Byte Wide	Input, PU	–	Low
$\overline{CACHD}$	Cacheable Data	Input, PU	–	Low
CPC[3:0]	Coprocessor Condition	Input	–	High
D[31:0]	Data Bus	3-State Bidirectional	4	High
DP[3:0]	Data Parity Bus	3-State Bidirectional	8	High
$\overline{DCAS}$	DRAM Column Address Strobe	3-State Output, PU	8	Low
$\overline{DMAC}$	DMA Cycle	3-State Output	8	Low
$\overline{DMAR}$	DMA Request	Input	–	Low
DMXS	DRAM Mux Select	3-State Output	8	High
$\overline{DOE}$	Data Output Enable	3-State Output, PU	8	Low
$\overline{DRAS}$	DRAM Row Address Strobe	3-State Output, PU	8	Low
$\overline{DRDY}$	Data Ready	Input, PU	–	Low
$\overline{DT}$	Data Transaction	3-State Output	8	Low
$\overline{EPSEL}$	EPROM Select	3-State Output, PU	8	Low
$\overline{FRCM}$	Force Cache Miss	Input, PU	–	Low
$\overline{HIGHZ}$	High Impedance	Input	–	Low
$\overline{INIT8}$	Initial Value for 8WIDE	Input, PU	-	–
$\overline{INIT16}$	Initial Value for 16WIDE	Input, PU		–
INT[5:0]	Interrupt [5:0]	Input	–	High/Low[2]
INTMASK	Interrupt Mask	Input	–	High
$\overline{IOSEL}$	I/O Select	3-State Output, PU	8	Low
$\overline{MXS}$	Memory Transaction Start	3-State Output, PU	8	Low
$\overline{PEN}$	Parity Enable	Input, PU	–	Low
PERR	Parity Error	3-State Output	8	High
$\overline{RESET}$	Reset	Input	–	Low
$\overline{RD}$	Read Strobe	3-State Bidirectional	8	Low
$\overline{RT}$	Read Transaction	3-State Bidirectional, PU	8	Low
RTACK	Refresh Timer Acknowledge	Input	–	High
$\overline{RTO}$	Refresh Timeout	3-State Output, PU	8	Low
$\overline{STALL}$	Stall	3-State Output	8	Low
SYSCLK	System Clock	Input	–	–
T2EN	Timer 2 Enable	Input	–	High
T2TO	Timer 2 Timeout	3-State Output	8	–
$\overline{WR}$[3:0]	Write Strobe [3:0]	3-State Output	8	Low

1. PU = internal pullup resistor.
2. The INTP bit in the BIU/Cache Configuration Register determines the polarity of INT[5:0].

Packaging

The LR33300 is available in a 160-pin Plastic Quad Flat Pack package (PQFP). The LR33310 is available in a 160-pin Metal Quad Flat Pack package (MQUAD).

Ordering Information

Table 8 lists the LR333x0 according to order number and package type.

Table 8 LR333x0 Ordering Information

Order Number	*Clock Frequency (MHz)*	*Package Type*	*Operating Range*
LR33300MC-20	20	160-pin PQFP	Commercial
LR33300MC-25	25	160-pin PQFP	Commercial
LR33310MC-33	33	160-pin MQUAD	Commercial
LR33310MC-40	40	160-pin MQUAD	Commercial
LR33310MC-50	50	160-pin MQUAD	Commercial

For debugging purposes, a 160-pin socket for the MQUAD package is available. One recommended vendor of this socket is:

Yamaichi
Contact: Frank Lessani
Part Number IC51-1604-845-04
408.452.0797

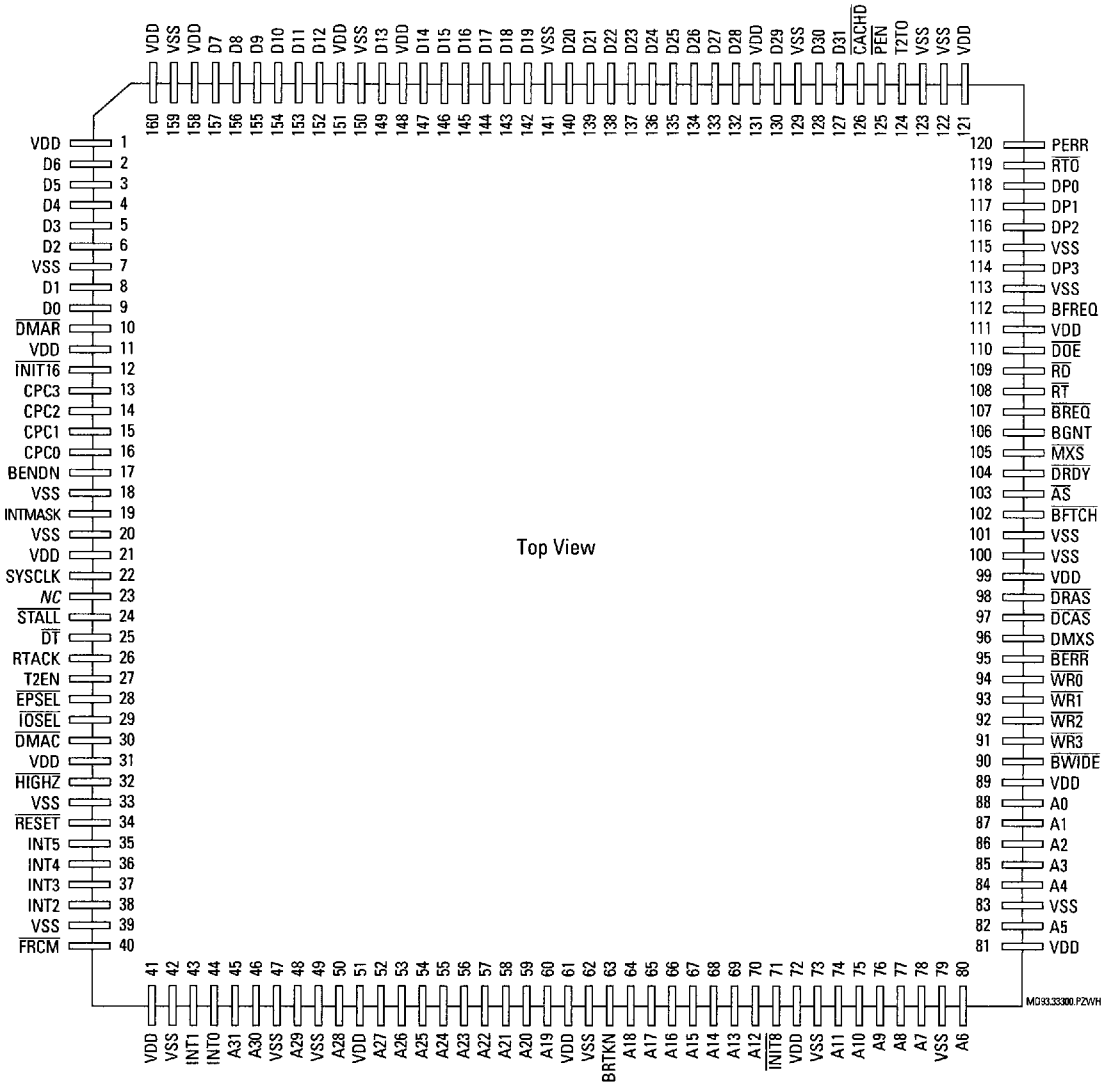
Package Information

This subsection provides three types of information for each package type: an alphabetical pin list, a pinout, and a mechanical drawing. The pin list and pinout are the same for the PQFP and MQUAD packages. Table 9 on page 26 and Figure 17 on page 27 contain the pin list and pinout, respectively. Figure 18 on page 28 shows the PQFP mechanical drawing. Figure 19 on page 29 shows the MQUAD mechanical drawing.

Table 9
Alphabetical Pin List for the 160-Pin MQUAD and 160-Pin PQFP

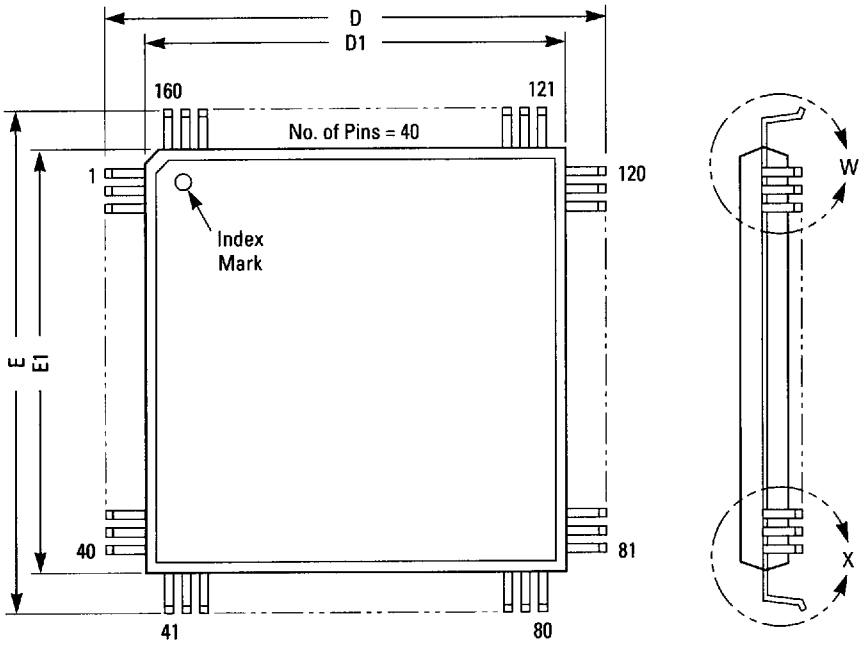
Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A0	88	$\overline{\text{CACHD}}$	126	$\overline{\text{DCAS}}$	97	VSS	20
A1	87	CPC0	16	$\overline{\text{DMAC}}$	30	VSS	33
A2	86	CPC1	15	$\overline{\text{DMAR}}$	10	VSS	39
A3	85	CPC2	14	DMXS	96	VSS	42
A4	84	CPC3	13	$\overline{\text{DOE}}$	110	VSS	47
A5	82	D0	9	$\overline{\text{DRAS}}$	98	VSS	49
A6	80	D1	8	$\overline{\text{DRDY}}$	104	VSS	62
A7	78	D2	6	$\overline{\text{DT}}$	25	VSS	73
A8	77	D3	5	$\overline{\text{EPSEL}}$	28	VSS	79
A9	76	D4	4	$\overline{\text{FRCM}}$	40	VSS	83
A10	75	D5	3	$\overline{\text{HIGHZ}}$	32	VSS	100
A11	74	D6	2	$\overline{\text{INIT16}}$	12	VSS	101
A12	70	D7	157	$\overline{\text{INIT8}}$	71	VSS	113
A13	69	D8	156	INT5	35	VSS	115
A14	68	D9	155	INT4	36	VSS	122
A15	67	D10	154	INT3	37	VSS	123
A16	66	D11	153	INT2	38	VSS	129
A17	65	D12	152	INT1	43	VSS	141
A18	64	D13	149	INT0	44	VSS	150
A19	60	D14	147	INTMASK	19	VSS	159
A20	59	D15	146	$\overline{\text{IOSEL}}$	29	VDD	1
A21	58	D16	145	$\overline{\text{MXS}}$	105	VDD	11
A22	57	D17	144	$\overline{\text{PEN}}$	125	VDD	21
A23	56	D18	143	PERR	120	VDD	31
A24	55	D19	142	$\overline{\text{RESET}}$	34	VDD	41
A25	54	D20	140	$\overline{\text{RD}}$	109	VDD	51
A26	53	D21	139	$\overline{\text{RT}}$	108	VDD	61
A27	52	D22	138	RTACK	26	VDD	72
A28	50	D23	137	$\overline{\text{RTO}}$	119	VDD	81
A29	48	D24	136	$\overline{\text{STALL}}$	24	VDD	89
A30	46	D25	135	SYSCLK	22	VDD	99
A31	45	D26	134	T2EN	27	VDD	111
$\overline{\text{AS}}$	103	D27	133	T2TO	124	VDD	121
BENDN	17	D28	132	$\overline{\text{WR0}}$	94	VDD	131
$\overline{\text{BERR}}$	95	D29	130	$\overline{\text{WR1}}$	93	VDD	148
BFREQ	112	D30	128	$\overline{\text{WR2}}$	92	VDD	151
$\overline{\text{BFTCH}}$	102	D31	127	$\overline{\text{WR3}}$	91	VDD	158
BGNT	106	DP0	118	VSS	7	VDD	160
$\overline{\text{BREQ}}$	107	DP1	117	VSS	18		
BRTKN	63	DP2	116				
$\overline{\text{BWIDE}}$	90	DP3	114				

Figure 17
160-Pin MQUAD and
160-Pin PQFP Pinout



Note:
1. *NC* (not connected) pins must *not* be connected to anything.

Figure 18
160-Pin PQFP Mechanical Drawing

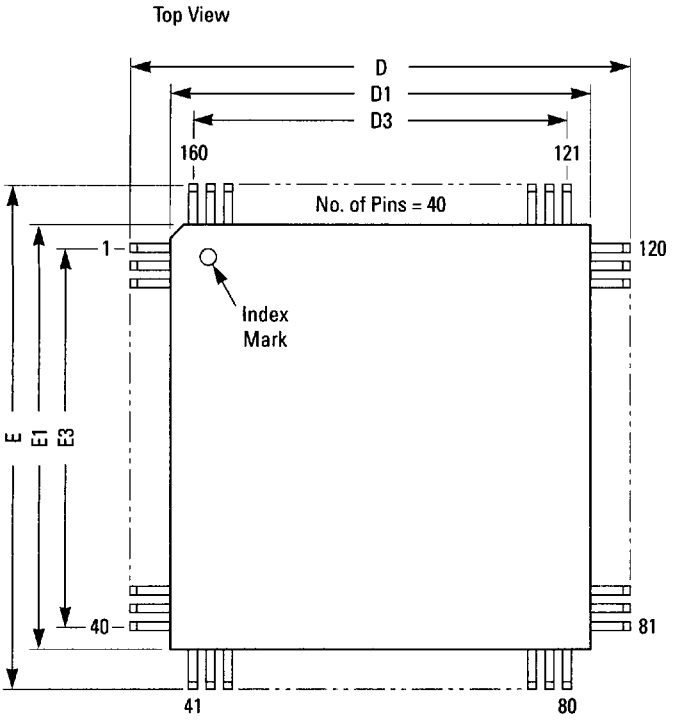


Dimension		mm
A	Max	3.86
A1	Min	0.25
	Max	0.36
A2	Min	3.30
	Max	3.50
B	Min	0.25
	Max	0.35
C	Min	0.12
	Max	0.18
D	Min	31.00
	Nom	31.20
	Max	31.40
D1	Min	27.90
	Nom	28.00
	Max	28.10
e	BSC	0.65
E	Min	31.00
	Nom	31.20
	Max	31.40
E1	Min	27.90
	Nom	28.00
	Max	28.10
L	Min	0.70
	Nom	0.80
	Max	0.90
θ	Min	0°
	Max	5°

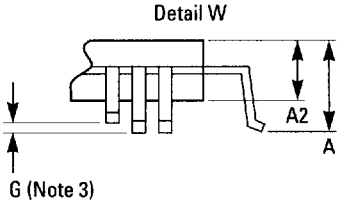
Note:
1. Total number of pins is 160.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.076 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Datum plane – H – is located at mold parting line and is coincident with the bottom of the lead, where the lead exits the plastic body. Lead pitch determined at – H –.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. These dimensions to be determined at – H –.
6. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code PZ.

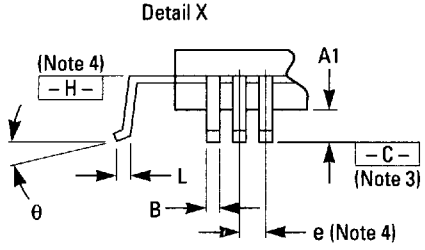
MD93.PZ

Figure 19
160-Pin MQUAD
Mechanical Drawing



Dimension		mm
A	Max	3.86
A1	Min	0.25
	Max	0.51
A2	Min	3.17
	Max	3.43
B	Typ	0.30
D	Min	31.00
	Max	31.40
D1	Min	27.56
	Max	27.72
D3	BSC	25.35
E	Min	31.00
	Max	31.40
E1	Min	27.56
	Max	27.72
E3	BSC	25.35
θ	Min	0°
	Max	7°
e	BSC	0.65
G	Max	0.10
L	Min	0.67
	Max	0.93





Note:
1. Total number of pins is 160.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Lead pitch determined at – H –.
5. Leadframe to package offset tolerance is ±0.10 mm Max.
6. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code WH.

MD93.WH