ST8012

Dot Matrix Lcd

120 Output LCD Common/Segment driver IC

Notice: Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice. This is not a final specification. Some parameters are subject to change.

1. DESCRIPTION

The ST8012 is a 120-output segment/common driver IC suitable for driving small/medium scale dot matrix LCD panels, and is used in PDA or electronic dictionary. The ST8012 is good as a segment driver or a common driver or a common/segment driver, and it can create a low power consuming, high-resolution LCD. The ST8012 have eight modes can selected to set common and segment numbers by select pin. The ST8012 also have analog DC/DC converter to use.

2. FEATURES

- Number of LCD drive outputs: 120
- Supply voltage for LCD drive: Max +16V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption and low output impedance
- Display duty selectable by select pin

SEL_2 SEL_1 SEL_0	DUTY	BIAS
0 0 0	---	Segment mode
0 0 1	1/32	1/6 or 1/5
0 1 0	1/48	1/7 or 1/5
0 1 1	1/64	1/9 or 1/7
1 0 0	1/80	1/9 or 1/7
1 0 1	1/96	1/10 or 1/8
1 1 0	1/112	1/11 or 1/9
1 1 1	1/120	1/11 or 1/9

- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratio of 2X/3X/4X/5X/6X)
- Abundant command functions
  LCD bias set, electronic volume, V_{SS} voltage regulation internal resistor ratio and booster frequency.
  All Functions have initial value, user can use the default value or setting by programmable pin to set.
- If select segment mode then except booster circuit will opened others circuit (follower and regulator circuit) will automatic closed.
- When don't used the serial interface, we can select one of default modes by serial interface pins please see Table5.
- Package: 154-pin COB.

(Segment mode)

- Shift clock frequency
  - 20 MHz (MAX.): V_{DD} = +5.0 ± 0.5 V
  - 15 MHz (MAX.): V_{DD} = +3.0 to + 4.5 V
  - 12 MHz (MAX.): V_{DD} = +2.5 to + 3.0 V
- Adopts a data bus system
- 4-bit parallel / serial input modes are selectable with a mode (P/S) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 88、72、56 、40、24、8 or 120 bits of input data
- Line latch circuits are reset when XDISPOFF active

(Common mode)

- Shift clock frequency: 4 MHz (MAX.)

- Built-in X-bit shift register
- Available in a single mode
- Y_1->Y_X Single mode

  Y_X->Y_1 Single mode

  PS:X=32、48、64、80、96、112、120

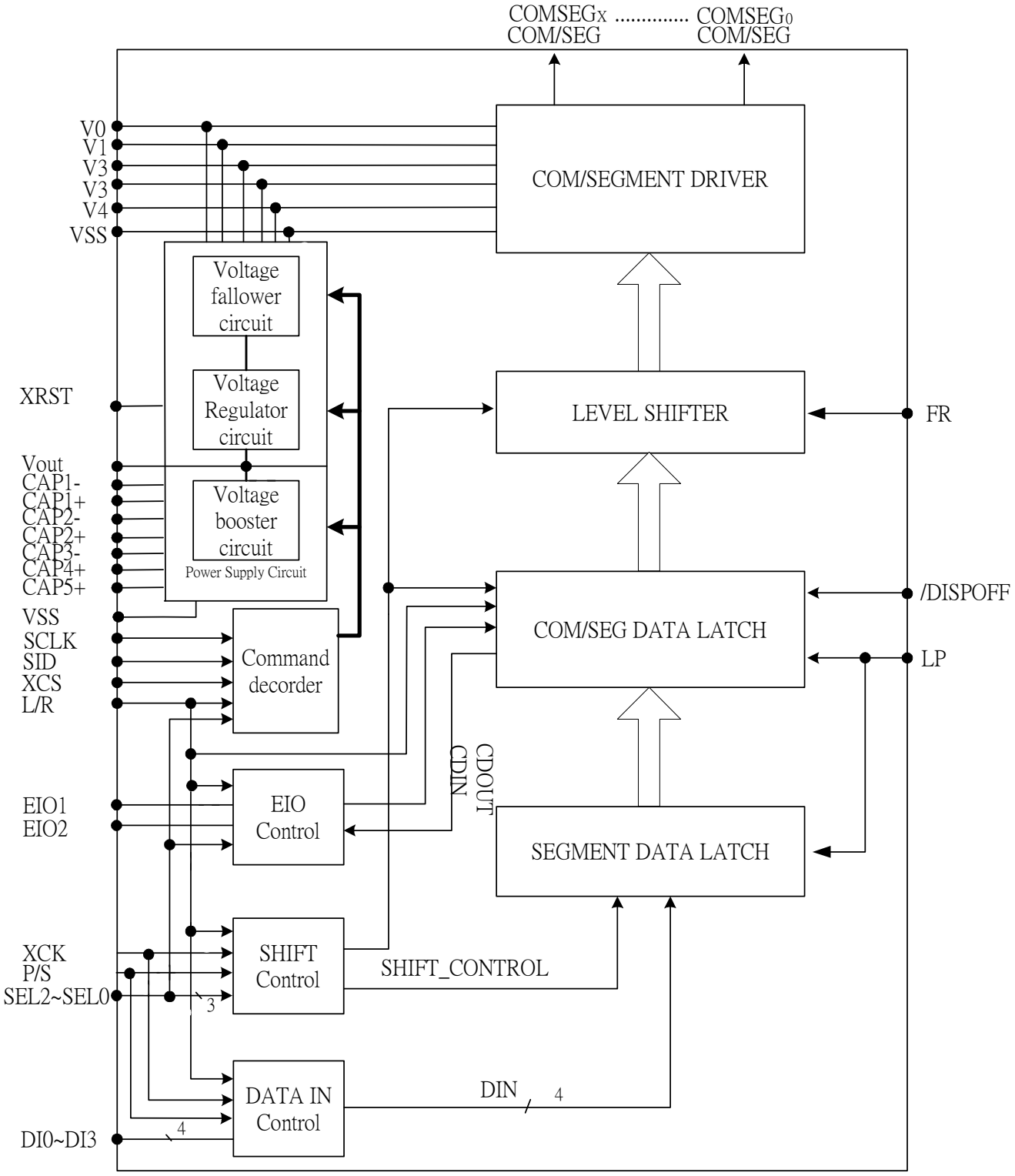
  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when XDISPOFF active

3. PIN DESCRIPTION

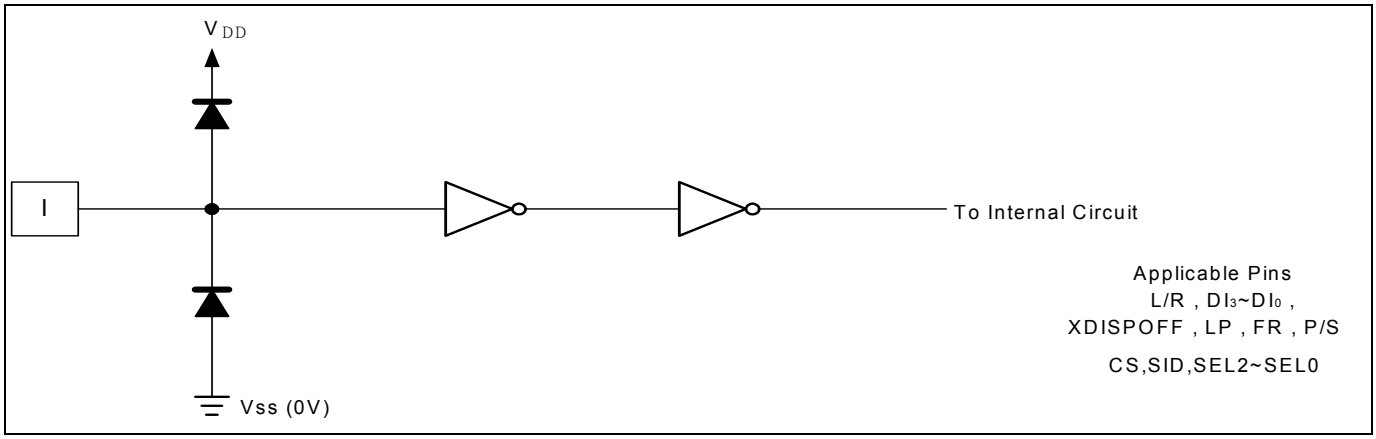
SYMBOL	I/O	DESCRIPTION	No of Num
$COMSEG_0$-$COMSEG_{119}$	O	LCD drive output	120
V_0~V_4	P	Power supply for LCD drive	5
L/R	I	Display data shift direction selection	1
V_{DD}	P	Power supply for logic system (+2.5 to +5.5 V)	1
EIO_2, EIO_1	I/O	Input/output for chip selection at segment mode and FLM input output function at com/seg mix mode or common mode	2
DI_0-DI_3	I	Display data input at segment mode	4
XCK	I	Clock input for taking display data at segment mode	1
XDISPOFF	I	Control input for output of non-select level	1
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode	1
FR	I	AC-converting signal input for LCD drive waveform	1
XRST	I	System Reset pin .When low level active. The XRST L PULSE timing min value is 200us and max value is 0.5s	1
P/S	I	This is the parallel data input/serial data input switch terminal. P/S=”H”: Parallel data input. P/S=”L”: Serial data input.	1
V_{SS}	P	Ground (0 V)	1
CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	1
CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP3+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	1
CAP4+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	1
CAP5+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	1
VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.	1
XCS	I	This is the command mode select pin. When XCS=”L” then write command to the LCD. See Figure1	1

<table>
<tr><td></td><td></td><td>Don’t toggle SCLK or SID from low level while XCS signal is HIGHT</td><td></td></tr>
<tr><td>SID</td><td>I</td><td>The command data. See Figure1</td><td>1</td></tr>
<tr><td>SCLK</td><td>I</td><td>The serial clock input. See Figure1</td><td>1</td></tr>
<tr><td>SEL2~SEL0</td><td>I</td><td>These pin are Duty selection.
<table>
<tr><th>SEL2,SEL1,SEL0</th><th>SEL 3, 2, 1</th><th>DUTY</th><th>BIAS</th></tr>
<tr><td>0 0 0</td><td>0, 0, 0</td><td>---</td><td>Segment mode</td></tr>
<tr><td>0 0 1</td><td>0, 0, 1</td><td>1/32</td><td>1/6 or 1/5</td></tr>
<tr><td>0 1 0</td><td>0, 1, 0</td><td>1/48</td><td>1/7 or 1/5</td></tr>
<tr><td>0 1 1</td><td>0, 1, 1</td><td>1/64</td><td>1/9 or 1/7</td></tr>
<tr><td>1 0 0</td><td>1, 0, 0</td><td>1/80</td><td>1/9 or 1/7</td></tr>
<tr><td>1 0 1</td><td>1, 0, 1</td><td>1/96</td><td>1/10 or 1/8</td></tr>
<tr><td>1 1 0</td><td>1, 1, 0</td><td>1/112</td><td>1/11 or 1/9</td></tr>
<tr><td>1 1 1</td><td>1, 1, 1</td><td>1/120</td><td>1/11 or 1/9</td></tr>
</table></td><td>3</td></tr>
</table>

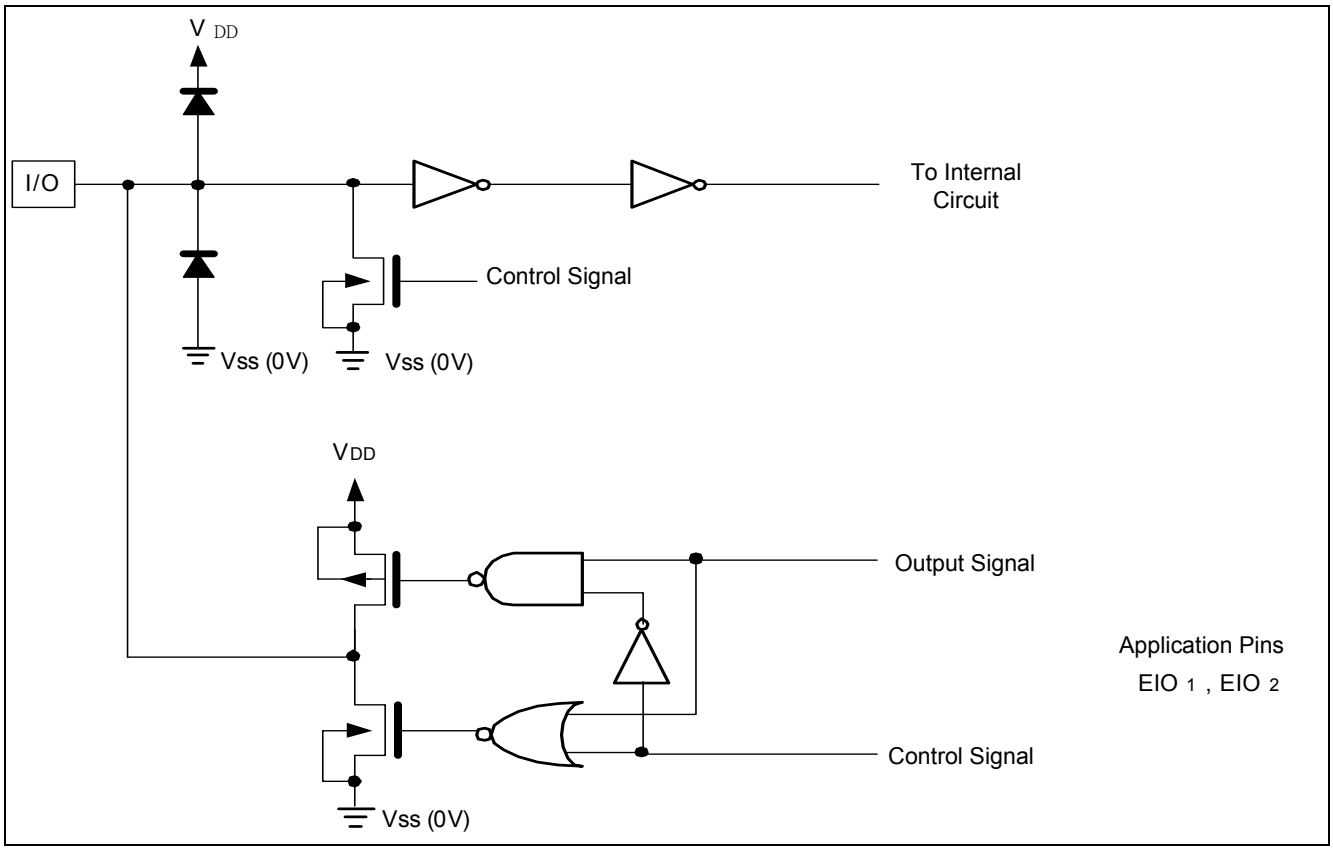
4. BLOCK DIAGRAM



INPUT/OUTPUT CIRCUITS



Input Circuit



Input/Output Circuit

5. FUNCTIONAL DESCRIPTION

5.1 Pin Functions

(Segment mode)

<table>
<tr><th>SYMBOL</th><th>FUNCTION</th></tr>
<tr><td>V_{DD}</td><td>Logic system power supply pin, connected to +2.5 to +5.5 V.</td></tr>
<tr><td>V_{SS}</td><td>Ground pin, connected to 0 V.</td></tr>
<tr><td>V_0 V_1
V_2 V_3
V_4</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VSS, and must maintain the relative magnitudes shown below.
$V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{ss}$
When the power supply turns ON, the internal power supply circuits produce the $V_1$to V_4voltages shown below.
The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/120 Duty</th><th>1/112 Duty</th><th>1/96Duty</th><th>1/80Duty</th><th>1/64Duty</th><th>1/48 Duty</th><th>1/30 Duty</th></tr>
<tr><td>V_4</td><td>1/11*V0 ,1/9*V0</td><td>1/11*V0, 1/9*V0</td><td>1/10*V0, 1/8*V0</td><td>1/9*V0, 1/7*V0</td><td>1/9*V0, 1/7*V0</td><td>1/7*V0, 1/5*V0</td><td>1/6*V0, 1/5*V0</td></tr>
<tr><td>V_3</td><td>2/11*V0,1/9*V0</td><td>2/11*V0, 2/9*V0</td><td>2/10*V0, 2/8*V0</td><td>2/9*V0, 2/7*V0</td><td>2/9*V0, 2/7*V0</td><td>2/7*V0, 2/5*V0</td><td>2/6*V0, 2/5*V0</td></tr>
<tr><td>V_2</td><td>9/11*V0, 7/9*V0</td><td>9/11*V0, 7/9*V0</td><td>8/10*V0, 6/8*V0</td><td>7/9*V0, 5/7*V0</td><td>7/9*V0, 5/7*V0</td><td>5/7*V0, 3/5*V0</td><td>4/6*V0, 3/5*V0</td></tr>
<tr><td>V_1</td><td>10/11*V0,8/9*V0</td><td>10/11*V0,8/9*V0</td><td>9/10*V0, 7/8*V0</td><td>8/9*V0, 6/7*V0</td><td>8/9*V0, 6/7*V0</td><td>6/7*V0, 4/5*V0</td><td>5/6*V0, 4/5*V0</td></tr>
</table>
</td></tr>
<tr><td>DI_3-DI_0</td><td>Input pins for display data
• In 4-bit parallel input mode, input data into the 4 pins, DI_3-DI_0.
• In serial input mode, input data into the 1 pin,DI_0.
Connect DI_3-DI_1 to V_{SS} .
• Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.</td></tr>
<tr><td>XCK</td><td>Clock input pin for taking display data
* Data is read at the falling edge of the clock pulse.</td></tr>
<tr><td>XRST</td><td>System Reset pin .When low level active.
If not used the hardware reset, this pin must pull height.
The XRST L PULSE timing min value is 200us and max value is 0.5s</td></tr>
<tr><td>LP</td><td>Latch pulse input pin for display data
• Data is latched at the falling edge of the clock pulse.</td></tr>
<tr><td>L/R</td><td>Input pin for selecting the reading direction of display data
• When set to V_{SS} level "L", data is read sequentially from $COMSEG_{119}$ to $COMSEG_0$.
• When set to V_{DD} level "H", data is read sequentially from $COMSEG_0$ to $COMSEG_{119}$.
• Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT
• PINS" in Functional Operations.</td></tr>
<tr><td>XDISPOFF</td><td>Control input pin for output of non-select level
• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.</td></tr>
</table>

	• When set to VSS level "L", the LCD drive output pins ($COMSEG_0$-$COMSEG_{119}$) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of XDISPOFF. When the XDISPOFF function is canceled, the driver outputs non-select level (V_2 or V_3), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if XDISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
P/S	Interface Mode selection pin • When P/S is “H” then parallel data input mode. When P/S is “L” the serial data input mode,
EIO_1, EIO_2	Input/output pins for chip selection. AT segment mode: • When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input(connect to Vss). • When L/R input is at V_{DD} level "H", EIO_1 is set for input(connect to Vss), and EIO_2 is set for output. • During output, set to "H" while LP • XCK is "H" and after 120 bits of data have been read, set to "L” for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 120 bits of data have been read.
$COMSEG_0$ –$COMSEG_{119}$	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_2 ,V_3,V_{ss}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP5+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
XCS	This is the command mode select pin. When XCS=”L” then write command to the LCD, when not used the command mode then must fixed to Vdd . See Figure1
SID	The command data, when not used the command mode then must fixed to Vdd. See Figure1
SCLK	The serial clock input, when not used the command mode then must fixed to Vdd. See Figure1

(Common mode)

<table>
<tr><th>SYMBOL</th><th>FUNCTION</th></tr>
<tr><td>V_{DD}</td><td>Logic system power supply pin, connected to +2.5 to +5.5 V.</td></tr>
<tr><td>V_{SS}</td><td>Ground pin, connected to 0 V.</td></tr>
<tr><td>V_0, V_1
V_2, V_3
V_4</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below.
$V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{ss}$
When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><td></td><td>1/120 Duty</td><td>1/112 Duty</td><td>1/96Duty</td><td>1/80Duty</td><td>1/64Duty</td><td>1/48 Duty</td><td>1/30 Duty</td></tr>
<tr><td>V_4</td><td>1/11*V0 ,1/9*V0</td><td>1/11*V0, 1/9*V0</td><td>1/10*V0, 1/8*V0</td><td>1/9*V0, 1/7*V0</td><td>1/9*V0, 1/7*V0</td><td>1/7*V0, 1/5*V0</td><td>1/6*V0, 1/5*V0</td></tr>
<tr><td>V_3</td><td>2/11*V0,1/9*V0</td><td>2/11*V0, 2/9*V0</td><td>2/10*V0, 2/8*V0</td><td>2/9*V0, 2/7*V0</td><td>2/9*V0, 2/7*V0</td><td>2/7*V0, 2/5*V0</td><td>2/6*V0, 2/5*V0</td></tr>
<tr><td>V_2</td><td>9/11*V0, 7/9*V0</td><td>9/11*V0, 7/9*V0</td><td>8/10*V0, 6/8*V0</td><td>7/9*V0, 5/7*V0</td><td>7/9*V0, 5/7*V0</td><td>5/7*V0, 3/5*V0</td><td>4/6*V0, 3/5*V0</td></tr>
<tr><td>V_1</td><td>10/11*V0,8/9*V0</td><td>10/11*V0,8/9*V0</td><td>9/10*V0, 7/8*V0</td><td>8/9*V0, 6/7*V0</td><td>8/9*V0, 6/7*V0</td><td>6/7*V0, 4/5*V0</td><td>5/6*V0, 4/5*V0</td></tr>
</table></td></tr>
<tr><td>LP</td><td>Shift clock pulse input pin for bi-directional shift register
• * Data is shifted at the falling edge of the clock pulse.</td></tr>
<tr><td>XRST</td><td>System Reset pin .When low level active.
If not used the hardware reset, this pin must pull height.
The XRST L PULSE timing min value is 200us and max value is 0.5s</td></tr>
<tr><td>L/R</td><td>Input pin for selecting the shift direction of bi-directional shift register
• Data is shifted from $COMSEG_{119}$ to $COMSEG_0$ when set to V_{SS} level "L", and data is shifted from $COMSEG_0$ to $COMSEG_{119}$ when set to V_{DD} level "H".
• Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.</td></tr>
<tr><td>XDISPOFF</td><td>Control input pin for output of non-select level
• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.
• When set to V_{SS} level "L", the LCD drive output pins ($COMSEG_0$-$COMSEG_x$) are set to level Vss.
• When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_1 or V_4), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly.
• Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.</td></tr>
<tr><td>FR</td><td>AC signal input pin for LCD drive waveform
• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.</td></tr>
</table>

	• Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
DI_3-DI_0	Not used • Connect DI_3-DI_0 to V_{SS}, not floating.
XCK	Not used • XCK is pulled down in common mode, so connect to V_{SS} .
$COMSEG_0$ -$COMSEG_{119}$	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0 V_1, V_4, or V_{SS}) is selected and output. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
EIO_1, EIO_2	Shift data Input/output pins for shift register • EIO_1 is output pin when L/R is at Vss level “L”, EIO_1 is input pin when L/R is at Vdd level “H” • When L/R=H, EIO_1 is used as input pin, it will be connect to FLM. • When L/R=L, EIO_1 is used as output pin, it won’t be connect to FLM. • EIO_2 is input pin when L/R is at Vss level “L”, EIO_1 is output pin when L/R is at Vdd level “H” • When L/R=H, EIO_2 is used as output pin, it won’t be connect to FLM, • When L/R=L, EIO_2 is used as input pin, it will be connect to FLM • Refer to “RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS” in Functional Operations.
CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP3+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
CAP4+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
CAP5+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
XCS	This is the command mode select pin. When XCS=”L” then write command to the LCD, when not used the command mode then must fixed to Vdd . See Figure1
SID	The command data, when not used the command mode then must fixed to Vdd. See Figure1
SCLK	The serial clock input, when not used the command mode then must fixed to Vdd. See Figure1

(common /segment mix mode)

EIO_1, EIO_2	Input/output pins for chip selection AT common/segment mode: • When L/R input is at Vss level “L”, EIO_1 is set output, and EIO_2 is set for input. EIO_1 : segment chip enable output, as default segment is enabled internally and be non-selected after 8,24,40,56,72 or 88 bits of data have been read. Depend on select mode. EIO_2 :common shift data input, no sift data output • When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. EIO_1 :common shift data, no shift data output EIO_2 : segment chip enable output, as default segment is enabled internally and be non-selected after 8,24,40,56,72 or 88 bits of data have been read. Depend on select mode. • During output, set to "H" while LP • XCK is "H" and after 120 bits of data have been read, set to "L” for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 120 bits of data have been read.

5.2 Functional Operations

TRUTH TABLE

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (COMSEG0-COMSEG119)
L	L	H	V_3
L	H	H	V_{ss}
H	L	H	V_2
H	H	H	V_0
X	X	L	V_{ss}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (COMSEG0-COMSEG119)
L	L	H	V_4
L	H	H	V_0
H	L	H	V_1
H	H	H	V_{ss}
X	X	L	V_{ss}

NOTES:

- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.

  Supply regular voltage that is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(Segment Mode)

(A) 4-bit Parallel Input Mode

L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
				30 CLOCK	29 CLOCK	28 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI_0	$COMSEG_0$	$COMSEG_4$	$COMSEG_8$	…	$COMSEG_{108}$	$COMSEG_{112}$	$COMSEG_{116}$
			DI_1	$COMSEG_1$	$COMSEG_5$	$COMSEG_9$	…	$COMSEG_{109}$	$COMSEG_{113}$	$COMSEG_{117}$
			DI_2	$COMSEG_2$	$COMSEG_6$	$COMSEG_{10}$	…	$COMSEG_{110}$	$COMSEG_{114}$	$COMSEG_{118}$
			DI_3	$COMSEG_3$	$COMSEG_7$	$COMSEG_{11}$	…	$COMSEG_{111}$	$COMSEG_{115}$	$COMSEG_{119}$
H	Input	Output	DI_0	$COMSEG_{119}$	$COMSEG_{115}$	$COMSEG_{111}$	…	$COMSEG_{11}$	$COMSEG_7$	$COMSEG_3$
			DI_1	$COMSEG_{118}$	$COMSEG_{114}$	$COMSEG_{110}$	…	$COMSEG_{10}$	$COMSEG_6$	$COMSEG_2$
			DI_2	$COMSEG_{117}$	$COMSEG_{113}$	$COMSEG_{109}$	…	$COMSEG_9$	$COMSEG_5$	$COMSEG_1$
			DI_3	$COMSEG_{116}$	$COMSEG_{112}$	$COMSEG_{108}$	…	$COMSEG_8$	$COMSEG_4$	$COMSEG_0$

(B) Serial Input Mode

L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
				120 CLOCK	119 CLOCK	118 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Output	Input	DI_0	$COMSEG_0$	$COMSEG_1$	$COMSEG_2$	…	$COMSEG_{117}$	$COMSEG_{118}$	$COMSEG_{119}$
			DI_1	X	X	X	X	X	X	X
			DI_2	X	X	X	X	X	X	X
			DI_3	X	X	X	X	X	X	X
H	Input	Output	DI_0	$COMSEG_{119}$	$COMSEG_{118}$	$COMSEG_{117}$	…	$COMSEG_2$	$COMSEG_1$	$COMSEG_0$
			DI_1	X	X	X	X	X	X	X
			DI_2	X	X	X	X	X	X	X
			DI_3	X	X	X	X	X	X	X

(Common Mode)

L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2
L	$COMSEG_{119}$ → $COMSEG_0$	Output	Input
H	$COMSEG_0$ → $COMSEG_{119}$	Input	Output

MIX MODE(SEGMENT/ COMMON MODE)

When (SEL2,SEL1,SEL0)=(0,0,1)➔ SELECT THE 32 COM/88 SEGMENT MODE

THEN SEGMENT SIDE OF MIX MODE

(a) 4-bit Parallel Input Mode

L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
				22 CLOCK	21 CLOCK	20 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Seg_end Output	Com_FLM Input	DI_0	$COMSEG_0$	$COMSEG_4$	$COMSEG_8$	…	$COMSEG_{76}$	$COMSEG_{80}$	$COMSEG_{84}$
			DI_1	$COMSEG_1$	$COMSEG_5$	$COMSEG_9$	…	$COMSEG_{77}$	$COMSEG_{81}$	$COMSEG_{85}$
			DI_2	$COMSEG_2$	$COMSEG_6$	$COMSEG_{10}$	…	$COMSEG_{78}$	$COMSEG_{82}$	$COMSEG_{86}$
			DI_3	$COMSEG_3$	$COMSEG_7$	$COMSEG_{11}$	…	$COMSEG_{79}$	$COMSEG_{83}$	$COMSEG_{87}$
H	Com_FLM Input	Seg_end Output	DI_0	$COMSEG_{119}$	$COMSEG_{115}$	$COMSEG_{110}$	…	$COMSEG_{43}$	$COMSEG_{39}$	$COMSEG_{35}$
			DI_1	$COMSEG_{118}$	$COMSEG_{114}$	$COMSEG_{109}$	…	$COMSEG_{42}$	$COMSEG_{38}$	$COMSEG_{34}$
			DI_2	$COMSEG_{117}$	$COMSEG_{113}$	$COMSEG_{108}$	…	$COMSEG_{41}$	$COMSEG_{37}$	$COMSEG_{33}$
			DI_3	$COMSEG_{116}$	$COMSEG_{112}$	$COMSEG_{107}$	…	$COMSEG_{40}$	$COMSEG_{36}$	$COMSEG_{32}$

(b) Serial Input Mode

L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
				88 CLOCK	87 CLOCK	86 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	Seg_end Output	Com_FLM Input	DI_0	$COMSEG_0$	$COMSEG_1$	$COMSEG_2$	…	$COMSEG_{85}$	$COMSEG_{86}$	$COMSEG_{87}$
			DI_1	X	X	X	X	X	X	X
			DI_2	X	X	X	X	X	X	X
			DI_3	X	X	X	X	X	X	X
H	Com_FLM Input	Seg_end Output	DI_0	$COMSEG_{119}$	$COMSEG_{118}$	$COMSEG_{117}$	…	$COMSEG_{34}$	$COMSEG_{33}$	$COMSEG_{32}$
			DI_1	X	X	X	X	X	X	X
			DI_2	X	X	X	X	X	X	X
			DI_3	X	X	X	X	X	X	X

COMMON SIDE OF MIX MODE

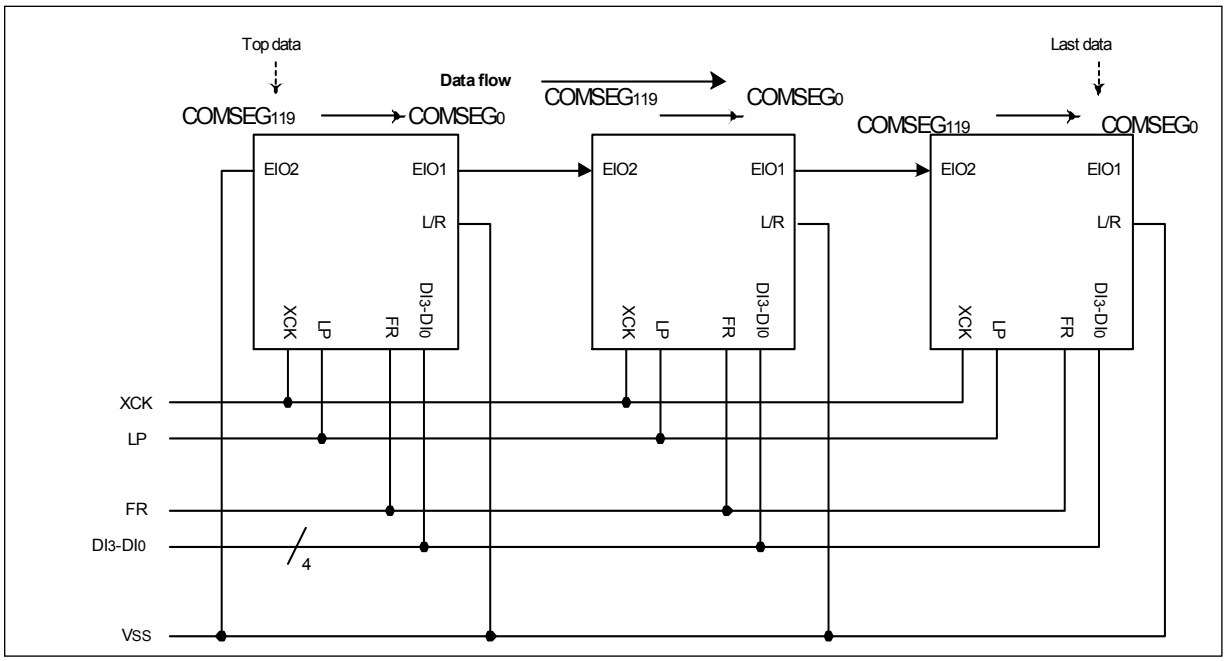
L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2
L	$COMSEG_{119}$ → $COMSEG_{88}$	Seg_end output	Input
H	$COMSEG_0$ → $COMSEG_{31}$	Input	Seg_end output

NOTES:

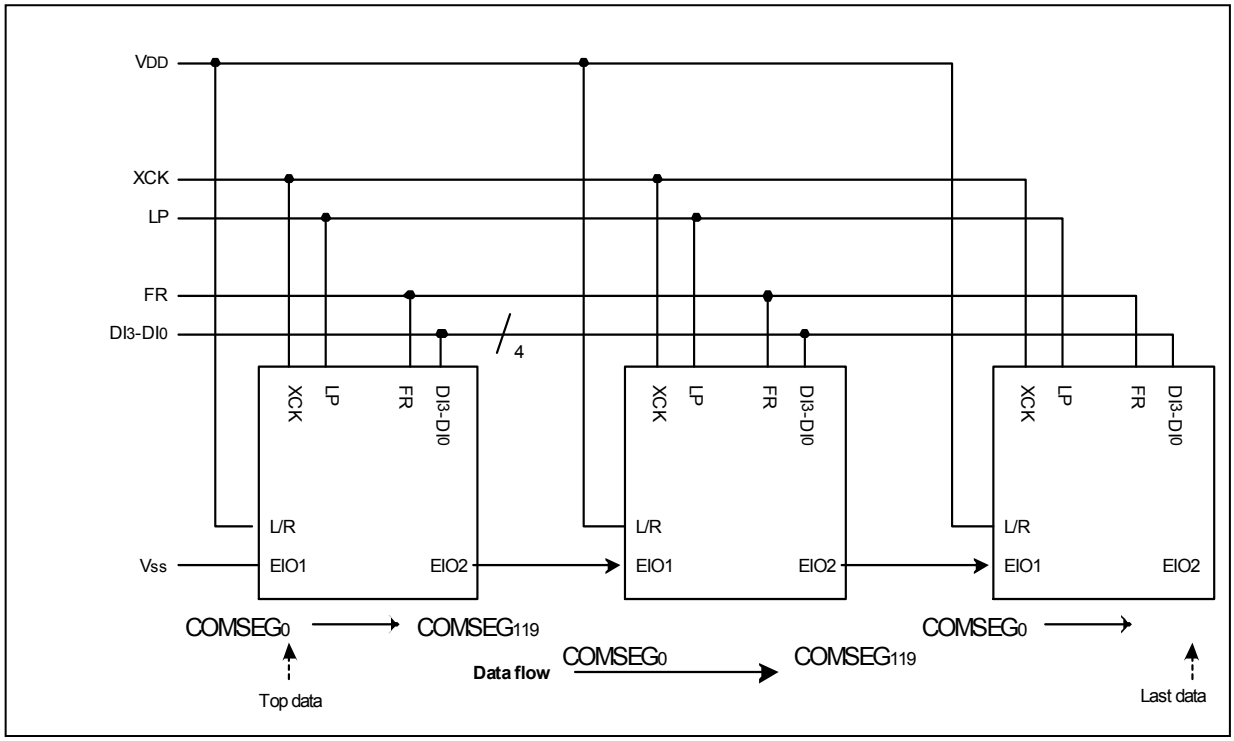
- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

Connection examples of plural segment drivers (120 segment)

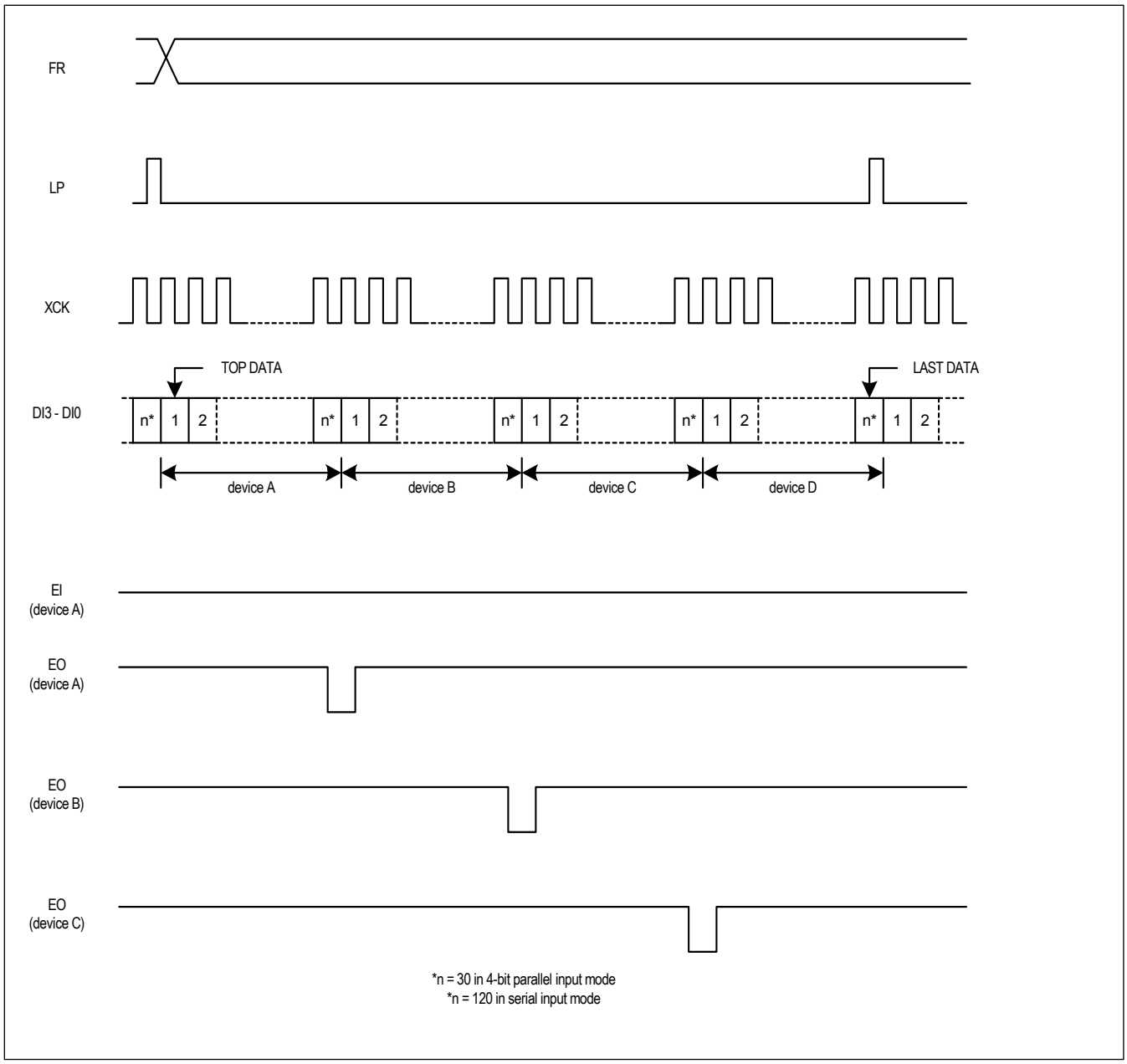
(c) When L/R = "L"



(d) When L/R = "H"

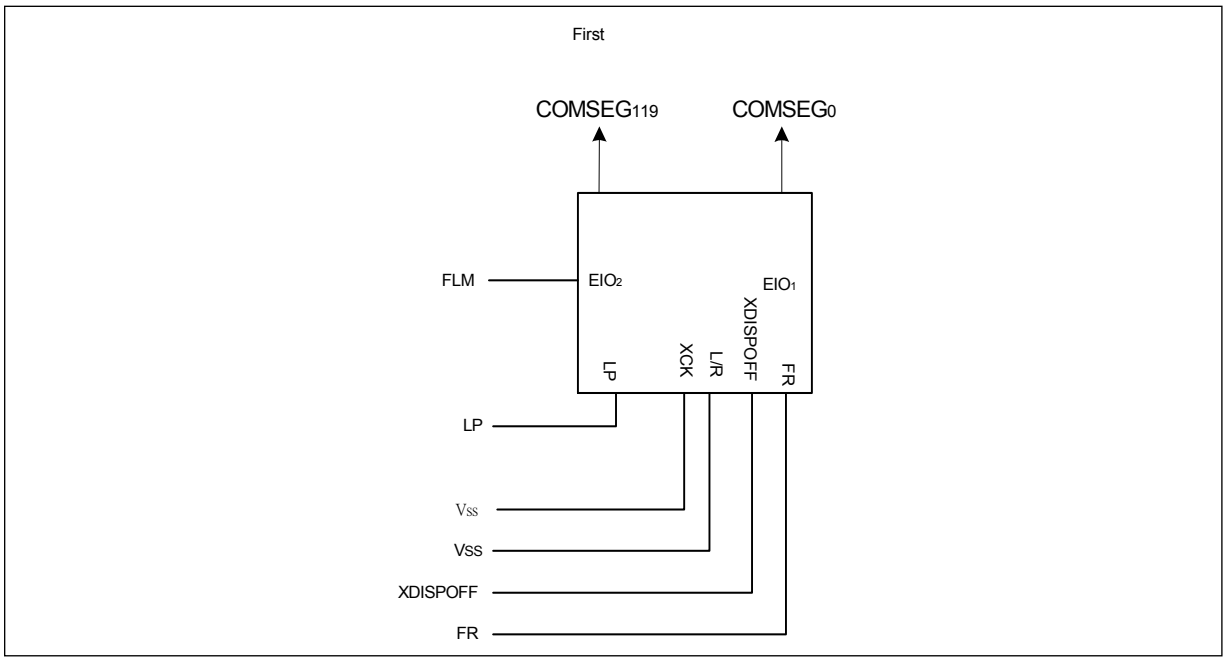


Timing chart of 4-device cascade connection of segment drivers

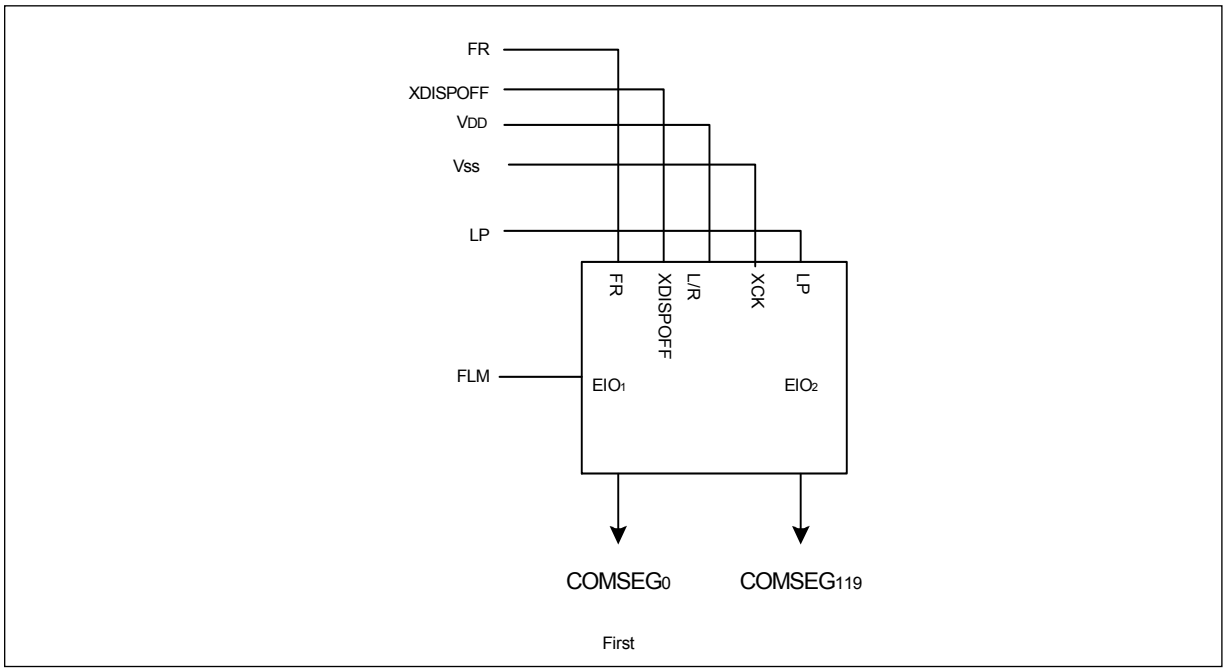


Connection examples for signal common drivers (120 common)

(e) L/R = ”L”



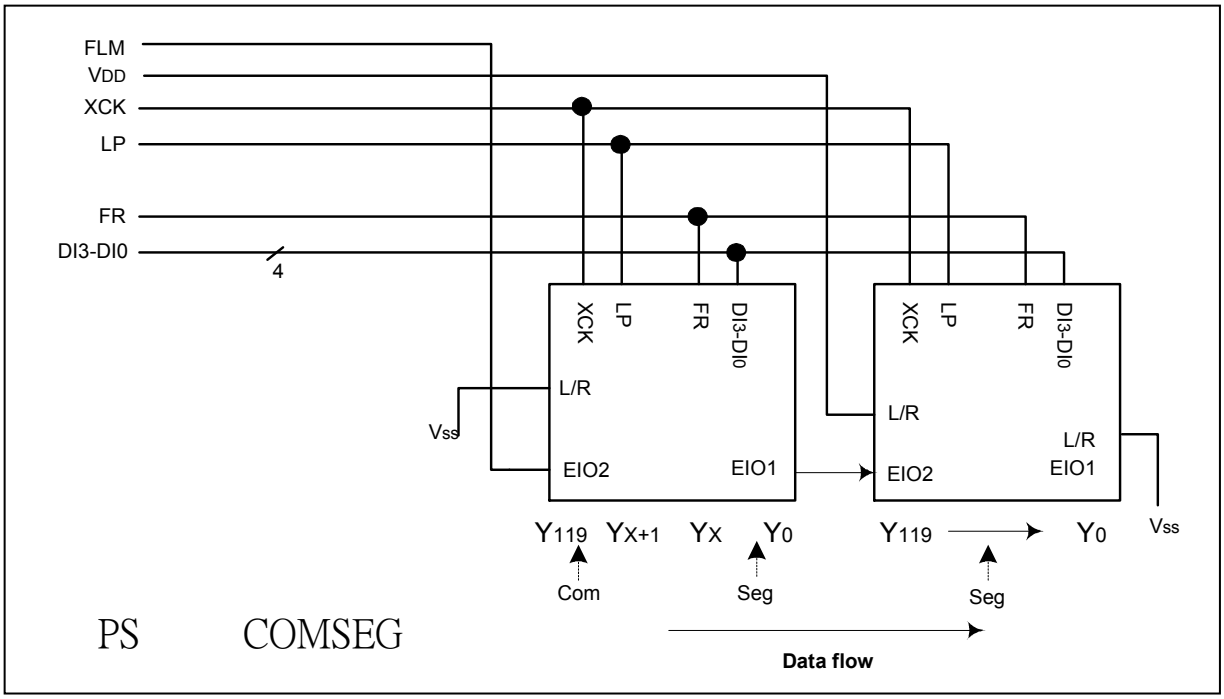
(f) L/R = “H”



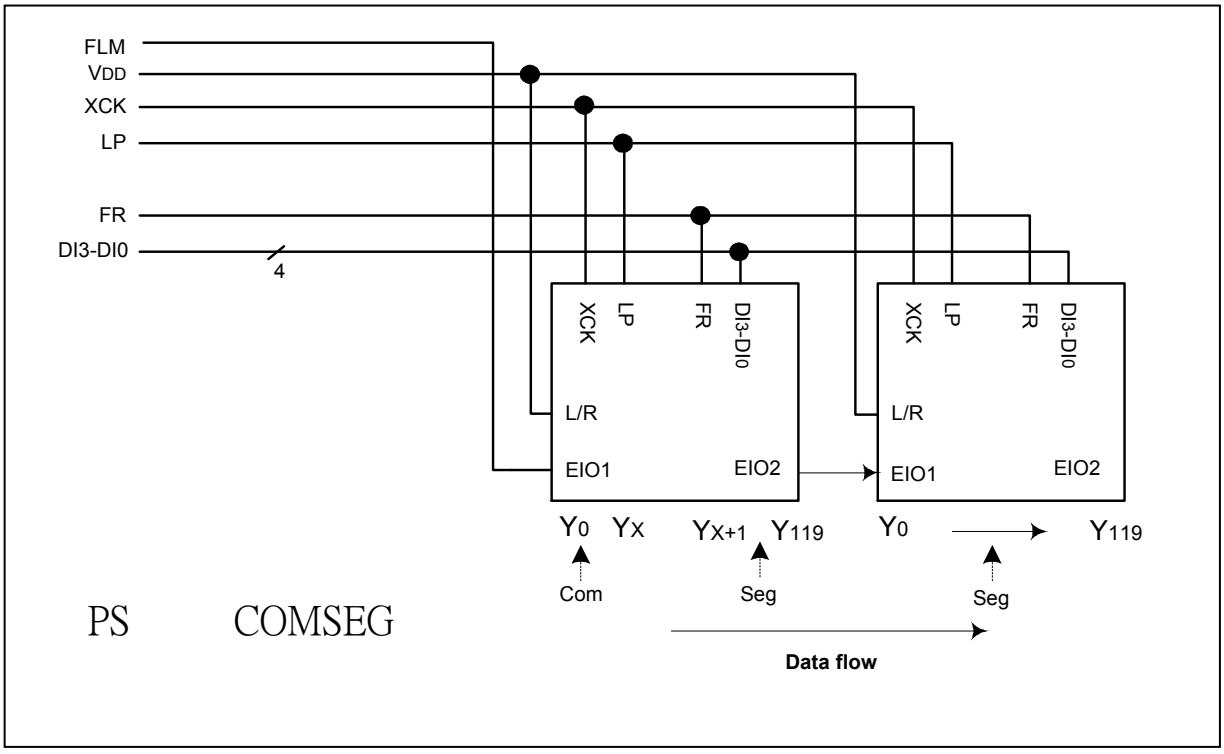
Connection examples for plural common/segment (mix mode) drivers

The mix mode is 1/32,1/48,1/64,1/80,1/96,1/112 duty mode

(g) L/R = "L"

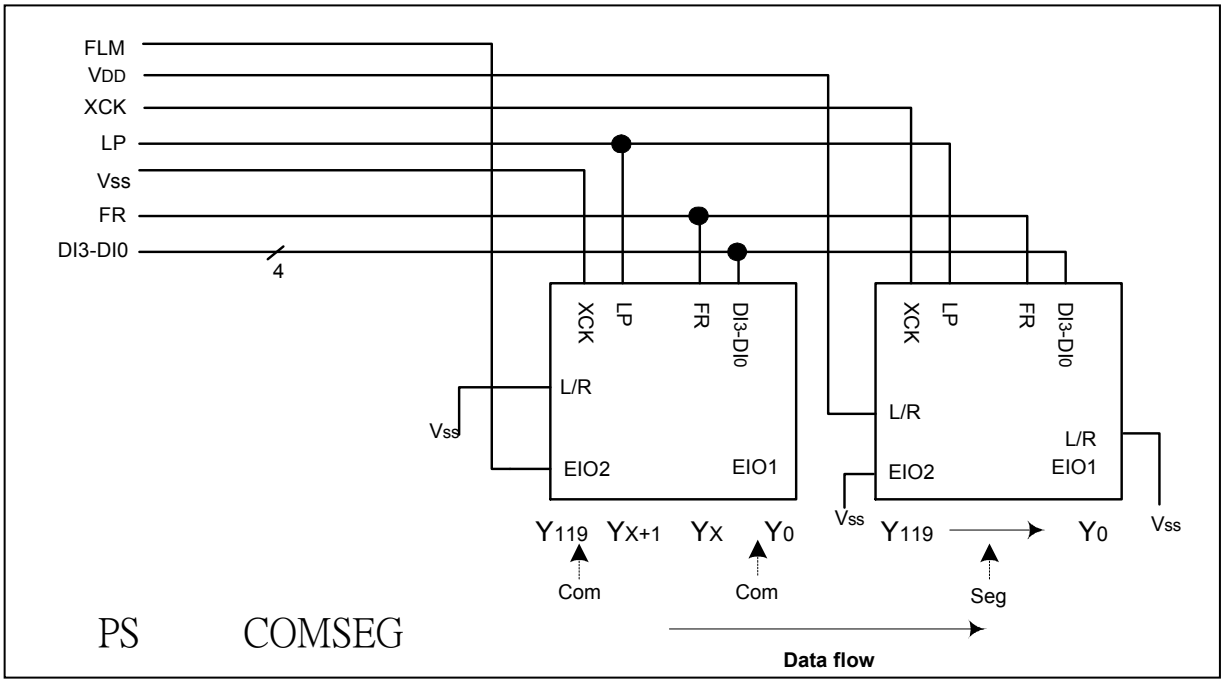


(h) L/R="H"

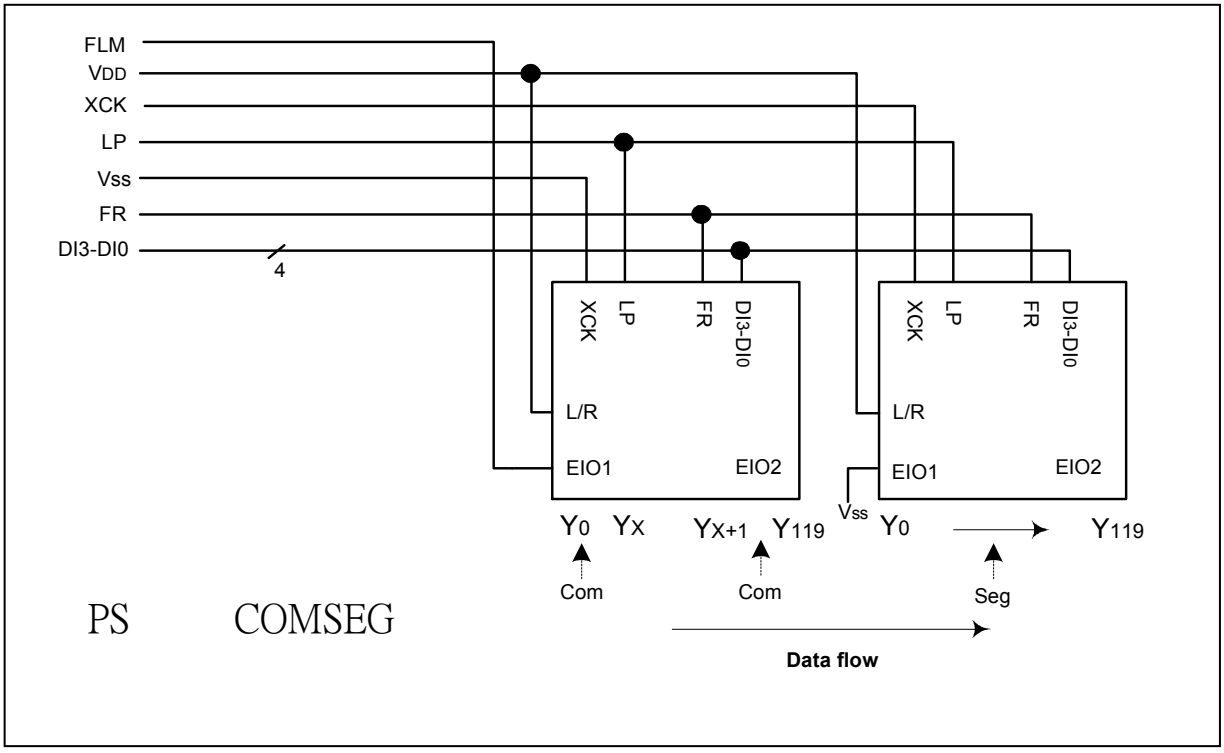


Connection examples for 120 com &120 seg (for 1/120 duty)

(i) L/R = "L"



(j) L/R = "H"



PRECAUTIONS

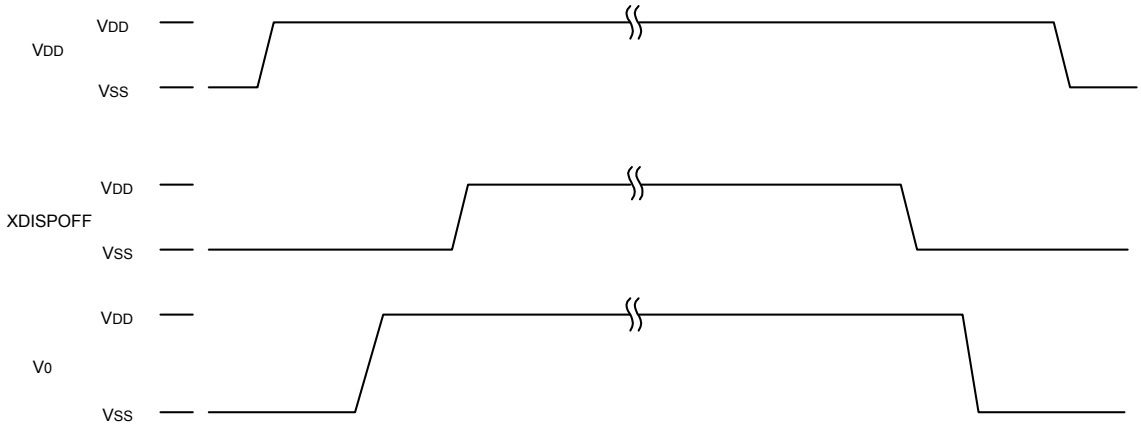
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level Vss on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here



6. DESCRIPTION FUNCTIONS

The MPU Interface

Selecting the Interface Type

With the ST8012 chips, data transfers are done through an 4-bit parallel data bus (D3 to D0) or through a serial data input (SI). Through selecting the P/S terminal polarity to the “H” or “L” it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

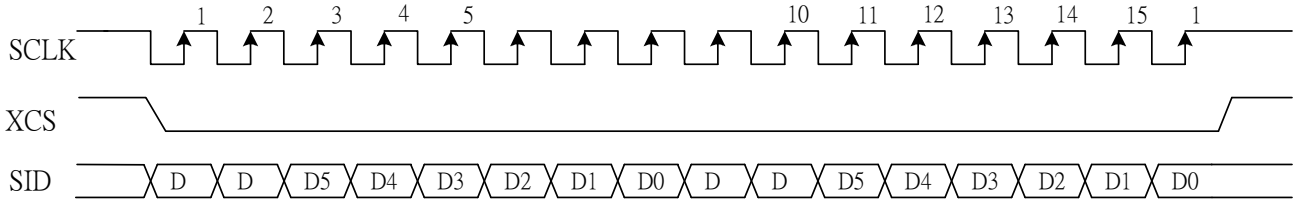
P/S	D_0	D_3~D_1
H: Parallel Input	D_0	D_3~D_1
L: Serial Input	SI	VDD

Command Serial Interface

With the ST8012 chips, command data transfers are done through a serial data input. And it’s timing show in Figure1.

Figure1

rite command timing diagram



ps :when don’t use the command must set XCS to height level.

The Power Supply Circuits (use serial interface)

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation, when the mode is in common mode or common/segment mode. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 3 shows the Power Control Set Command 3-bit data control function, and Table 4 shows reference combinations.

Table3

bit	Function	Status	
		“111”	“000”
D2 D1 D0	Booster circuit control bit	ON	OFF

The Control Details of Each Bit of the Power Control Set Command

Table4

Use Settings	Com / Seg	D2	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Step-up voltage
Only the internal power supply is used	Com mode / Com/Seg mode	1	ON	ON	ON	VDD	Used
Only the voltage regulator circuit and the voltage follower circuit are used		0	OFF	ON	ON	VOUT, VDD	Open
Only the internal power supply is used	Seg mode	1	ON	ON	ON	VDD	Used
Only the voltage regulator circuit and the voltage follower circuit are used		0	OFF	ON	ON	VOUT, VDD	Open

Command interface unused mode (use the default value)

When command interface is unused. The CS,SCLK and SID signal can be fixed as the following mode

Table5

XCS	SCLK	SID	Booster	Regulator	Follower
H	X	X	Default register used (All Off)		
L	H	H	OFF	ON	ON
L	L	H	ON	ON	ON

THE DEFAULT BIAS,CONTRAST CONTROL,Ra/Rb ratio and Boost Frequency is used when the above mode is selected.

NOTE :If all of the Cs, SCLK and SID signals are set to low level. The default power control register will be used, the power control of booster, regulator and follower will always be off.

PROGRAM NOTE: Do not toggle sclk or SID from low level while XCS signal is HIGHT.

Entry Standby mode: Entry standby must closed the AC circuit(BOOSTER) and /XDISPOFF also go to low level.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the ST8012 chips it is possible to product a 2X, 3X, 4X, 5X or 6X step-up of the V_{DD} – V_{SS} voltage levels.

6X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, between CAP2+ and CAP4–,between CAP1+ and CAP5–, and between V_{DD} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 6 times the voltage level between V_{DD} and V_{SS}.

5X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, between CAP2+ and CAP4–,and between V_{DD} and V_{OUT}, to produce a voltage level in the negative direction at the VOUT terminal that is 5 times the voltage level between V_{DD} and V_{SS}.

4X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and between V_{DD} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and V_{SS}.

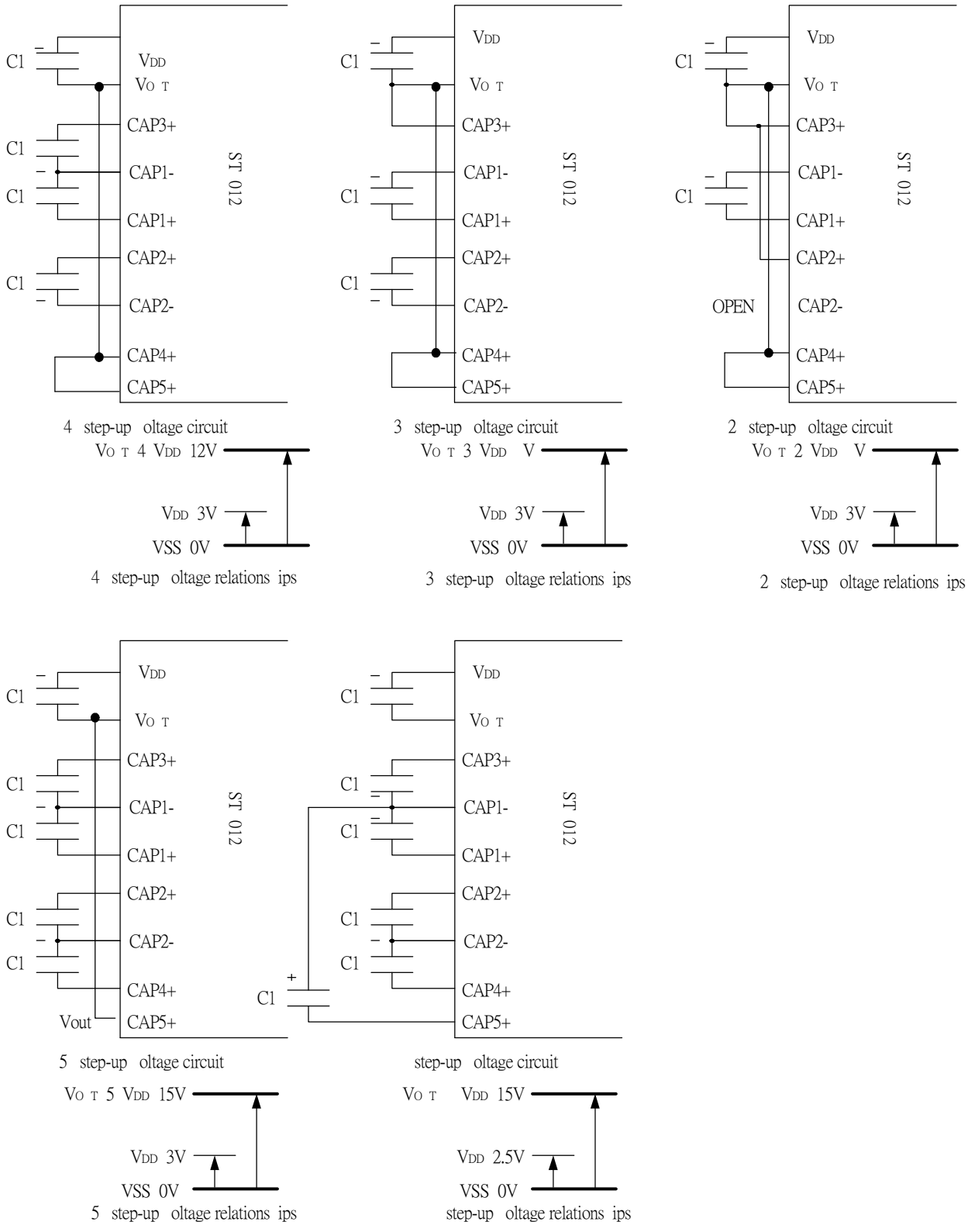
3X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between V_{DD} and V_{OUT},and short between CAP3– and V_{OUT} to produce a voltage level in the negative direction at the V_{OUT} terminal that is 3 times the voltage difference between V_{DD} and V_{SS}. The step-up voltage relationships are shown in Figure2.

2X step-up:

Connect capacitor C1 between CAP1+ and CAP1–, and between V_{DD} and V_{OUT}, leave CAP2+ open, and short between CAP2–, CAP3– and V_{OUT} to produce a voltage in the negative direction at the V_{OUT} terminal that Is twice the voltage between V_{DD} and V_{SS}.

Figure2



* The V_{SS} voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.

The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V0 through the voltage regulator circuit. Because the ST78012 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.(VREG thermal gradients approximate -0.05%/°C)

(A) When the V0 Voltage Regulator Internal Resistors Are Used

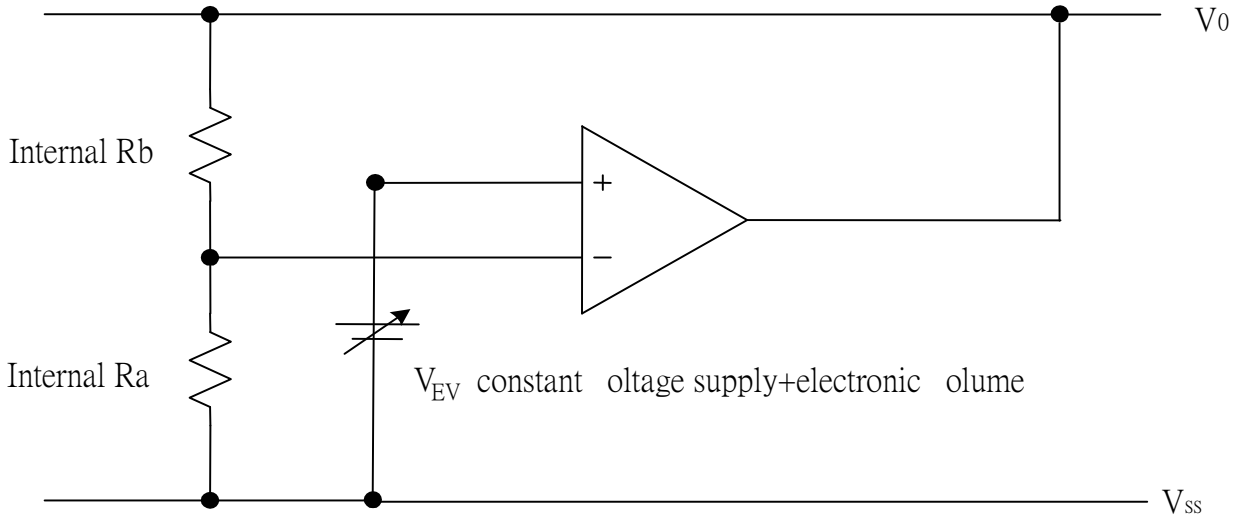
Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where | V0 | < | VOUT|.

Figure 3

$$V_0 \quad 1 + \frac{Rb}{Ra} \bullet V_{EV}$$

$$1 + \frac{Rb}{Ra} \bullet 1 - \frac{\alpha}{200} \bullet V_{REG}$$

$$\because V_{EV} \quad 1 - \frac{\alpha}{200} \bullet V_{REG}$$



VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 6.

Table6

Part no.	Equipment Type	Thermal Gradient	V_{REG}
ST8012	Internal Power Supply	–0.05 %/°C	2.1V

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronicvolume register. Table 6 shows the value for α depending on the electronic volume register settings.

Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The Rb/Ra ratio assumes the values shown in Table 8 depending on the 3-bit data settings in the VDD voltage regulator internal resistor ratio register.

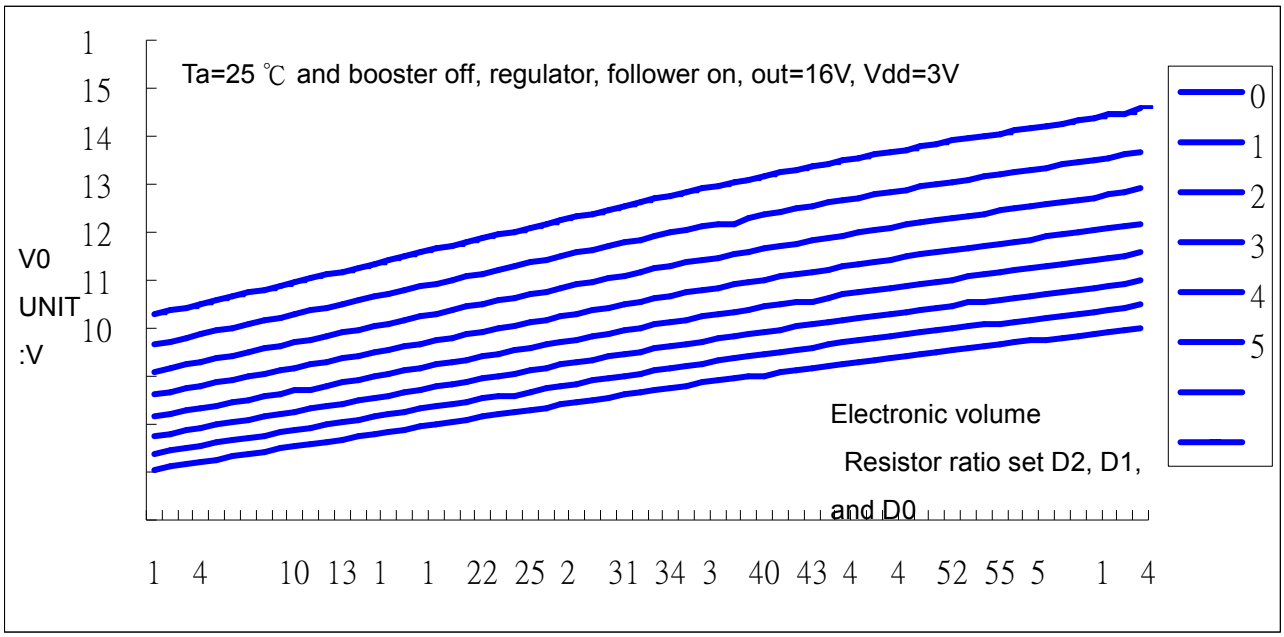
Table7

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V_0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table8

Register			ST8012
D2	D1	D0	(1) –0.05 %/°C
0	0	0	5.0
0	0	1	5.22
0	1	0	5.48
0	1	1	5.76
1	0	0	6.07
1	0	1	6.42
1	1	0	6.81
1	1	1	7.25



The LCD Voltage Generator Circuit

The V_0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit.

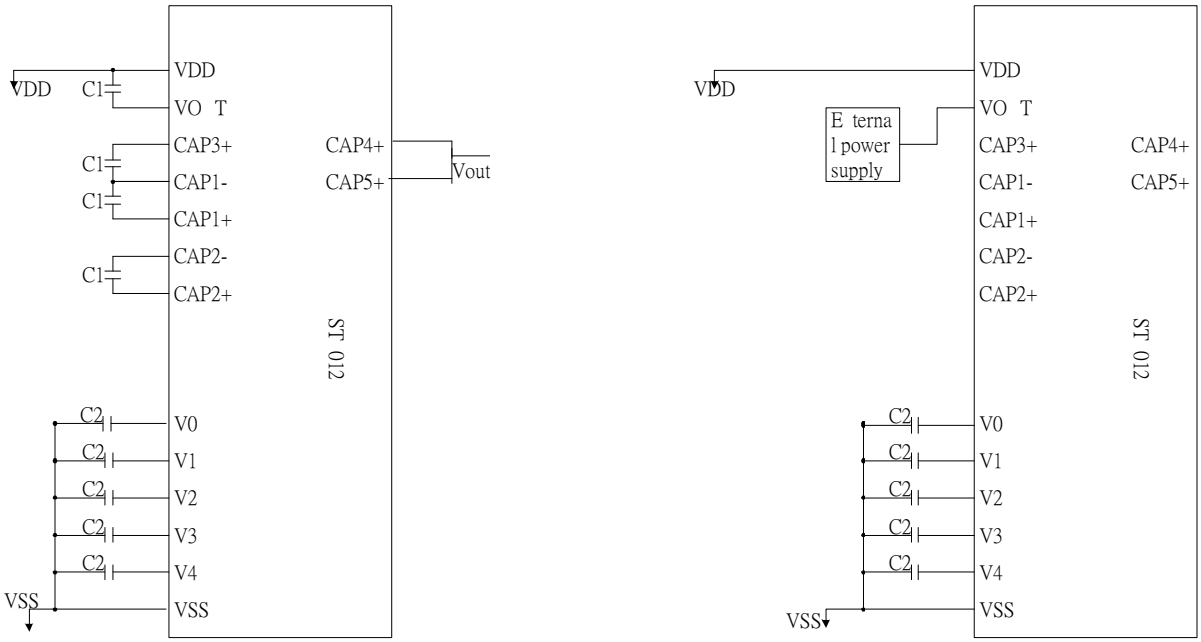
Reference Circuit Examples

Figure 5 shows reference circuit examples.

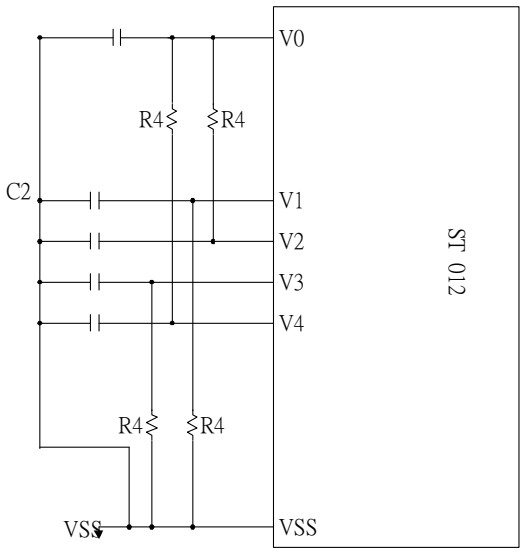
1.When used all of the step-up circuit, voltage regulating circuit and V/F circuit.
(Example with 4x setup-up)

2.When the voltage regulator circuit and V/F circuit alone are used

Figure 4



3.When the built-in power circuit is used to drive a liquid crystal panel heavily loaded with AC or DC, it is recommended to connect an external resistor to stabilize potentials of V_1, V_2, V_3 and V_4 which are output from the built-in voltage follower. Examples of shared reference settings When V_0 can vary between –8 and 12 V



Item	Set value	units
c1	1.0 to 4.7	uF
c2	0.1 to 4.7	uF

C1 and C2 are determined by the size of the LCD being driven

Reference set value R4:100K Ω ~ 1M Ω it is recommended to set an optimum resistance value R4 taking the liquid crystal display and the drive wveform

* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.
* 2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

• Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to V_{OUT} from the outside.
• Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V_1 to V_4). Note that all C2 capacitors must have the same capacitance value.
• Next turn all the power supplies ON and determine C1.

COMMANDS

The ST8012 identify the data bus signals by a combination of XCS, SDI, and SCLK signals.

<Example of Commands>

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

The D3 can select the Frame direction , if select '0' is normal else select '1' is reverse.

								Select Status						
D7	D6	D5	D4	D3	D2	D1	D0	1/120duty	1/112duty	1/96duty	1/80duty	1/64duty	1/48duty	1/32duty
0	0	0	0	0	X	X	0	1/11 bias	1/11 bias	1/10 bias	1/9 bias	1/9 bias	1/7 bias	1/6 bias
							1	1/9 bias	1/9 bias	1/8 bias	1/7 bias	1/7 bias	1/5 bias	1/5 bias
0	0	0	0	1	X	X	0	1/11 bias	1/11 bias	1/10 bias	1/9 bias	1/9 bias	1/7 bias	1/6 bias
							1	1/9 bias	1/9 bias	1/8 bias	1/7 bias	1/7 bias	1/5 bias	1/5 bias

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	0	1	0	X	0	0	0	Booster circuit: OFF
					1	1	1	Booster circuit: ON

V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see the function explanation is "The Voltage Regulator circuit " and table 7 .

D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	X	0	0	0	Small
					0	0	1	
					0	1	0	
						↓		↓
					1	1	0	
					1	1	1	Large

The Electronic Volume

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply.

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V5 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the

electronic volume register has been set.

D7	D6	D5	D4	D3	D2	D1	D0	|VSS|
1	1	0	0	0	0	0	0	Small
1	1	0	0	0	0	1	0	
1	1	0	0	0	0	1	1	
			↓					↓
1	1	1	1	1	1	1	0	
1	1	1	1	1	1	1	1	Large

Booster Frequency Set

By using this command to set three bits of data to the booster frequency, the liquid crystal drive Booster Frequency assumes one of the 8 frequencies. When this command is input, the booster frequency register has been set.

D7	D6	D5	D4	D3	D2	D1	D0	Booster Frequency
0	1	1	0	X	0	0	0	Small
0	1	1	0	X	0	0	1	
0	1	1	0	X	0	1	0	
0	1	1	0	X	0	1	1	
0	1	1	0	X	1	0	0	
0	1	1	0	X	1	0	1	
0	1	1	0	X	1	1	0	
0	1	1	0	X	1	1	1	Large

The default value of ST8012

When select common mode or common/segment mode the Bias、Contrast control、Ra/Rb Ratio and Booster Frequency all have the default value, if user don't not used programmable to setting the status can used the default value.

SEL 3, 2, 1	DUTY	BIAS	Contrast control	Ra/Rb Ratio	Booster Frequency
0, 0, 0	---	Segment mode	---	---	---
0, 0, 1	1/32	1/6	32	4	5k
0, 1, 0	1/48	1/7	32	4	5k
0, 1, 1	1/64	1/9	32	4	5k
1, 0, 0	1/80	1/9	32	4	5k
1, 0, 1	1/96	1/10	32	4	5k
1, 1, 0	1/112	1/11	32	4	5k
1, 1, 1	1/120	1/11	32	4	5k

TABLE OF ST8012 COMMAND

Command	Command Code								Function
	D7	D6	D5	D4	D3	D2	D1	D0	
LCD bias set	0	0	0	0	0	X	X	0	D0Sets the LCD drive voltage bias ratio.0: 1/6 bias, 1: 1/5 bias (ST8012) D3 select frame direction.0:normal,1:reverse
					1			1	
Power control set	0	0	1	0	X	Power control set			Select internal power supply operating mode
VSS voltage regulator internal resistor ratio set	0	1	0	0	X	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
Electronic volume mode set Electronic volume register set	1	1	Electronic volume value						Set the V0 output voltage electronic volume register
Booster Frequency Set	0	1	1	0	X	Booster Frequency			Set the LCD booster frequency

7. BSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3~+5.5	V	1,2
Supply voltage (2)	V_1	V_1	V_{DD+}10~ V_{DD-}0.3	V	
	V_2	V_2	V_{DD+}10~ V_{DD-}0.3		
	V_3	V_3	-0.3~V_{5S}+10	V	
	V_4	V_4	-0.3~V_{5S}+10	V	
Input voltage	V_I	$D1_4$-DI_0, XCK, LP, L/R, FR, EIO_1, EIO_2,XDISPOFF,	-0.3 to V_{DD}+0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:

1. TA = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

8. RECOMMENDED OPERATING Conditions

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	VDD	VDD	+2.5		+5.5	V	1, 2
Supply voltage (2)	V0	V0	+6.0		+16.0	V	
Operating temperature	TOPR		-20		+85	℃	

9. ELECTRICAL CHARACTERISTICS

DC Characteristics

(Segment Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +3.6 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI3-DI0, XCK, LP, L/R FR, EIO_1, EIO_2,XDISPOFF			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI3-DI0, XCK, LP, LIR, FR, EIO_1, EIO_2, XDISPOFF			-10	µA	
	I_{LIH}	$V_I = V_{DD}$				+10	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0 = 15 V	Y_1-Y_{120}		1.5	2.0	kΩ	
Standby current	I_{STB}		V_{SS}			5	µA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			7.0	mA	3
Supply current (3)	I_0		V_0, V_0			0.9	mA	4

NOTES:

1. V_{DD} = +3.0 V, V_0 = +12.0 V
2. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{SS}. The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{XCK} = 8MHz, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +3.6 V, V_0 = +6.0 to +15.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABL E PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI4-DI0, XCK, LP, L/R FR, P/S, DIX, EIO_1, EIO_2, XDISPOFF			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI4-DI0, XCK, LP, L/R FR, P/S, DIX, EIO_1, EIO_2, XDISPOFF			-10.0	µA	
	I_{LIH}	$V_I = V_{DD}$	DI4-DI0, LP, L/R, FR, P/S, DIX, XDISPOFF			+10.0	µA	
Input pull-down current	I_{PD}	$V_I = V_{DD}$	XCK, EIO_1, EIO_2			100	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0 = 15 V	COMSEG0-COMSEG119		1.5	2.0	kΩ	
Standby current	I_{SPD}		V_{SS}			5	µA	1
Supply current (1)	I_{DD}		V_{DD}			80	µA	2
Supply current (2)	I_0		V_O			130	µA	2

NOTES:

1. V_{DD} = +3.0 V, V_0 = +12.0 V,
2. V_{DD} = +3.0 V, V_0 = +12.0 V, f_{LP} =19.2 kHz, f_{FR} = 80 Hz, 1/240 duty operation, no-load.

AC Characteristics

(Segment Mode 1) (V_{SS} = 0 V, V_{DD} = +2.5 to +3.6 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 11ns	125			ns	1
Shift clock "H" pulse width	t_{WCKH}		51			ns	
Shift clock "L" pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse "H" pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (V_{SS} = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (V_{SS} = 0 V, V_{DD} = +3.0 to +3.6 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Latch pulse fall to shift clock rise time	t_{LSW}		50			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

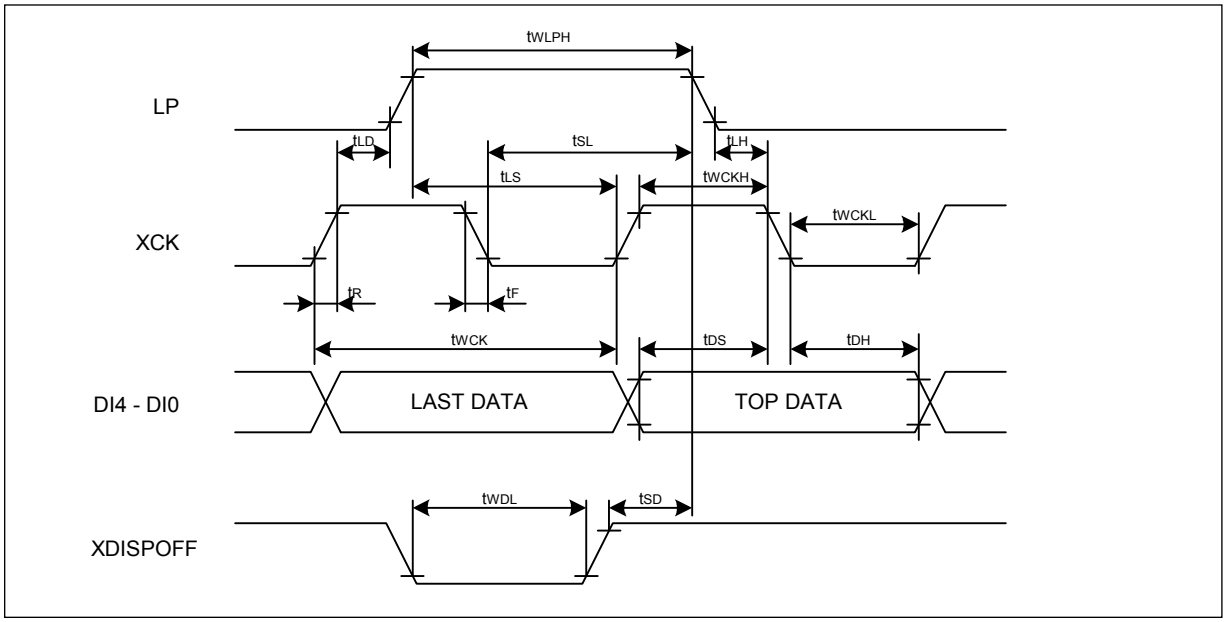
NOTES:

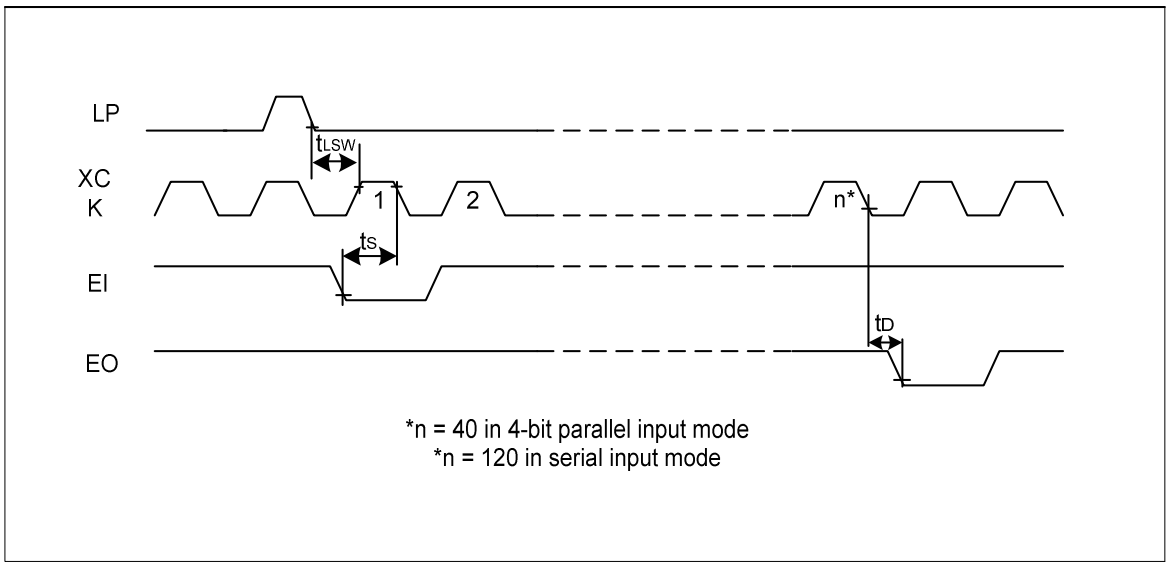
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 6.0 to +15.0 V, T_{OPR} = -20 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Shift clock period	t_{WLP}	t_R, t_F 20ns	250			ns
Shift clock “H” pulse width	t_{WLPH}	V_{DD}=5± 0.5V V_{DD}=2.5~4.5V	15 30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF “L” pulse width	t_{WDL}		1.2			us
Output delay time (1)	t_{DL}	CL=10pF			200	ns
Output delay time (2)	t_{PD1},t_{PD2}	CL=10pF			1.2	us
Output delay time (3)	t_{PD3}	CL=10pF			1.2	us

Timing Chart of Segment Mode





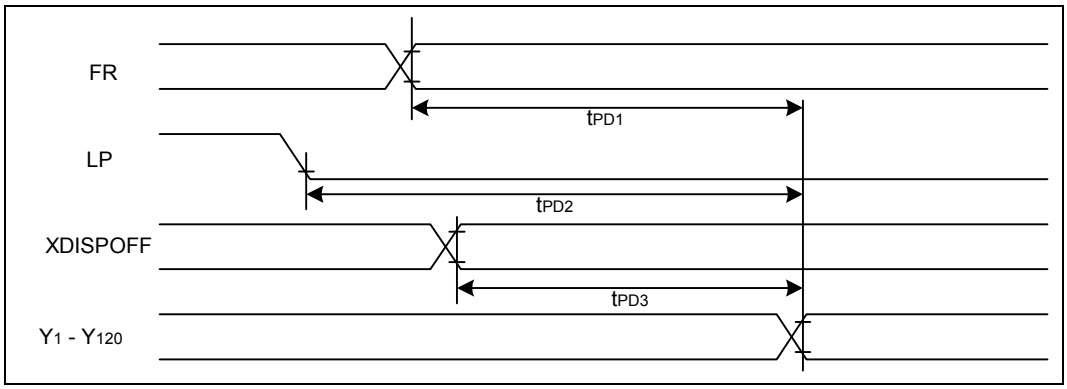
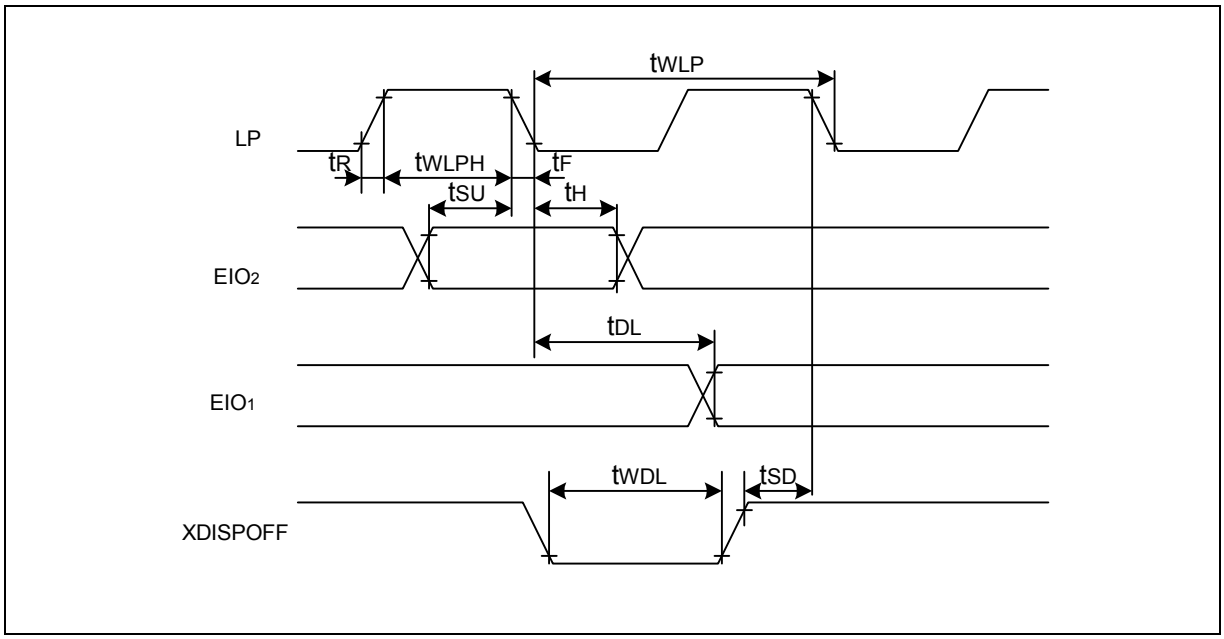


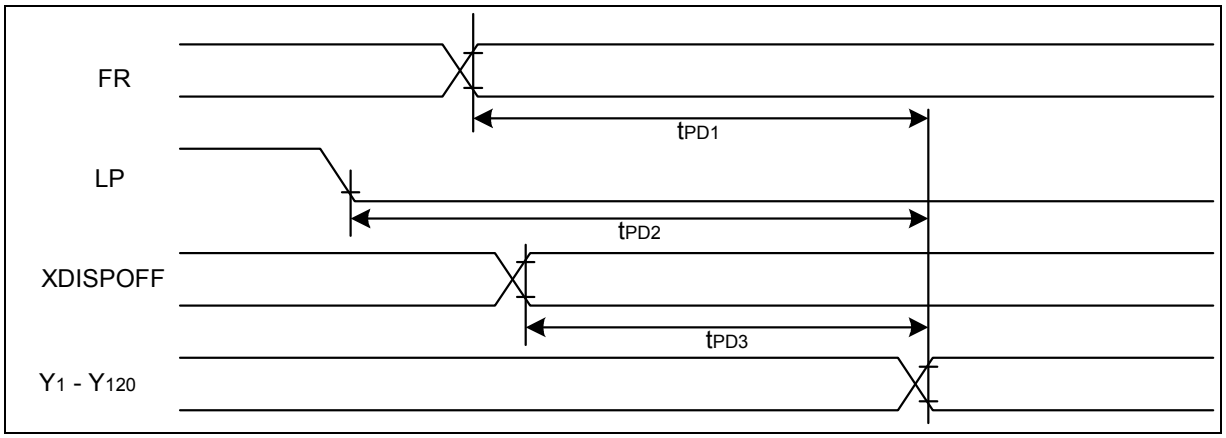
Fig. 8 Timing Characteristics (3)

(Common Mode) (V_{SS} = 0 V, V_{DD} = +2.5 to +3.6 V, V_0 = +6.0 to +15.0 V V, T_{OPR} = -20 to +85° C)

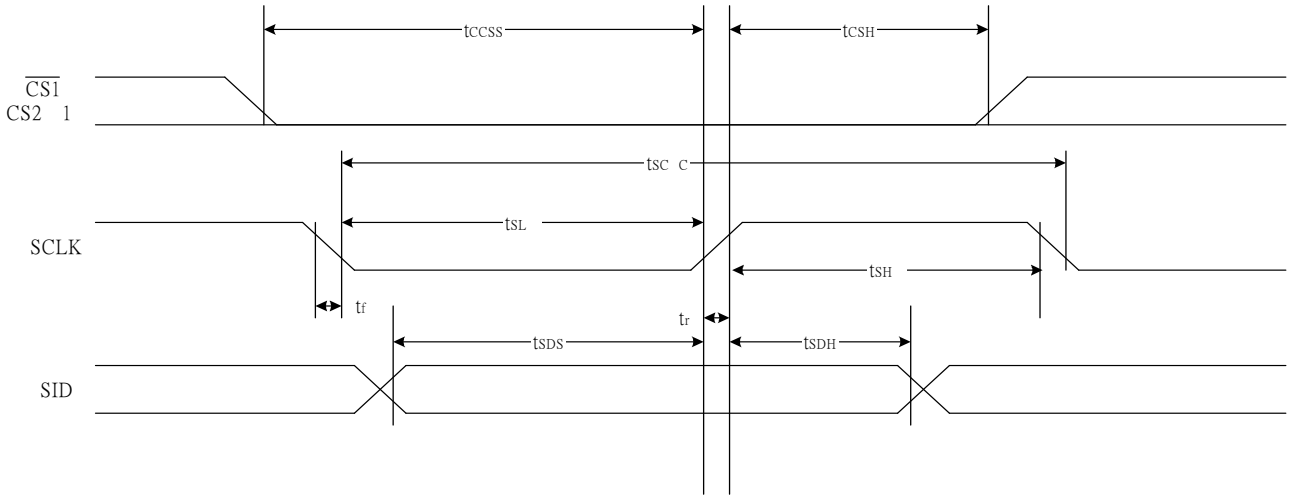
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R,t_F ≤ 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0± 0.5V	15			ns
		V_{DD} = +2.5+ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs

Timing Chart of Common Mode





The serial interface timing



Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCLK	tSCYC		50	—	ns
SCL “H” pulse width		tSHW		25	—	
SCL “L” pulse width		tSLW		25	—	
Data setup time	SID	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCL time	CS	tCSS		20	—	
CS-SCL time		tCSH		40	—	

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCLK	tSCYC		100	—	ns
SCL “H” pulse width		tSHW		50	—	
SCL “L” pulse width		tSLW		50	—	
Data setup time	SID	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCL time	CS	tCSS		30	—	
CS-SCL time		tCSH		60	—	

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCLK	tSCYC		200	—	ns
SCL “H” pulse width		tSHW		80	—	
SCL “L” pulse width		tSLW		80	—	
Data setup time	SID	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCL time	CS	tCSS		40	—	
CS-SCL time		tCSH		100	—	

10. APPLICATION CIRCUIT

8051 serial transfer mode example

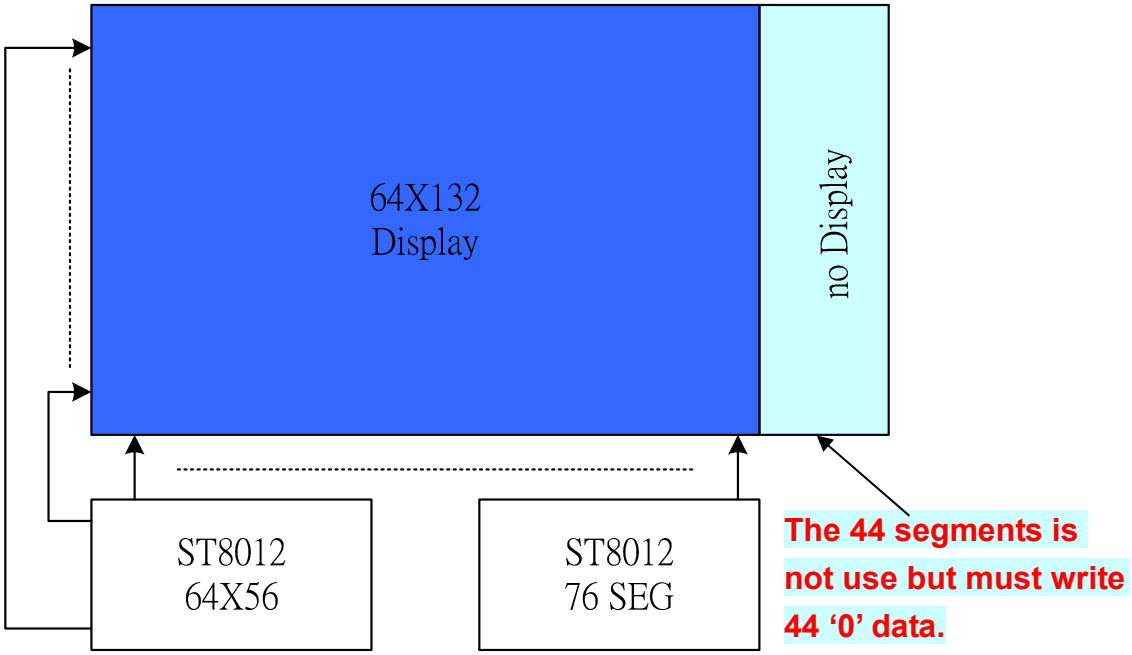
```
CLR CS
CLR SCLK          ;SID=D.7
MOVBIT SID,D.7    ; READ DATA FROM SID
SETB SCLK
CLR SCLK          ;SID=D.6
MOVBIT SID,D.6    ; READ DATA FROM SID
SETB SCLK
CLR SCLK          ;SID=D.5
MOVBIT SID,D.5    ; READ DATA FROM SID
SETB SCLK
CLR SCLK          ;SID=D.4
MOVBIT SID,D.4    ; READ DATA FROM SID
SETB SCLK
CLR SCLK          ;SID=D.3
MOVBIT SID,D.3    ; READ DATA FROM SID
SETB SCLK
CLR SCLK          ;SID=D.2
MOVBIT SID,D.2    ; READ DATA FROM SID
SETB SCLK
CLR SCLK          ;SID=D.1
MOVBIT SID,D.1    ; READ DATA FROM SID
SETB SCLK
CLR SCLK          ;SID=D.0
MOVBIT SID,D.0    ; READ DATA FROM SID
SETB SCLK
CLR SCLK
SETB CS
RET
```

Application for Data Writing of segment mode

When ST8012 is as a segment mode driver , you must write ‘0’ data to the part of no display, when segments are not all used . Example: the second segment have 120 segments ,but only use 100 segments then you must write 100 data that you need and right ,then you still write 20 ‘0’ data to fill the part of segments not used .Otherwise there will be having errors, when you don’t write the 20 ‘0’ data to fill the part of no display segments.

A summary of ST8012 in segment mode you must write the number of segments data to fill the segments.(EX : use two ST8012 to show the 64X132, then you must write the 80X160 data to fill the segments, use three ST8012 to show 120X200 the you must write the 120X240 data to fill the segments……)

EX:



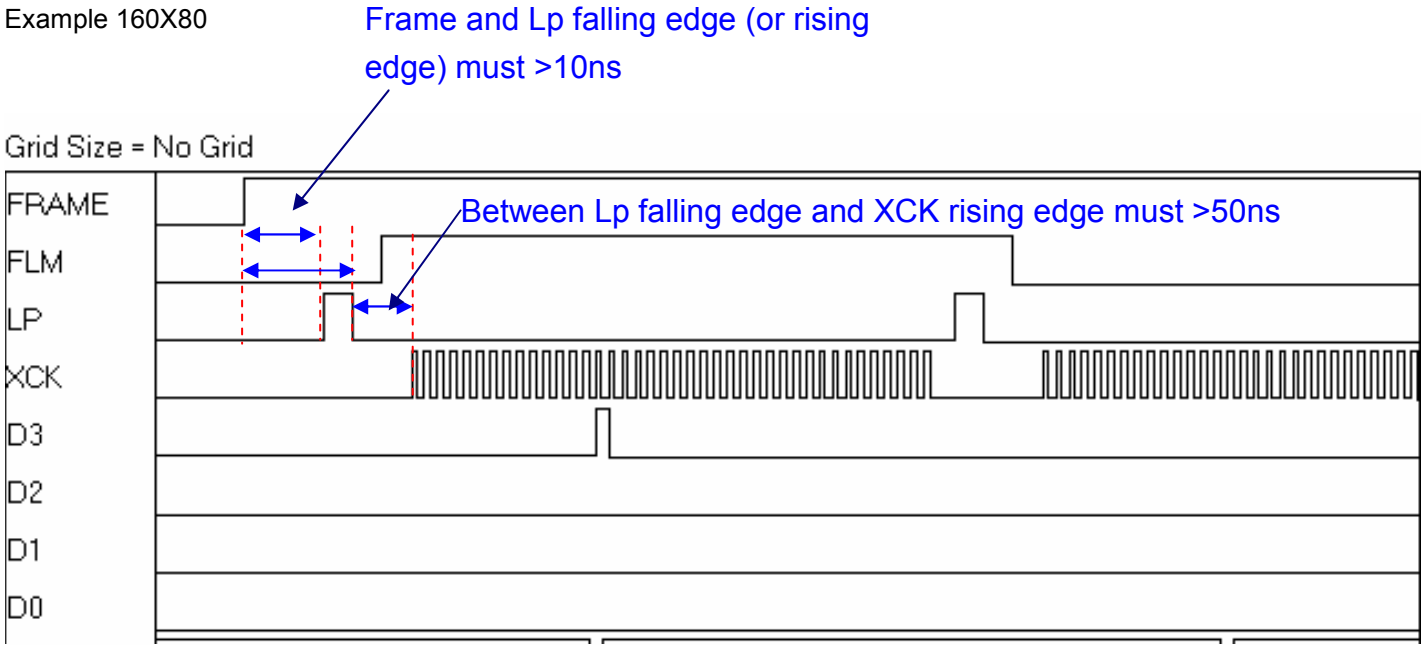
Application1 Circuit for Module of VLCD

No	Duty	Vlcd (v)
1	1/32	6,7
2	1/48	7,8
3	1/64	9,10
4	1/80	10,11
5	1/96	10,11
6	1/112	11,12
7	1/120	11,12

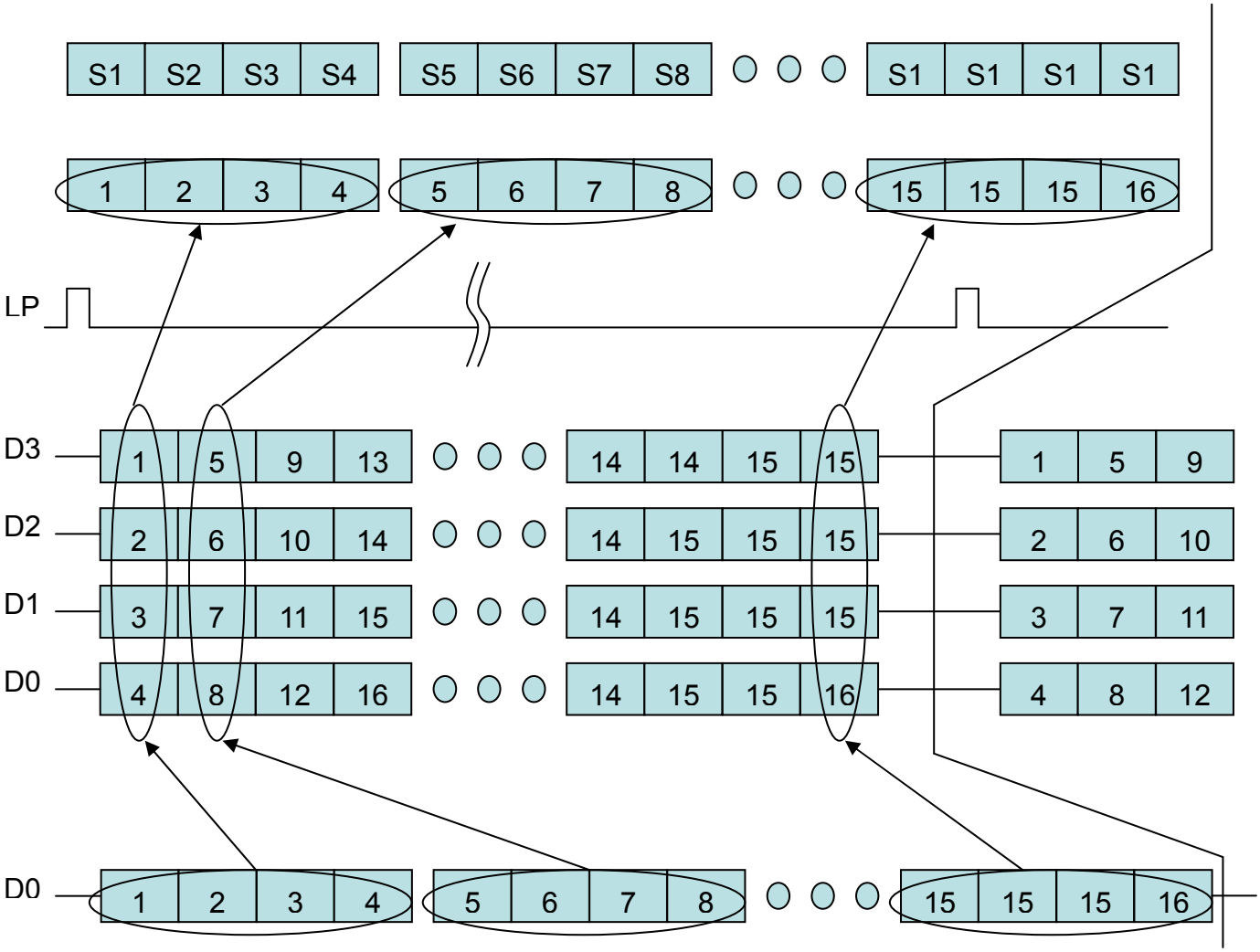
Note : The value of panel's ITO resistor is 10Ω.

Application Timing Block:

Example 160X80

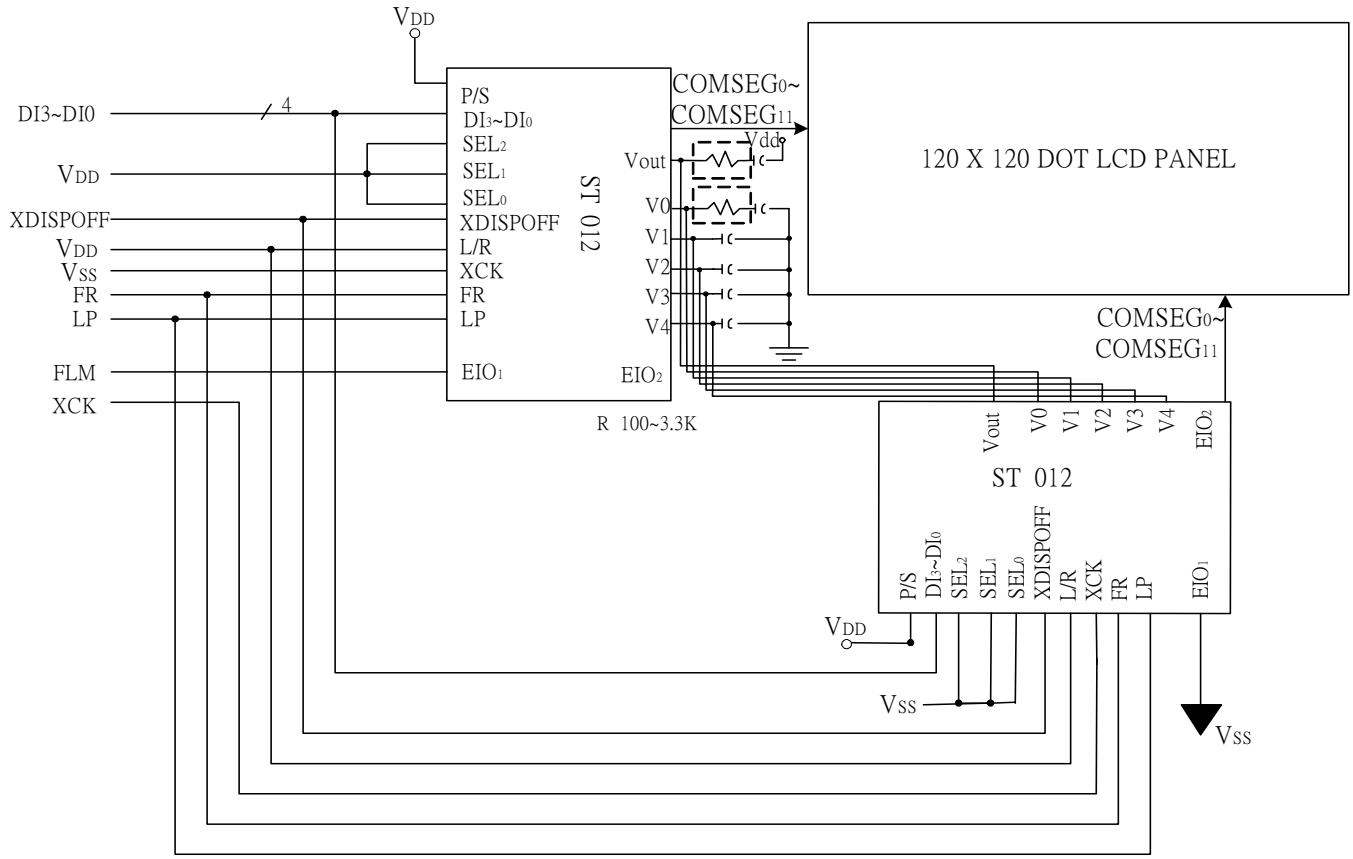


Parallel vs. Serial Interface Diagram

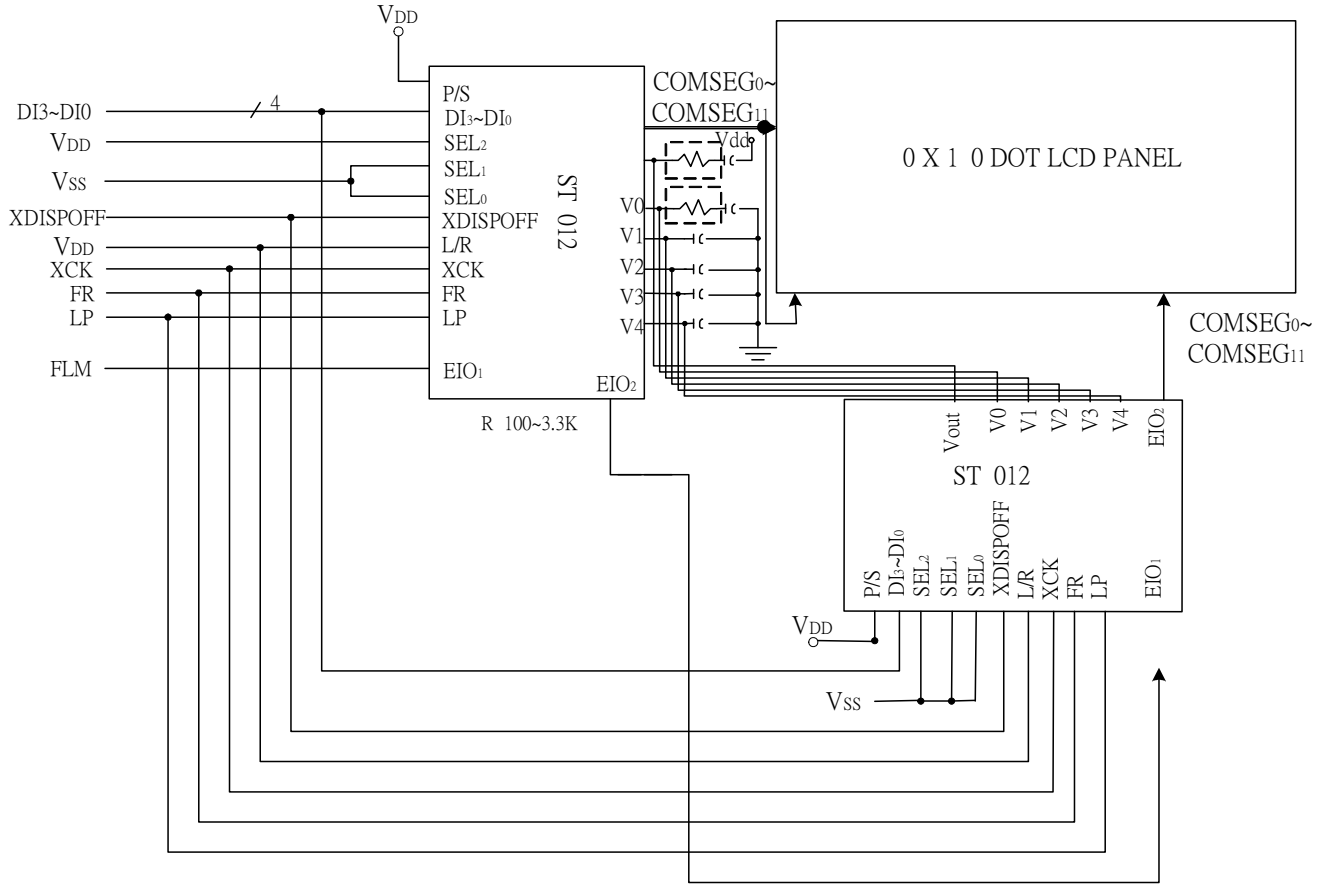


Application2 Circuit for Module

1/120 duty, 120 commons and 120 segments

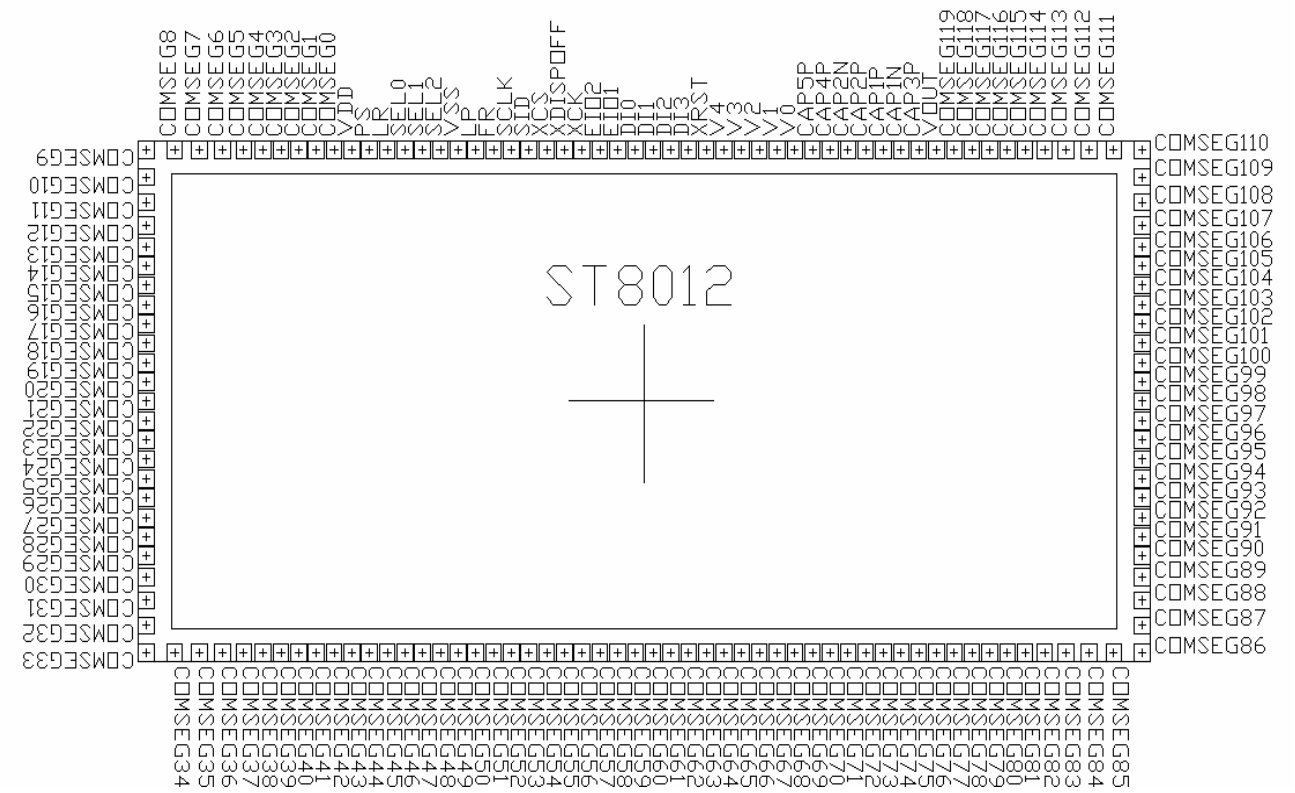


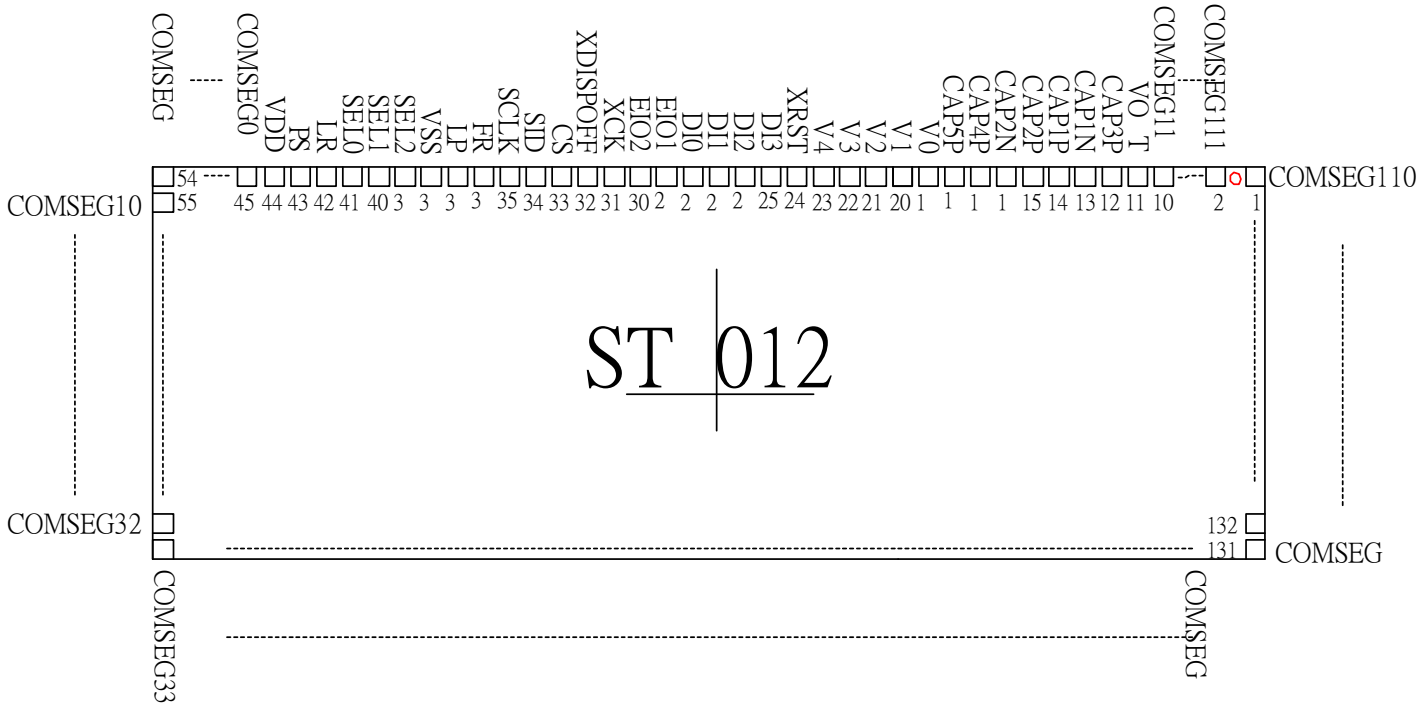
1/80 duty, 80 commons and 160 segments



11. PAD DIAGRAM

- Chip size：5,840(μm) x 2,820(μm)
- Pad size：80 μm x 80 μm
- Origin： Chip center (0,0)
- Pin Pitch：110 ~ 110 μm
- Chip Thickness：19 mil (19X25.4μm=482.6μm)





Substrate Connect to Vss.

Unit：um

Pin.No	Page pin name	X	Y	Pin.No	Page pin name	X	Y
1	COMSEG110	2810	1300	78	COMSEG33	-2810	-1300
2	COMSEG111	2650	1300	79	COMSEG34	-2650	-1300
3	COMSEG112	2510	1300	80	COMSEG35	-2510	-1300
4	COMSEG113	2380	1300	81	COMSEG36	-2380	-1300
5	COMSEG114	2260	1300	82	COMSEG37	-2260	-1300
6	COMSEG115	2150	1300	83	COMSEG38	-2150	-1300
7	COMSEG116	2050	1300	84	COMSEG39	-2050	-1300
8	COMSEG117	1950	1300	85	COMSEG40	-1950	-1300
9	COMSEG118	1850	1300	86	COMSEG41	-1850	-1300
10	COMSEG119	1750	1300	87	COMSEG42	-1750	-1300
11	VOUT	1650	1300	88	COMSEG43	-1650	-1300
12	CAP3P	1550	1300	89	COMSEG44	-1550	-1300
13	CAP1N	1450	1300	90	COMSEG45	-1450	-1300
14	CAP1P	1350	1300	91	COMSEG46	-1350	-1300
15	CAP2P	1250	1300	92	COMSEG47	-1250	-1300
16	CAP2N	1150	1300	93	COMSEG48	-1150	-1300
17	CAP4P	1050	1300	94	COMSEG49	-1050	-1300
18	CAP5P	950	1300	95	COMSEG50	-950	-1300
19	V0	850	1300	96	COMSEG51	-850	-1300
20	V1	750	1300	97	COMSEG52	-750	-1300
21	V2	650	1300	98	COMSEG53	-650	-1300
22	V3	550	1300	99	COMSEG54	-550	-1300
23	V4	450	1300	100	COMSEG55	-450	-1300
24	XRST	350	1300	101	COMSEG56	-350	-1300
25	DI3	250	1300	102	COMSEG57	-250	-1300
26	DI2	150	1300	103	COMSEG58	-150	-1300
27	DI1	50	1300	104	COMSEG59	-50	-1300
28	DI0	-50	1300	105	COMSEG60	50	-1300
29	EIO1	-150	1300	106	COMSEG61	150	-1300
30	EIO2	-250	1300	107	COMSEG62	250	-1300
31	XCK	-350	1300	108	COMSEG63	350	-1300
32	XDISPOFF	-450	1300	109	COMSEG64	450	-1300
33	XCS	-550	1300	110	COMSEG65	550	-1300
34	SID	-650	1300	111	COMSEG66	650	-1300
35	SCLK	-750	1300	112	COMSEG67	750	-1300
36	FR	-850	1300	113	COMSEG68	850	-1300
37	LP	-950	1300	114	COMSEG69	950	-1300
38	VSS	-1050	1300	115	COMSEG70	1050	-1300
39	SEL2	-1150	1300	116	COMSEG71	1150	-1300
40	SEL1	-1250	1300	117	COMSEG72	1250	-1300
41	SEL0	-1350	1300	118	COMSEG73	1350	-1300
42	LR	-1450	1300	119	COMSEG74	1450	-1300
43	PS	-1550	1300	120	COMSEG75	1550	-1300
44	VDD	-1650	1300	121	COMSEG76	1650	-1300
45	COMSEG0	-1750	1300	122	COMSEG77	1750	-1300
46	COMSEG1	-1850	1300	123	COMSEG78	1850	-1300

47	COMSEG2	-1950	1300	124	COMSEG79	1950	-1300
48	COMSEG3	-2050	1300	125	COMSEG80	2050	-1300
49	COMSEG4	-2150	1300	126	COMSEG81	2150	-1300
50	COMSEG5	-2260	1300	127	COMSEG82	2260	-1300
51	COMSEG6	-2380	1300	128	COMSEG83	2380	-1300
52	COMSEG7	-2510	1300	129	COMSEG84	2510	-1300
53	COMSEG8	-2650	1300	130	COMSEG85	2650	-1300
54	COMSEG9	-2810	1300	131	COMSEG86	2810	-1300
55	COMSEG10	-2810	1160	132	COMSEG87	2810	-1160
56	COMSEG11	-2810	1030	133	COMSEG88	2810	-1030
57	COMSEG12	-2810	910	134	COMSEG89	2810	-910
58	COMSEG13	-2810	800	135	COMSEG90	2810	-800
59	COMSEG14	-2810	700	136	COMSEG91	2810	-700
60	COMSEG15	-2810	600	137	COMSEG92	2810	-600
61	COMSEG16	-2810	500	138	COMSEG93	2810	-500
62	COMSEG17	-2810	400	139	COMSEG94	2810	-400
63	COMSEG18	-2810	300	140	COMSEG95	2810	-300
64	COMSEG19	-2810	200	141	COMSEG96	2810	-200
65	COMSEG20	-2810	100	142	COMSEG97	2810	-100
66	COMSEG21	-2810	0	143	COMSEG98	2810	0
67	COMSEG22	-2810	-100	144	COMSEG99	2810	100
68	COMSEG23	-2810	-200	145	COMSEG100	2810	200
69	COMSEG24	-2810	-300	146	COMSEG101	2810	300
70	COMSEG25	-2810	-400	147	COMSEG102	2810	400
71	COMSEG26	-2810	-500	148	COMSEG103	2810	500
72	COMSEG27	-2810	-600	149	COMSEG104	2810	600
73	COMSEG28	-2810	-700	150	COMSEG105	2810	700
74	COMSEG29	-2810	-800	151	COMSEG106	2810	800
75	COMSEG30	-2810	-910	152	COMSEG107	2810	910
76	COMSEG31	-2810	-1030	153	COMSEG108	2810	1030
77	COMSEG32	-2810	-1160	154	COMSEG109	2810	1160

NOTE

2001.12/19 Modify the booster capacity

2002 1/8 Modify the serial command interface-timing block (p16)

2002 1/14 Modify the Register command code

2002 1/17 Modify the Reset Register command defined

2002 1/23 Modify the pin description defined and command interface unused mode (p17)

2002 2/22 Modify the Booster circuit diagram (p19)

2002 2/22 Modify the Mix Mode table(p10)、add the serial interface timing(p33、p34)、add pad data(p37)

2002 2/22 Modify the CS SET (p34)

2002/3/20 Modify the serial interface, when in the serial interface the d0←data.and add the AC direction.

2002/4/3 Modify the pad location (P39)

2002/06/04 Modify the XREST ACTIVE (p2)

2002/06/010 Modify the Chip Size (P37)

2002/06/21 Modify common and segment mode pin description (P6~P8)

2002/07/01 Modify booster circuit (P20)

2002/07/09 Command interface unused mode (use the default value)(P18)

2002/10/14 Delete the software reset and cog package , add the regulator liner line , delete some AC application.

2002/11/22 Modify the booster frequency V1.1A

2003/03/31 Modify booster turns off command (p28)

2003/04/04 Add the XCS used math.

2003/4/17 Modify the Application circuit

2003/6/17 Add Application circuit V1.3

2003/11/12 Add Pin Pitch value V1.4

2004/04/05 Add application timing block V1.5

2004/09/08 Define timing(t_{LSW}) of Segment Mode. P33~P35 V1.6