



4-Bit Arithmetic Logic Unit/Function Generator

ELECTRICALLY TESTED PER: MPG 10H581

The 10H581 is a high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple-through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (PG) and carry generate (GG) are provided allowing fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the 10579, full-carry look-ahead, as a second order look ahead block, the 10H581 provides high speed arithmetic operations on very long words.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and not increase in power supply current.

- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
VCC1	1	7	GND
F0	2	8	51 Ω to VTT
F1	3	9	51 Ω to VTT
GG	4	10	51 Ω to VTT
Cn + 4	5	11	51 Ω to VTT
F3	6	12	51 Ω to VTT
F2	7	13	51 Ω to VTT
PG	8	14	51 Ω to VTT
B3	9	15	50 Ω to VEE
A3	10	16	GND
B2	11	17	50 Ω to VEE
VEE	12	18	VEE
S3	13	19	50 Ω to VEE
S0	14	20	GND
S2	15	21	50 Ω to VEE
A2	16	22	GND
S1	17	23	GND
A1	18	24	50 Ω to VEE
B1	19	1	VEE
B0	20	2	50 Ω to VEE
A0	21	3	GND
Cn	22	4	50 Ω to VEE
M	23	5	GND
VCC2	24	6	GND

BURN - IN CONDITIONS:

VTT = - 2.0 V MAX/ - 2.2 V MIN

VEE = - 5.7 V MAX/ - 5.2 V MIN

Military 10H581

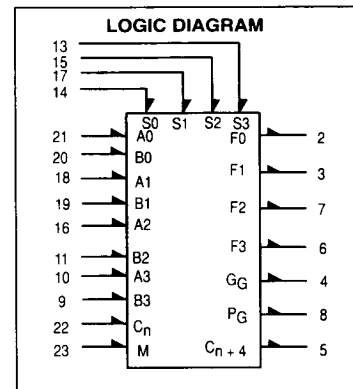
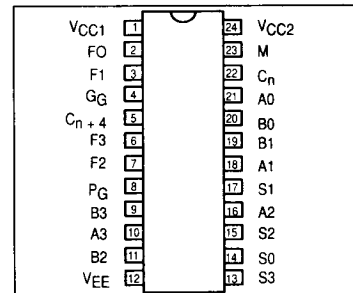


AVAILABLE AS

- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: 10H581/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: K
CERFLAT: J

The letter "M" appears before the slash on LCC.



10H581

ARITHMETIC/LOGIC FUNCTIONS

Function Select				Logic Function M is High C = D. C.	Arithmetic Operation M is Low C _n is low
S ₃	S ₂	S ₁	S ₀	F	F
L	L	L	L	$F = \bar{A}$	$F = A$
L	L	L	H	$F = \bar{A} + \bar{B}$	$F = A \text{ plus } (A \cdot \bar{B})$
L	L	H	L	$F = \bar{A} + B$	$F = A \text{ plus } (A \cdot B)$
L	L	H	H	$F = \text{Logical "1"}$	$F = A \text{ times } 2$
L	H	L	L	$F = \bar{A} \cdot B$	$F = (A + B) \text{ plus } 0$
L	H	L	H	$F = \bar{B}$	$F = (A + B) \text{ plus } (A \cdot \bar{B})$
L	H	H	L	$F = A \oplus B$	$F = A \text{ plus } B$
L	H	H	H	$F = A + \bar{B}$	$F = A \text{ plus } (A + B)$
H	L	L	L	$F = \bar{A} \cdot B$	$F = (A + \bar{B}) \text{ plus } 0$
H	L	L	H	$F = A \oplus B$	$F = A \text{ minus } B \text{ minus } 1$
H	L	H	L	$F = B$	$F = (A + \bar{B}) \text{ plus } (A \cdot B)$
H	L	H	H	$F = A + B$	$F = A \text{ plus } (A + \bar{B})$
H	H	L	L	$F = \text{Logical "0"}$	$F = \text{minus } 1 \text{ (two's complement)}$
H	H	L	H	$F = A \cdot \bar{B}$	$F = (A \cdot \bar{B}) \text{ minus } 1$
H	H	H	L	$F = A \cdot B$	$F = (A \cdot B) \text{ minus } 1$
H	H	H	H	$F = A$	$F = \text{minus } 1$

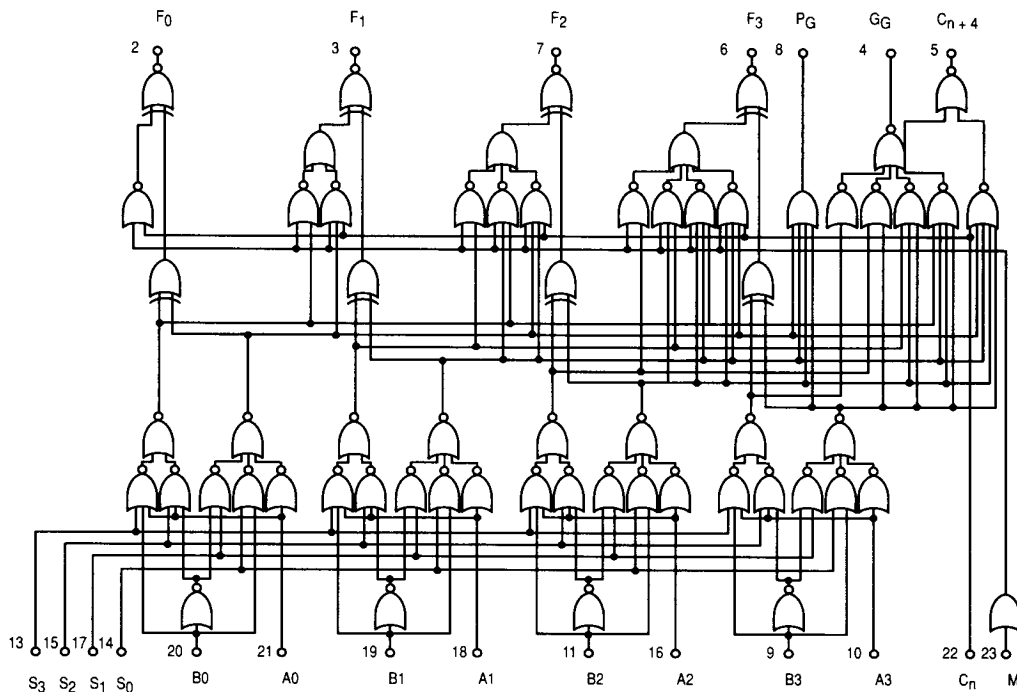


Figure 1. Logic Diagram

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- $$V_{FEL} = -2.94 \text{ V}$$



10H581 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH}	V _{IL}	V _{IHA}	V _{ILA}	PS ₁	PS ₂	VEE ₁	VEE ₂
T _A = 25 °C	-0.78	-1.950	-1.105	-1.475	+1.11	+0.31	-5.46	-4.94
T _A = 125 °C	-0.65	-1.950	-1.000	-1.400	+1.24	+0.36	-5.46	-4.94
T _A = -55 °C	-0.88	-1.950	-1.255	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3			V _{IH}	V _{IL}	V _{IHA}	V _{ILA}	V _{EE1/2}	V _{CC}	P.U.T.			
	Functional Parameters:	Min	Max	Min	Max	Min	Max	V	9 - 11 16 - 23	13 - 15			12	1, 24	2 - 8			
V _{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.09	-0.88	V										
V _{OL1}	Low Output Voltage	-1.85	-1.620	-1.82	-1.545	-1.92	-1.655	V	9 - 11, 14, 16 18, 19, 21 - 23	9, 10, 13, 15 16, 17, 19, 21			12	1, 24	2, 3, 5 - 8			
V _{OHA}	High Output Voltage	-0.95	-0.78	-0.845	-0.63	-1.10	-0.88	V	9 - 11, 13 16 - 23	13 - 23	16 - 23	13 - 15 22, 23	12	1, 24	2 - 8			
V _{OLA}	Low Output Voltage	-1.85	-1.60	-1.88	-1.525	-1.92	-1.635	V		9 - 11, 13 - 23	14, 15	9 - 11 16 - 23	12	1, 24	2 - 8			
V _{OL2}	Low Output Voltage	-1.99	-1.620	-1.88	-1.545	-2.10	-1.655	V	11, 14, 16, 18 20, 22, 23	9, 10, 13, 15 17, 19, 21	8		12	1, 24	4			
I _{EE}	Power Supply Current	-145		-160		-160		mA	9 - 11, 16 18 - 21				12	1, 24	12			
I _{IH1}	Input Current High		200		340		340	μA	13, 23				12	1, 24	13, 23			
I _{IH2}	Input Current High		220		375		375	μA	10, 16, 18 21				12	1, 24	10, 16, 18 21			
I _{IH3}	Input Current High		245		415		415	μA	9, 11 19, 20				12	1, 24	9, 11, 19, 20			
I _{IH4}	Input Current High		265		450		450	μA	14, 15, 17				12	1, 24	14, 15, 17			
I _{IH5}	Input Current High		290		580		495	μA	22				12	1, 24	22			
I _{IL}	Input Current Low	0.5		0.3		0.5		mA	9 - 11 13 - 23				1, 16		9 - 11, 13 - 23			

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Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	PS1	PS2	VEE1	VEE2
T _A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-4.94
T _A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-4.94
T _A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND							
		Min	Max	Min	Max	Min	Max		V _{IN}	V _{OUT}	V _{CC}	V _{EE1}	PS1	P. U. T.		
t _{TLH} / t _{THL}	Rise & Fall Time	0.5	2.3	0.764	2.64	0.62	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7		
t _{pd}	Propagation Delay C _N to C _N + 4	0.6	2.2	0.74	2.64	0.74	2.4	ns	"	"	"	"	"	"		
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.7	2.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7		
t _{pd}	Propagation Delay C _N to F	1.0	3.0	1.44	3.96	1.8	3.6	ns	"	"	"	"	"	"		
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.84	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7		
t _{pd}	Propagation Delay A to F	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"		
t _{TLH} / t _{THL}	Rise & Fall Time	0.8	2.4	1.08	3.12	1.0	2.88	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7		
t _{pd}	Propagation Delay A to PG	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"		
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.764	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7		
t _{pd}	Propagation Delay A to GG	1.5	3.7	1.92	4.68	1.8	4.44	ns	"	"	"	"	"	"		
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.74	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7		
t _{pd}	Propagation Delay A to C _N + 4	1.5	3.6	1.92	4.68	1.8	4.32	ns	"	"	"	"	"	"		

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Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	V _{EE1}	V _{EE2}	V _{EE1}	V _{EE2}
T _A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-4.94	-5.2	-4.94
T _A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-4.94	-5.2	-4.94
T _A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-4.94	-5.2	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max								
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.3	0.74	3.0	0.74	2.76	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7
t _{pd}	Propagation Delay B to F	2.0	4.5	2.52	5.76	2.2	5.0	ns	"	"	"	"	"	"	"
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7
t _{pd}	Propagation Delay B to PG	1.5	3.8	1.92	4.8	1.8	4.56	ns	"	"	"	"	"	"	"
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7
t _{pd}	Propagation Delay B to GG	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"	"
t _{TLH} / t _{THL}	Rise & Fall Time	0.5	2.0	0.5	2.64	0.5	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7
t _{pd}	Propagation Delay B to Cn + 4	2.0	4.0	2.52	5.16	2.4	4.8	ns	"	"	"	"	"	"	"
t _{TLH} / t _{THL}	Rise & Fall Time	0.7	2.3	0.86	3.0	0.86	2.76	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7
t _{pd}	Propagation Delay M to F	1.5	4.2	1.92	5.4	1.8	5.04	ns	"	"	"	"	"	"	"
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.74	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22		2 - 7
t _{pd}	Propagation Delay S to F	1.5	4.5	1.92	5.76	1.8	5.4	ns	"	"	"	"	"	"	"

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T _A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-4.94
T _A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
		+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9	Subgroup 10	Subgroup 11	Subgroup 12	Subgroup 13	Subgroup 14							
	Functional Parameters:	Min	Max	Min	Max	Min	Max		V _{IN}	V _{OUT}	V _{CC}	V _{EE1}	PS ₁	P. U. T.
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t _{pd}	Propagation Delay S to P _G	1.5	4.0	1.92	5.16	1.8	4.8	ns	"	"	"	"	"	"
t _{TLH} / t _{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t _{pd}	Propagation Delay S to C _n + 4	1.5	4.1	1.92	5.28	1.8	4.92	ns	"	"	"	"	"	"
t _{TLH} / t _{THL}	Rise & Fall Time	0.5	3.2	0.5	4.0	0.5	3.84	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t _{pd}	Propagation Delay S to G _G	1.3	4.5	1.68	5.76	1.56	5.4	ns	"	"	"	"	"	"