



Quad 2-Input NOR Gate

ELECTRICALLY TESTED PER:
MPG 1662 (-30°C to +85°C)

- $P_D = 240$ mW typ/pkg
- $t_{pd} = 0.9$ ns typ (510 ohm load)
= 1.1 ns typ (50 ohm load)
- Full Load Current, $I_L = -25$ mAdc max

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage ($V_{CC} = 0$)	V_{CC}	-8.0	0	Vdc
Base Input Voltage ($V_{CC} = 0$)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	-55	+125	°C
Operating Temperature Range	T_A	-30	+85	°C

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
AOUT	2	6	51 Ω to V_{TT}
BOUT	3	7	51 Ω to V_{TT}
A _{IN1}	4	8	OPEN
A _{IN2}	5	9	OPEN
B _{IN1}	6	10	OPEN
B _{IN2}	7	11	OPEN
V_{EE}	8	12	V_{EE}
N.C.	9	13	OPEN
C _{IN1}	10	14	OPEN
C _{IN2}	11	15	GND
D _{IN1}	12	16	OPEN
D _{IN2}	13	1	GND
COUT	14	2	51 Ω to V_{TT}
DOUT	15	3	51 Ω to V_{TT}
V_{CC2}	16	4	GND

BURN - IN CONDITIONS:
 $V_{TT} = -2.0$ V MAX/-2.2 V MIN
 $V_{EE} = -5.7$ V MAX/-5.2 V MIN

Military 1662

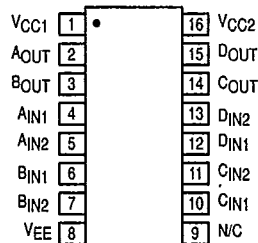


AVAILABLE AS

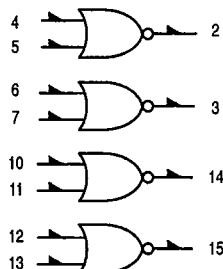
- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: N/A
 - 4) 1662/BXA *
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

* 883 Processing (Non-Compliant)



LOGIC DIAGRAM



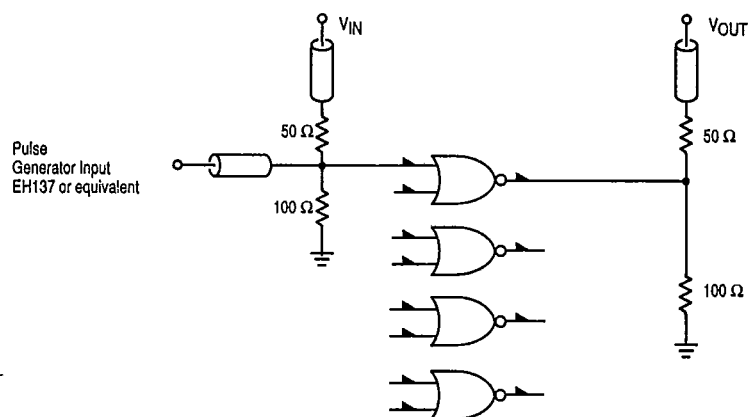


Figure 1. Test Circuit

NOTES

1. Coaxial cables (Equal lengths, typ 2 places) to scope.
2. $t_r = t_f = 1.5 \text{ ns} \pm 0.2 \text{ ns}$.
3. PRR = 20 MHz, 50% duty cycle.
4. Unused outputs connected to a 50 Ω resistor to ground.

Temp.	25°C	85°C	-30°C
V _{ILL}	0.31 V	0.34 V	0.28 V
V _{IHH}	1.11 V	1.19 V	1.04 V

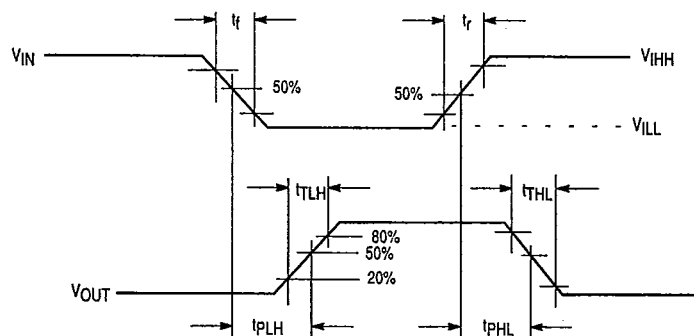


Figure 2. Test Circuit Waveforms

1662
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V _{IH}	V _{IL}	V _{IHA}	V _{ILA}	V _{EE}	V _{EEL}
T _A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T _A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T _A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0.0 V, Output Load = 50 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max									
VOH	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V								
VOL	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V								
VOHA	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V								
VOLA	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V								
IEE	Power Supply Drain Current	-56		-56		-56		mA								
IINH	Input Current High		350		350		350	μA								
IINL	Input Current Low	0.5		0.3		0.5		μA								

T-43-22



T-43-22

1662
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V _{IH}	V _{IL}	V _{IHA}	V _{ILA}	V _{EE}	V _{EEL}	V _{CC}
T _A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T _A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T _A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max						
t _{TLH}	Rise Time		2.1		2.3		2.2	ns	5, 6 11, 12	2, 3, 14, 16	V _{CC}	VEEL	P.U.T.
t _{THL}	Fall Time		2.1		2.3		2.2	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t _{PHL}	Propagation Delay High to Low A, B and D		1.9		2.1		2.0	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t _{PLH}	Propagation Delay Low to High A, B and D		2.1		2.1		2.1	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t _{PHL}	Propagation Delay High to Low C		2.0		2.2		2.1	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t _{PLH}	Propagation Delay Low to High C		2.1		2.1		2.1	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15