GigaBit Logic **16G020/S0030**

T-51-11

Dual GaAs SPST Switch 0.5 nS Switching Time

3

FEATURES

- Very fast switching time (0.5 ns typical)
- High isolation (better than 50dB @ 2GHz)
- Broad bandwidth (DC to 4GHz)
- Ultra low DC power consumption (60μW typical)
- Low insertion loss (< 3dB)
- Two layer gold metalization

APPLICATIONS

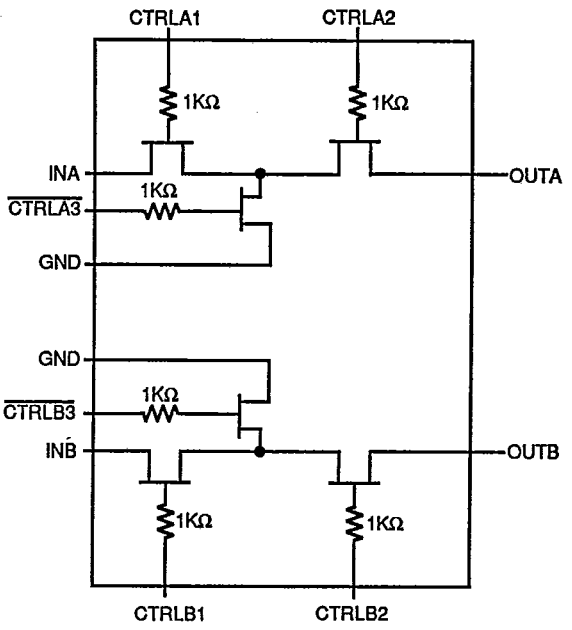
- Electronic Countermeasure
- Phased-array Radar
- Telecommunication
- Fiber-optic system
- Test equipment
- High resolution monitor

PRODUCT DESCRIPTION

The S0030 is a wide band dual GaAs SPST switch with typical switching time of 500ps. The circuit topology of one switch consists of two series FETs and one shunt FET and was designed to provide greater than 70db isolation at 1 GHz. The S0030 is a wire-bonding option of GigaBit's 16G020-F programmable FET array and uses 6 of the 11 FETs contained in the array. The gate resistors are 1K chip resistors included in the package and mounted close to the gate bond pad to minimize the shunt capacitance of the bond wire. The S0030 can be configured as an SPDT by connecting together inputs INA and INB, or as a building block to form single pole multithrow switches.

For more information on the GaAs MESFETs used in the S0030, please refer to the 16G020 data sheet.

CIRCUIT DIAGRAM



Note: GND pins connected to package bottom surface.

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T-51-11

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	ABSOLUTE MAXIMUM RATINGS
CTRL	Control Voltage	-8V to +5V
V_{in}	Input Voltage	-4.5V to +4.5V
P_{in}	Input Power	26 dBm
I_G	Gate Forward Biased Current	20 mA
I_D, I_S	Continuous Drain/Source Current	50 mA
I_D, I_S	Pulsed Drain/Source Current	100mA
T_{STOR}	Storage Temperature	-60°C to +150°C

SWITCH CONTROL VOLTAGE

The depletion GaAs MESFETs used in the S0030 have pinchoff voltages between -0.7V and -1.1V. In order to turn the switch off, the control signal of the series FETs (CTRL1 and CTRL2) must be brought at least 1.1V more negative than the lowest voltage of the RF signal. For example (see figure 1 below), if the peak to peak RF signal amplitude is 2Vo (-Vo to +Vo), the control signal in the series FETs should be -Vo -1.1 volts maximum. We recommend bringing the control signal of the series FETs to -Vo -1.5V to improve isolation when the switch is off. To turn the switch on, the control voltage of the series FETs should be +Vo + 0.6 Volts typical or 0.6 Volts above the most positive voltage of the RF signal.
Conversely, the control signal of the shunt FET ($\overline{CTRL3}$) should be brought to +Vo +0.6 Volts typical when the switch is off and to - Vo - 1.5V typical when the switch is on.
GigaBit Logic part number 16G061 (dual Pin Driver) may be used to conveniently generate control signal voltages to drive the S0030 from an ECL or an AC-coupled small signal source.

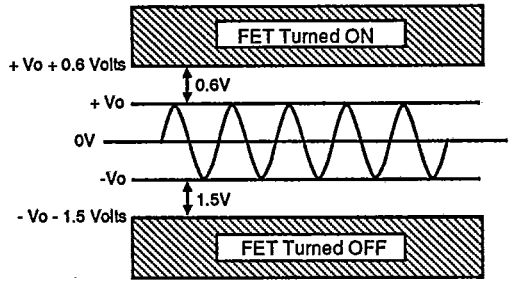

FIGURE 1.
FET TURN ON AND OFF VOLTAGES

Condition of the Switch	SWITCH CONTROL FUNCTION (Note 1)			
	CTRL 1	CTRL 2	CTRL 3	UNITS
ON	+Vo + 0.6	+Vo + 0.6	-Vo - 1.5	V
OFF	-Vo - 1.5	-Vo - 1.5	+Vo + 0.6	V

Note 1: Vo=input signal amplitude

S0030 ELECTRICAL CHARACTERISTICS (Note 1)				
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**TYP (25°C)**	**UNITS**
T_{ON} , T_{OFF}	Switching Time	$\overline{CTRL1}$ = CTRL2 = - 2V to 0.5V $\overline{CTRL3}$ = + 0.5V to -2V (see test circuit fig.2 p4)		
		V_{in} = -0.5V	0.5	ns
		V_{in} = - 1V	0.6	ns
S21 off	Isolation	$\overline{CTRL1}$ = CTRL2 = - 2V $\overline{CTRL3}$ = + 0.1V Package lid grounded, 50 Ω output temination to GND RF_{in} = - 0.5V to 0.5V		
		f_{in} = 1 GHz	< -70	dB
		f_{in} = 1.5 GHz	< -65	dB
		f_{in} = 2.0 GHz	-50	dB
		f_{in} = 3.0 GHz	-30	dB
		f_{in} = 4.0 GHz	-20	dB
S21 on	Insertion Loss	$\overline{CTRL1}$ = CTRL2 = + 1V $\overline{CTRL3}$ = - 2V Package lid grounded, 50 Ω output termination to GND		
		f_{in} = 100 MHz	-2.2	dB
		f_{in} = 1 GHz	-2.85	dB
		f_{in} = 3 GHz	-3.3	dB
		f_{in} = 4 GHz	-3.4	dB
S11 on	Return Loss	$\overline{CTRL1}$ = CTRL2 = + 1V $\overline{CTRL3}$ = - 2V Package lid grounded, 50 Ω output termination to GND		
		f_{in} = 100 MHz	-20	dB
		f_{in} = 1 GHz	-15	dB
		f_{in} = 3 GHz	-12	dB
		f_{in} = 4 GHz	-20	dB

Note 1: **For more information on the electrical characteristics of the MESFETs used in the S0030, please refer to the 16G020 data sheet.**

T-51-11

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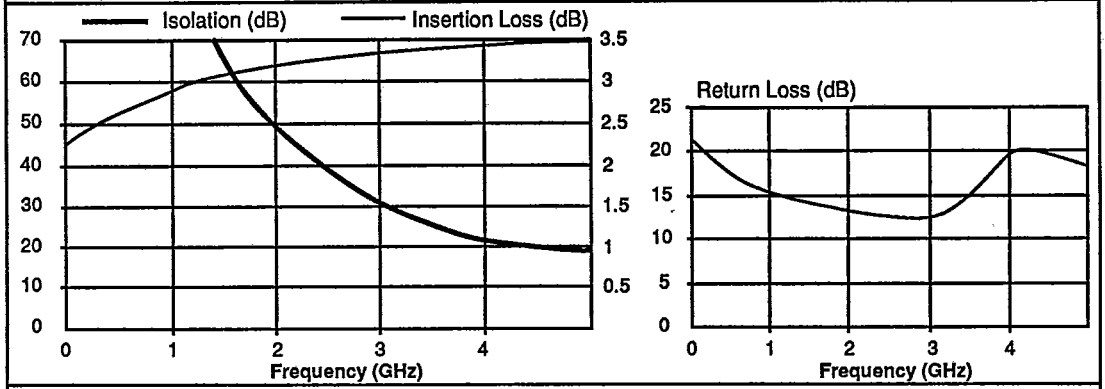
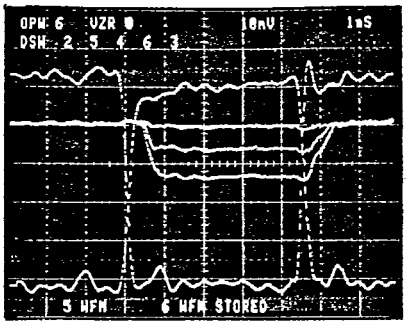
DEVICE CHARACTERISTICS

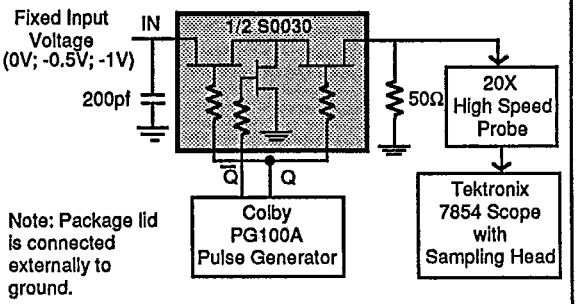


SWITCHING TIME MEASUREMENT



Vertical Scale: 0.5V/div ; Horizontal Scale: 1ns/div

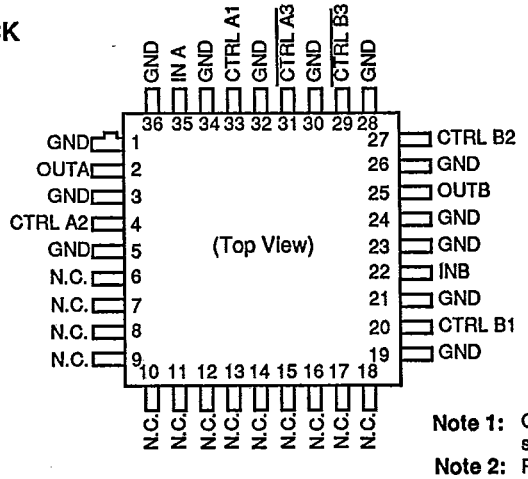
Figure 2: Test Configuration and Equipment



Note: Package lid is connected externally to ground.

PACKAGE PINOUT DIAGRAM

36 LEAD FLATPACK
16G020/S0030



Note 1: GND pins and Package bottom surface are internally connected.
Note 2: Package Lid is the labelled surface.

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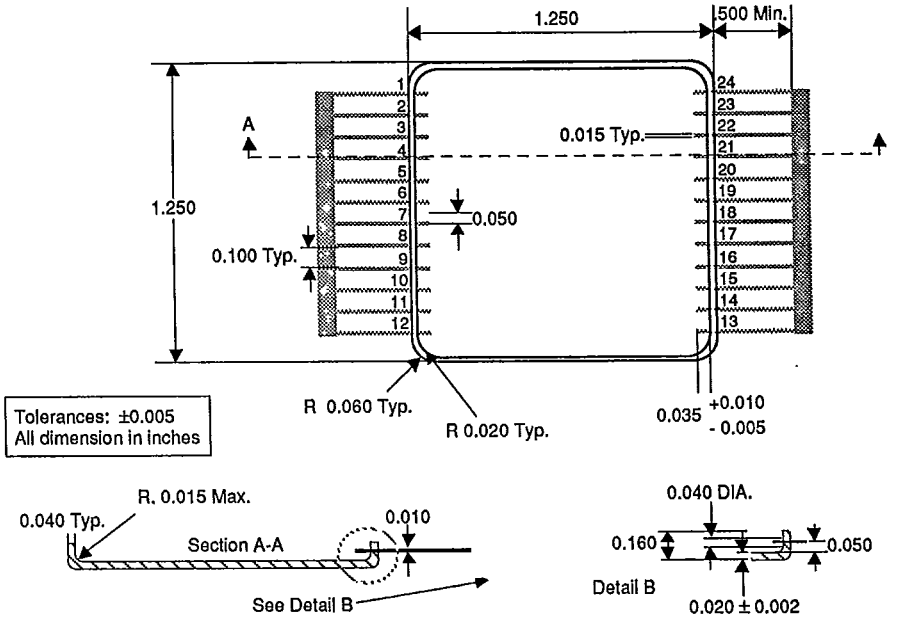
24 PIN HYBRID 18 PIN PACKAGE

T-90-20

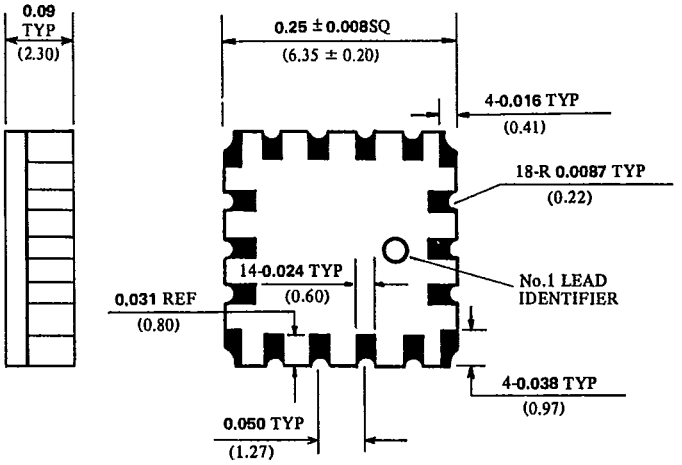
24 PIN HYBRID PACKAGE

Type H



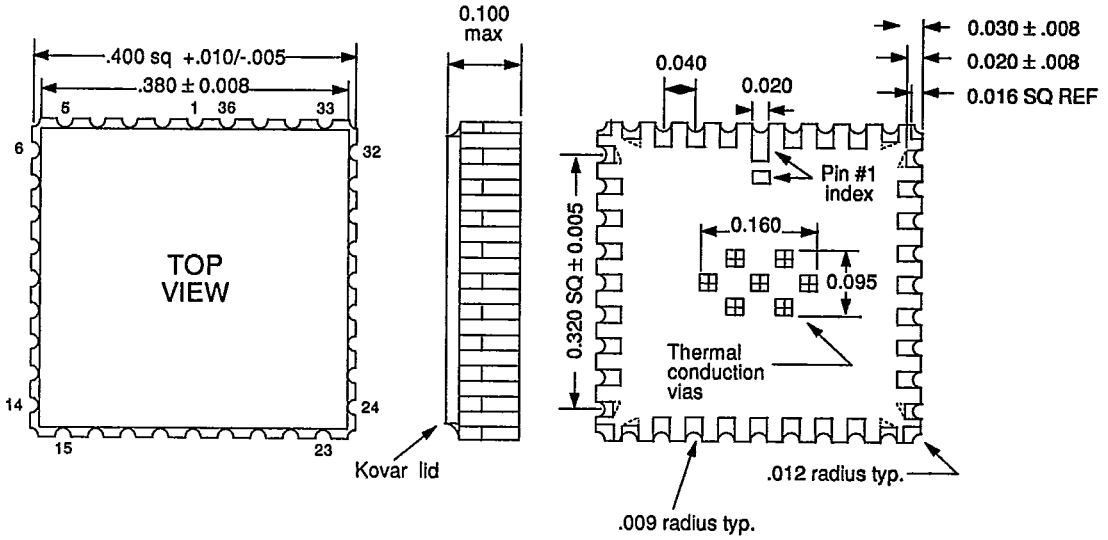
18 PIN LEADLESS CHIP CARRIER

TYPE L1



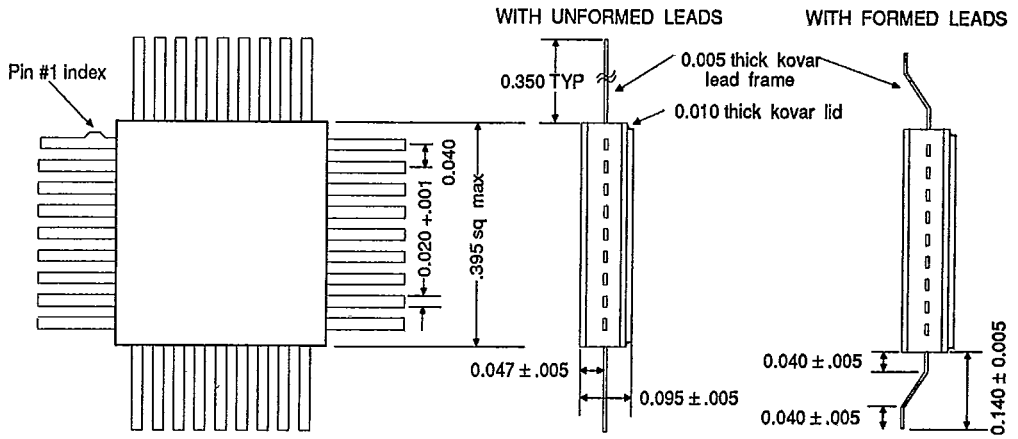
All dimensions shown in **inches** and (millimeters)

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



11

T-90-20

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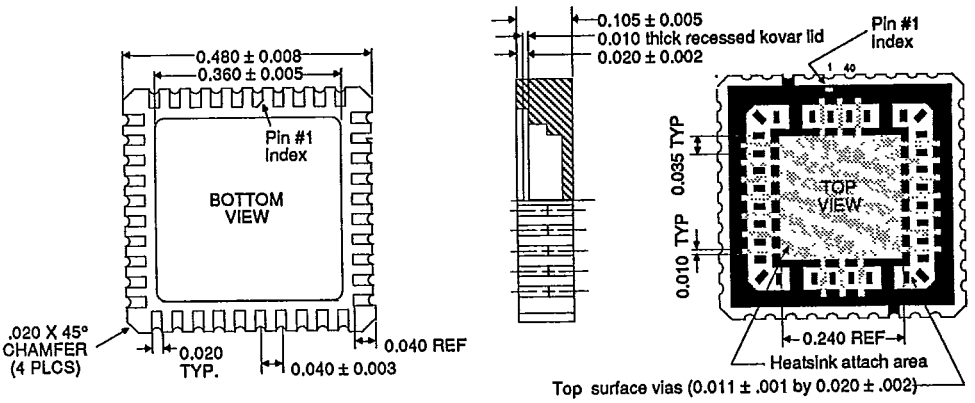
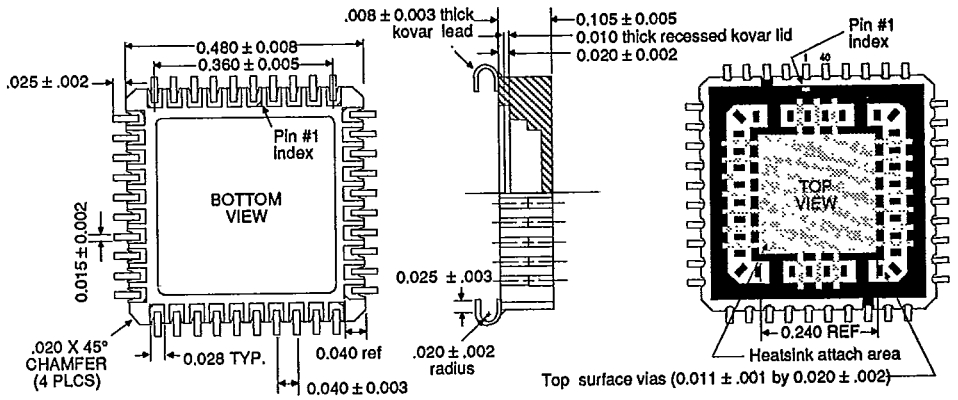
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

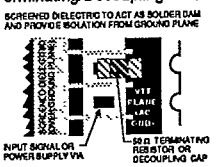


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:
Metalized Ceramic.....
Screened Dielectric.....
Bare Ceramic.....

Top Surface Terminating/Decoupling Detail



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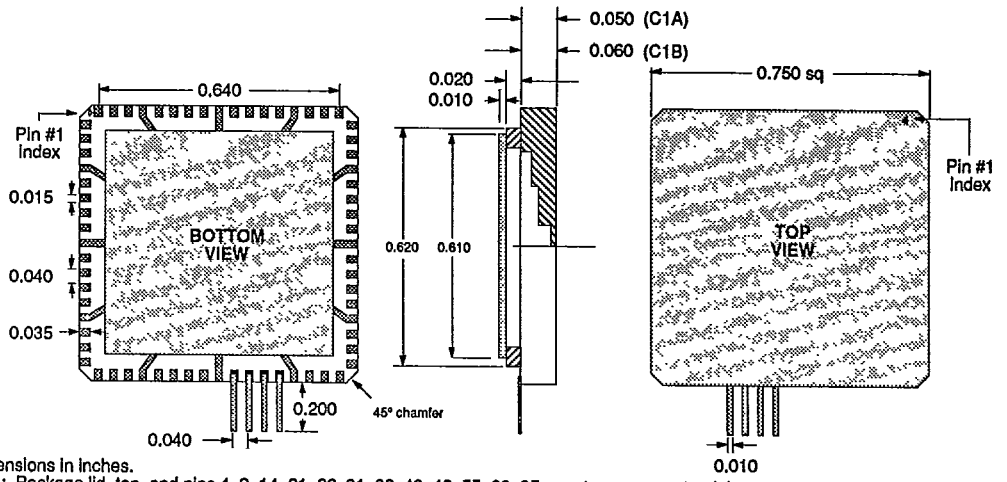
68 & 132 PIN PACKAGES

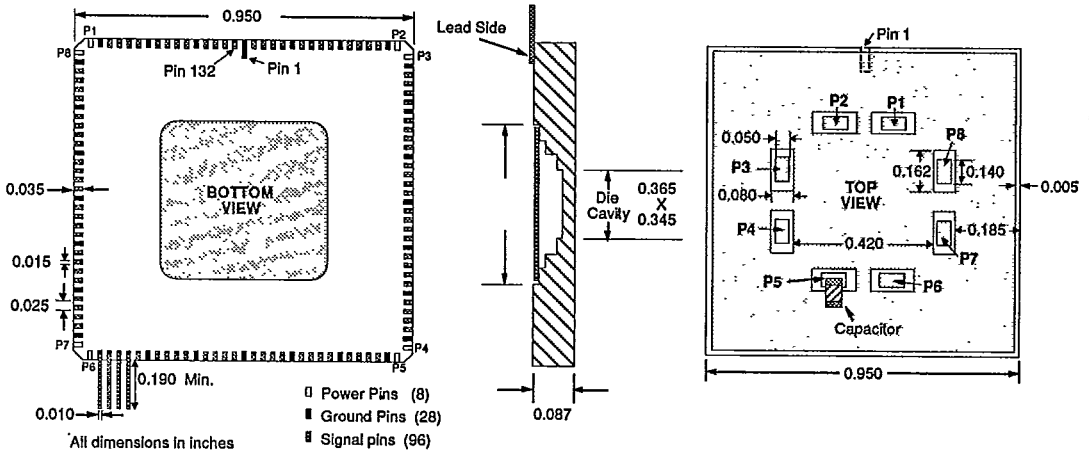
T-90-20

68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3



11