CMOS DDS Modulator

AD7008

FEATURES
Single +5 V Supply
32-Bit Phase Accumulator
On-Chip COSINE and SINE Look-Up Tables
On-Chip 10-Bit DAC
Frequency, Phase and Amplitude Modulation
Parallel and Serial Loading
Software and Hardware Power Down Options
20 MHz and 50 MHz Speed Grades
44-Pin PLCC

APPLICATIONS
Frequency Synthesizers
Frequency, Phase or Amplitude Modulators
DDS Tuning
Digital Demodulation

GENERAL DESCRIPTION

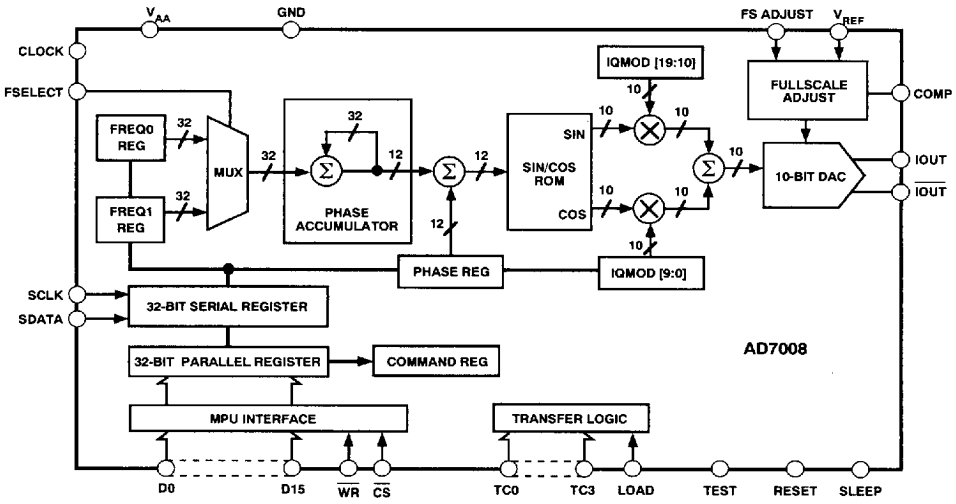
The AD7008 direct digital synthesis chip is a numerically controlled oscillator employing a 32-bit phase accumulator, sine and cosine look-up tables and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation, frequency modulation, and both in-phase and quadrature amplitude modulation suitable for SSB generation.

Clock rates up to 20 MHz and 50 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation may be effected by loading registers either through the parallel microprocessor interface or the serial interface. A frequency-select pin permits selection between two frequencies on a per cycle basis.

The serial and parallel interfaces may be operated independently and asynchronously from the DDS clock; the transfer control signals are internally synchronized to prevent metastability problems. The synchronizer can be bypassed to reduce the transfer latency in the event that the microprocessor clock is synchronous with the DDS clock.

A power-down pin allows external control of a power-down mode (also accessible through the microprocessor interface). The AD7008 is available in 44-pin PLCC.

FUNCTIONAL BLOCK DIAGRAM



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AD7008—SPECIFICATIONS[1] ($V_{AA} = V_{DD} = +5$ V ± 5%; $T_A = T_{MIN}$ to T_{MAX}, $R_{SET} = 390\ \Omega$, $R_{LOAD} = 51\ \Omega$ for IOUT and $\overline{IOUT}$, unless otherwise noted)

Parameter	AD7008AP20	AD7008JP50	Units	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS				
Resolution	10	10	Bits	
No. of Channels	1	1		
Update Rate (f_{MAX})	20	50	Msps max	
IOUT Full Scale	20	20	mA max	
Output Compliance	1	1	Volts max	
DC Accuracy				
Integral Nonlinearity	±1	±1	LSB typ	
Differential Nonlinearity	±1	±1	LSB typ	
DDS SPECIFICATIONS[2]				
Dynamic Specifications				
Signal-to-Noise Ratio	50	50	dB min	$f_{CLK} = f_{MAX}$, $f_{OUT} = 2$ MHz
Total Harmonic Distortion	−55	−53	dB min	$f_{CLK} = f_{MAX}$, $f_{OUT} = 2$ MHz
Spurious Free Dynamic Range (SFDR)[3]				
Narrow Band (±50 kHz)	−70	−70	dB min	$f_{CLK} = 6.25$ MHz, $f_{OUT} = 2.11$ MHz
Wide Band (±2 MHz)	−55	−55	dB min	
Power-Down Option	Yes	Yes		
VOLTAGE REFERENCE				
Internal Reference @ +25°C	1.27	1.27	Volts typ	
T_{MIN} to T_{MAX}	1.2/1.35	1.2/1.35	Volts min/max	
Reference TC	300	300	ppm/°C typ	
LOGIC INPUTS				
V_{INH}, Input High Voltage	V_{DD}–0.9	V_{DD}–0.9	V min	
V_{INL}, Input Low Voltage	0.9	0.9	V max	
I_{INH}, Input Current	10	10	μA max	
C_{IN}, Input Capacitance	10	10	pF max	
POWER SUPPLIES				
V_{DD}	4.75/5.25	4.75/5.25	V min/V max	
I_{AA}	26	26	mA typ	$R_{SET} = 390\ \Omega$
I_{DD}	22 + 1.5/MHz	22 + 1.5/MHz	mA typ	
$I_{AA} + I_{DD}$[4]	80	125	mA typ	SLEEP = 0 V; CR2 = 0 (AM Disabled)
	110	160	mA max	$f_{CLK} = f_{MAX}$
	10	20	mA max	SLEEP = V_{DD}

NOTES
[1]Operating temperature ranges as follows: A Version: −40°C to +85°C; J Version: 0°C to +70°C.
[2]All dynamic specifications are measured using IOUT. 100% Production tested.
[3]$f_{CLK} = 6.25$ MHz, Frequency Word = 5671C71C HEX, $f_{OUT} = 2.11$ MHz.
[4]With AM enabled (CR2 = 1), T_{MAX} should be limited as follows: AD7008AP20, $T_{MAX} = +70$°C; AD7008JP50, $T_{MAX} = +55$°C.
Specifications subject to change without notice.

TIMING CHARACTERISTICS (V_{AA} = V_{DD} +5 V ± 5%; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	AD7008AP20	AD7008JP50	Units	Test Conditions/Comments
t_1	50	20	ns min	CLOCK Period
t_2	20	8	ns min	CLOCK High Duration
t_3	20	8	ns min	CLOCK Low Duration
t_4	5	5	ns min	CLOCK to Control Setup Time
t_5	3	3	ns min	CLOCK to Control Hold Time
t_6	$4t_1$	$4t_1$	ns min	LOAD Period
t_7	$2t_1$	$2t_1$	ns min	LOAD High Duration
t_8	5	5	ns min	LOAD High to TC0–TC3 Setup Time
t_9	5	5	ns min	LOAD High to TC0–TC3 Hold Time
t_{10}	10	10	ns min	$\overline{WR}$ Rising to $\overline{CS}$ Low Setup Time
t_{11}	10	10	ns min	$\overline{WR}$ Rising to $\overline{CS}$ Low Hold Time
t_{12}	20	20	ns min	Minimum $\overline{WR}$ Low Duration
t_{13}	10	10	ns min	Minimum $\overline{WR}$ High Duration
t_{14}	3	3	ns min	$\overline{WR}$ to D0–D15 Setup Time
t_{15}	3	3	ns min	$\overline{WR}$ to D0–D15 Hold Time
t_{16}	20	20	ns min	SCLK Period
t_{17}	8	8	ns min	SCLK High Duration
t_{18}	8	8	ns min	SCLK Low Duration
t_{19}	10	10	ns min	SCLK Rising to SDATA Setup Time
t_{20}	10	10	ns min	SCLK Rising to SDATA Hold Time

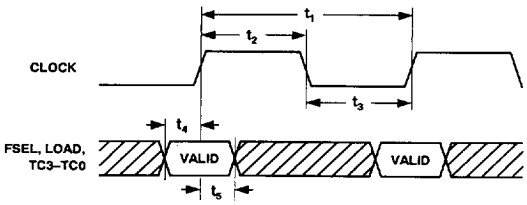

Figure 1. Clock Synchronization Timing

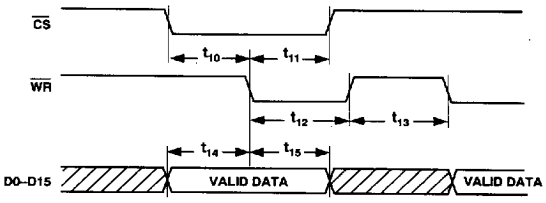

Figure 3. Parallel Port Timing

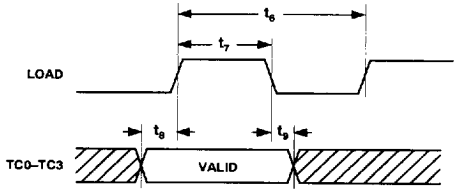

Figure 2. Register Transfer Timing

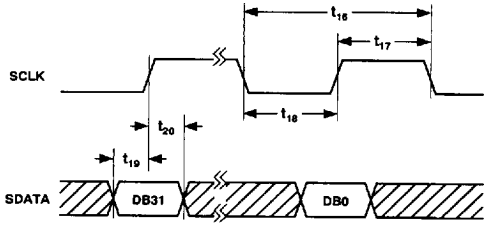

Figure 4. Serial Port Timing

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ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{AA}, V_{DD} to GND . . . . . −0.3 V to +7 V
AGND to DGND . . . . . −0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to AGND . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . −40°C to +85°C
Commercial (J Version) . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Junction Temperature . . . . . +115°C
PLCC θ_{JA} Thermal Impedance . . . . . +55°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD7008AP20	−40°C to +85°C	44-Pin PLCC	P-44A
AD7008JP50	0°C to +70°C	44-Pin PLCC	P-44A

*For outline information see Package Information section.

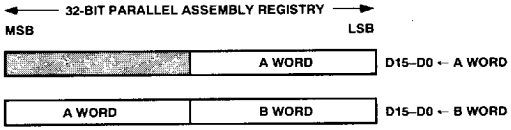


Figure 5. 16-Bit Parallel Port Loading Sequence

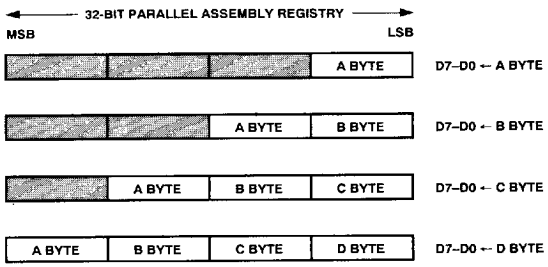
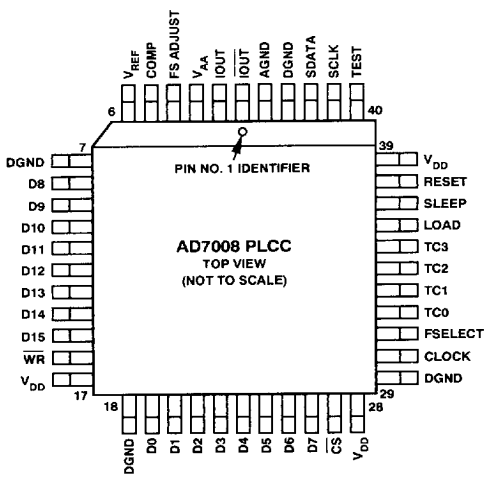


Figure 6. 8-Bit Parallel Port Loading Sequence

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7008 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
PLCC



PIN DESCRIPTION

Mnemonic	Function
POWER SUPPLY	
V_{AA}	Positive power supply for the analog section. A 0.1 μF decoupling capacitor should be connected between V_{AA} and AGND. This is +5 V ± 5 %.
AGND	Analog Ground.
V_{DD}	Positive power supply for the digital section. A 0.1 μF decoupling capacitor should be connected between V_{DD} and DGND. This is +5 V ± 5%. Both V_{AA} and V_{DD} should be externally tied together.
DGND	Digital Ground; both grounds should be externally tied together.
ANALOG SIGNAL AND REFERENCE	
IOUT, $\overline{IOUT}$	Current Output. This is a high impedance current source. A load resistor should be connected between IOUT and AGND. $\overline{IOUT}$ should be either tied directly to AGND or through an external load resistor to AGND.
FS ADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) is connected between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is as follows: $IOUT_{FULL\text{-}SCALE}\ (mA) = 6233 \times V_{REF}\ (V)/R_{SET}\ (\Omega)$
V_{REF}	Voltage Reference Input. A 0.1 μF decoupling ceramic capacitor should be connected V_{REF} and V_{AA}. There is an internal 1.27 voltage reference which can over driven by an external reference if required.
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF decoupling ceramic capacitor should be connected between COMP and V_{AA}.
DIGITAL INTERFACE AND CONTROL	
CLOCK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of this clock. Hence, the output frequency accuracy and phase noise is determined by this clock.
FSELECT	Frequency Select Input. FSELECT controls which frequency register, FREQ0 or FREQ1, is used in the phase accumulator. Frequency selection can be done on a cycle-per-cycle basis.
LOAD	Register load, active high digital Input. This pin, in conjunction with TC3–TC0, control loading of internal registers from either the parallel or serial assembly registers.
TC3–TC0	Transfer Control address bus, digital inputs. This address determines the source and destination registers that are used during a transfer. The source register can either be the parallel assembly register or the serial assembly register. The destination register can be any of the following: COMMAND REG, FREQ0 REG, FREQ1 REG, PHASE REG or IQMOD REG. TC3-TC0 should be valid prior to LOAD rising and should not change until LOAD falls.
$\overline{CS}$	Chip Select, active low digital input. This input in conjunction with $\overline{WR}$ is used when writing to the parallel assembly register.
$\overline{WR}$	Write, active low digital input. This input in conjunction with $\overline{CS}$ is used when writing to the parallel assembly register.
D7–D0	Data bus, digital inputs. This represent the low byte of the 16-bit data input port used to write to the 32-bit parallel assembly register. The databus can configured for either a 8-bit or 16-bit MPU/DSP ports.
D15–D8	Data Bus, Digital Inputs. This represent the high byte of the 16-bit data input port used to write to the 32-bit parallel assembly register. The databus can configured for either a 8-bit or 16-bit MPU/DSP ports. When the databus is configured for 8-bit operation, D8–D15 should be tied to DGND.
SCLK	Serial Clock, digital input. SCLK is used, in conjunction with SDATA, to clock data into the 32-bit serial assembly register.
SDATA	Serial Data, digital input. Serial data is clocked on the rising edge of SCLK, Most Significant Bit (MSB) first.
SLEEP	Low power sleep control, active high digital input. SLEEP puts the AD7008 into a low power sleep mode. Internal clocks are disable while also turning off the DAC current sources. A SLEEP bit is also provided in the COMMAND REG to put the AD7008 into a low power sleep mode.
RESET	Register Reset, active high digital input. RESET clears the COMMAND REG and all the modulation registers to zero.
TEST	Test Mode. This used for factory test only and should be left as a No Connect.

CIRCUIT DESCRIPTION

In contrast to previous direct digital synthesizer devices, the AD7008 provides an exciting new level of integration for the RF/Communications system designer. The AD7008 combines the numerical controlled oscillator (NCO), SIN/COSINE look-up tables, frequency, phase and IQ modulators, and a digital-to-analog converter on a single integrated circuit.

The internal circuitry of the AD7008 consists of four main sections. These are

Numerical Controlled Oscillator (NCO) + Phase Modulator
SIN and COSINE look up tables
In Phase and Quadrature Modulators
Digital-to-Analog Converter

Numerical Controlled Oscillator + Phase Modulator

This consists of two frequency select registers, a phase accumulator and a phase offset register. The main component of the NCO is a 32-bit phase accumulator which accumulates a phase step on every clock cycle. The value of the phase step determines how many clocks cycles are required for the phase accumulator to count 2π radians (i.e., one cycle of the output frequency). The output frequency, f_{OUT}, is given by:

$$f_{OUT} = \frac{Phase\ Step}{2\pi} f_{CLOCK} = \frac{\Delta\ Phase}{2^{32}} f_{CLOCK}$$

$$0 \leq \Delta\ Phase \leq 2^{32} - 1$$

The input to the phase accumulator (i.e., the phase step) can be selected either from the FREQ0 Register or FREQ1 Register and this is controlled by the FSELECT pin. This allows binary frequency shift keying to be easily implemented. The two FSK frequencies can be loaded into FREQ0 and FREQ1 and selected using the FSELECT pin. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. More complex frequency modulation schemes, such as GMSK, can be implemented by updating the contents of these registers.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit PHASE Register. The contents of this register are added to the most significant bits of the NCO.

Sin and Cosine Look-Up Tables (LUT)

The output of the phase accumulator is converted to an amplitude signal by means of an Sine/Cosine ROM LUT. Although the NCO contains a 32-bit phase accumulator, the output of the NCO is truncated to 12-bits. Using the full resolution of the phase accumulator is both impractical and unnecessary as this would require a look-up table of 2^{32} entries.

It is necessary only to have sufficient phase resolution in the LUTs such that the dc error of the output waveform is dominated by the quantization error in the DAC. This requires the look-up tables to have two more bits of phase resolution than the 10-bit DAC.

In Phase and Quadrature Modulators

Two 10-bit amplitude multipliers are provided allowing the easy implementation of either Quadrature Amplitude Modulation (QAM) or Amplitude Modulation (AM). The 20-bit IQMOD Register is used to control the amplitude of the I (cosine) and Q (sine) signals. IQMOD[9–0] controls the I amplitude and IQMOD[19–10] controls the Q amplitude.

The user should ensure that when summing the I and Q signals the result should not exceed 10-bits, as there is no internal clipping logic to prevent overflow.

When amplitude modulation is not required, the IQ multipliers can be bypassed (CR2 = 0). The sine output is directly sent to the 10-bit DAC.

Digital-to-Analog Converter

The AD7008 include a high impedance current source 10-bit DAC, capable of driving wide range of loads at different speeds. Full-scale output current can be adjusted, for optimum power and external load requirements, through the use of a single external resistor (R_{SET}).

The DAC can be configured for single or differential ended operation. $\overline{I_{OUT}}$ can be either tied directly to AGND for single ended operation or through external load resistor.

MPU Interface

The chip contains two 32-bit assembly registers, one for parallel bus data, and one for serial input data. Each of the modulation registers can be loaded from either assembly register under control of the LOAD pin and the Transfer-Control (TC) pins (See Table I). The Command register can only be loaded from the parallel assembly register.

Table I. Source and Destination Registers

TC3	TC2	TC1	TC0	LOAD	Source Register	Destination Register
X	X	X	X	0	N/A	N/A
0	0	X	X	1	Parallel	COMMAND
1	0	0	0	1	Parallel	FREQ0
1	0	0	1	1	Parallel	FREQ1
1	0	1	0	1	Parallel	PHASE
1	0	1	1	1	Parallel	IQMOD
1	1	0	0	1	Serial	FREQ0
1	1	0	1	1	Serial	FREQ1
1	1	1	0	1	Serial	PHASE
1	1	1	1	1	Serial	IQMOD

Table II. AD7008 Control Registers

Register	Size	Reset State	Description
COMMAND REG	4 Bits CR3–CR0	All Zeros	Command Register. This is written to using the parallel assembly register.
FREQ0 REG	32 Bits DB31–DB0	All Zeros	Frequency Select Register 0. This defines the output frequency, when FSELECT = 0, as a fraction of the CLOCK frequency.
FREQ1 REG	32 Bits DB31–DB0	All Zeros	Frequency Select Register 1. This defines the output frequency, when FSELECT = 1, as a fraction of the CLOCK frequency.
PHASE REG	12 Bits DB11–DB0	All Zeros	Phase Offset Register. The contents of this register is added to the output of the phase accumulator.
IQMOD REG	20 Bits DB19–DB0	All Zeros	I and Q Amplitude Modulation Register. This defines the amplitude of the I and Q signals as 10-bit two complement binary fractions. DB[19:10] is multiplied by the Quadrature (sine component and DB[9:0] is multiplied by the In-Phase (cosine) component.

Table III. Command Register Bits

CR0	=0	Eight-Bit Databus. Pins D15–D8 are ignored and the parallel assembly register shifts eight places left on each write. Hence four successive writes are required to load the 32-bit parallel assembly register, Figure 6.
	=1	Sixteen-Bit Databus. The parallel assembly register shifts 16 places left on each write. Hence two successive writes are required to load the 32-bit parallel assembly register, Figure 5.
CR1	=0	Normal Operation.
	=1	Low Power Sleep Mode. Internal Clocks and the DAC current sources are turn off.
CR2	=0	Amplitude Modulation Bypass. The output of the sine LUT is directly sent to the DAC.
	=1	Amplitude Modulation Enable. IQ modulation is enabled allowing AM or QAM to be performed.
CR3	=0	Synchronizer Logic Enabled. The FSELECT, LOAD and TC3–TC0 signals are passed through a 4-stage pipeline to synchronize them with the CLOCK frequency, avoiding metastability problems.
	=1	Synchronizer Logic Disabled. The FSELECT, LOAD and TC3–TC0 signals bypass the synchronization logic. This allows for faster response to the control signals.

TC3–TC0 should be set up and stable before LOAD rises, and should not change until after LOAD falls.

The microprocessor asserts both $\overline{WR}$ and $\overline{CS}$ to load the parallel assembly register. At the end of each write, the parallel assembly register is shifted left by 8 or 16 bits (depending on CR0), and the new data is loaded into the low bits. Hence, two 16-bit writes or four 8-bit writes are used to load the parallel assembly register. When loading parallel data destined for the phase or IQ registers, it is only necessary to write as much data as will be used by that register. For instance, the Command Register requires only one write to the parallel assembly register.

Serial data is input to the chip on the rising edge of SCLK, most significant bit first. The data in the assembly registers can be transferred to the modulation registers by means of the transfer control pins.

APPLICATIONS

The AD7008 can be used in a wide range of communication applications ranging from digital mobile radio, to frequency agile Wireless Local Area Networks (WANs), to SSB telephony.

For digital mobile radio applications the chip provides direct synthesis and phase modulation capabilities to 20 MHz in a single low power, low cost part.

For WANs a wide range of modulation capabilities allow a system developer to optimize modulation bandwidth and noise immunity.

In the area of SSB telephony (military, commercial and amateur), the chip provides the first single chip implementation of a phasing type SSB generator. Combined with a single chip DSP (ADSP-2101) implementing the speech input and Hilbert transform, the AD7008 forms a two-chip direct SSB generation capability to over 20 MHz.

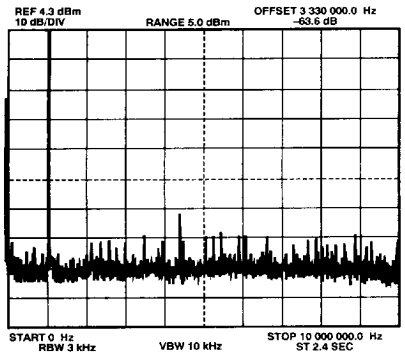


Figure 7. f_{CLK} = 20 MHz, f_{OUT} = 1.1 MHz

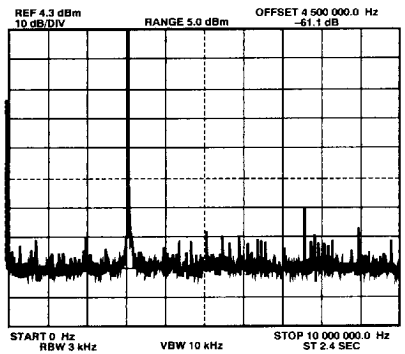


Figure 8. f_{CLK} = 20 MHz, f_{OUT} = 3.1 MHz

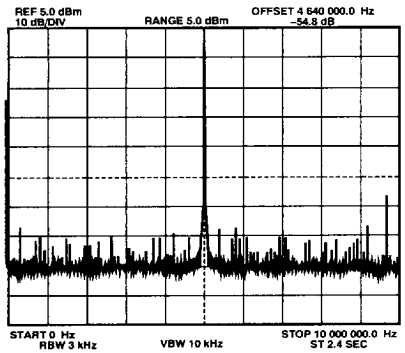


Figure 9. f_{CLK} = 20 MHz, f_{OUT} = 5.1 MHz

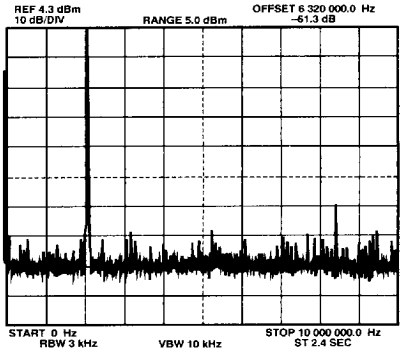


Figure 10. f_{CLK} = 20 MHz, f_{OUT} = 2.1 MHz

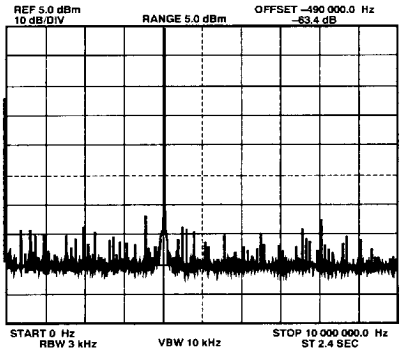


Figure 11. f_{CLK} = 20 MHz, f_{OUT} = 4.1 MHz

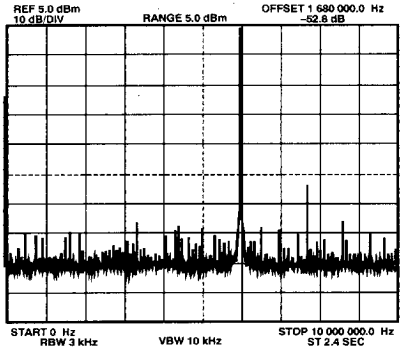


Figure 12. f_{CLK} = 20 MHz, f_{OUT} = 6.1 MHz

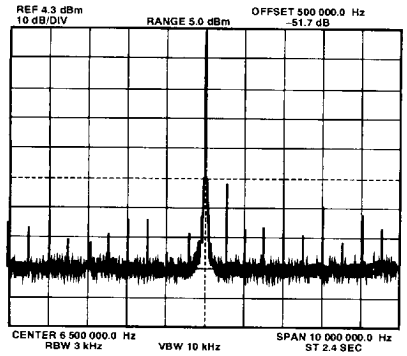


Figure 13. f_{CLK} = 20 MHz, f_{OUT} = 6.5 MHz

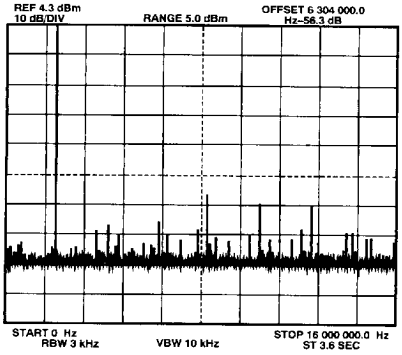


Figure 14. f_{CLK} = 50 MHz, f_{OUT} = 2.1 MHz

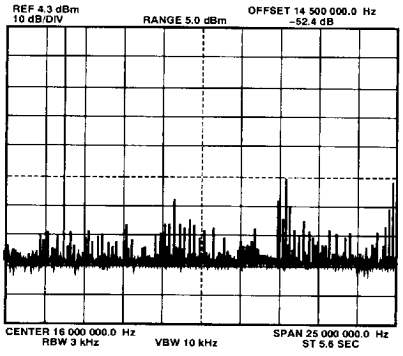


Figure 15. f_{CLK} = 50 MHz, f_{OUT} = 7.1 MHz

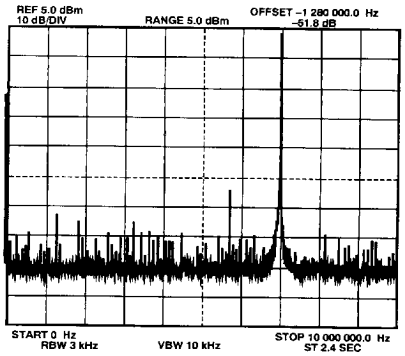


Figure 16. f_{CLK} = 20 MHz, f_{OUT} = 7.1 MHz

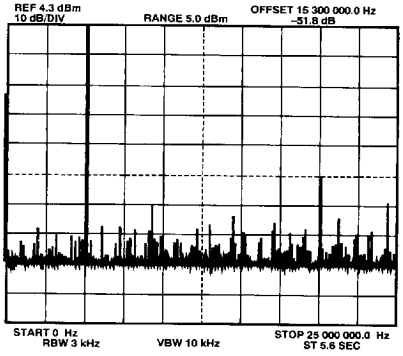


Figure 17. f_{CLK} = 50 MHz, f_{OUT} = 5.1 MHz

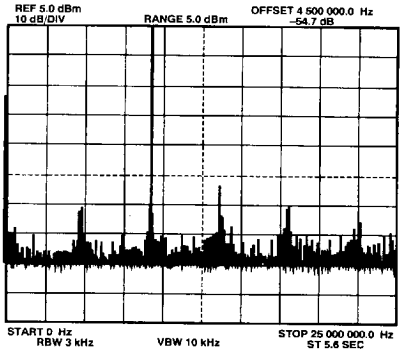


Figure 18. f_{CLK} = 50 MHz, f_{OUT} = 9.1 MHz

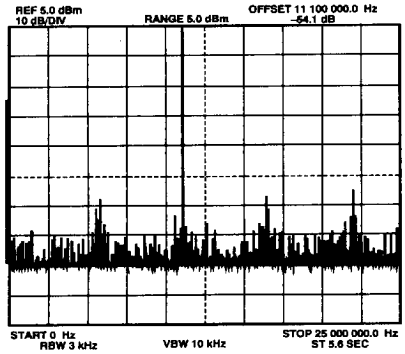


Figure 19. f_{CLK} = 50 MHz, f_{OUT} = 11.1 MHz

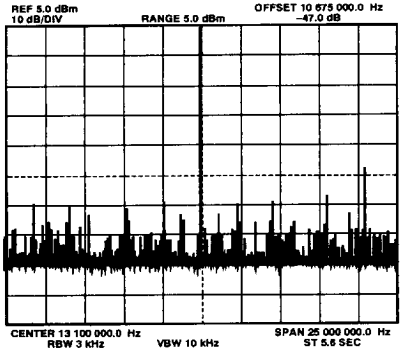


Figure 20. f_{CLK} = 50 MHz, f_{OUT} = 13.1 MHz

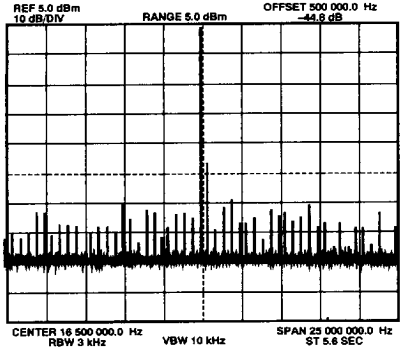


Figure 21. f_{CLK} = 50 MHz, f_{OUT} = 16.5 MHz

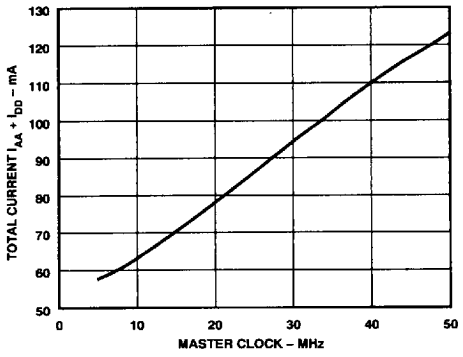


Figure 22. Typical Current Consumption vs. Frequency

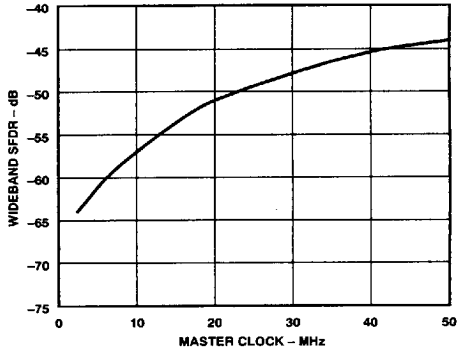


Figure 23. Typical Plot of SFDR vs. Master Clock Frequency When f_{OUT} = 1/3f_{CLK}, Frequency Word = 5671C71C HEX