Preliminary

Am2080/Am2080B

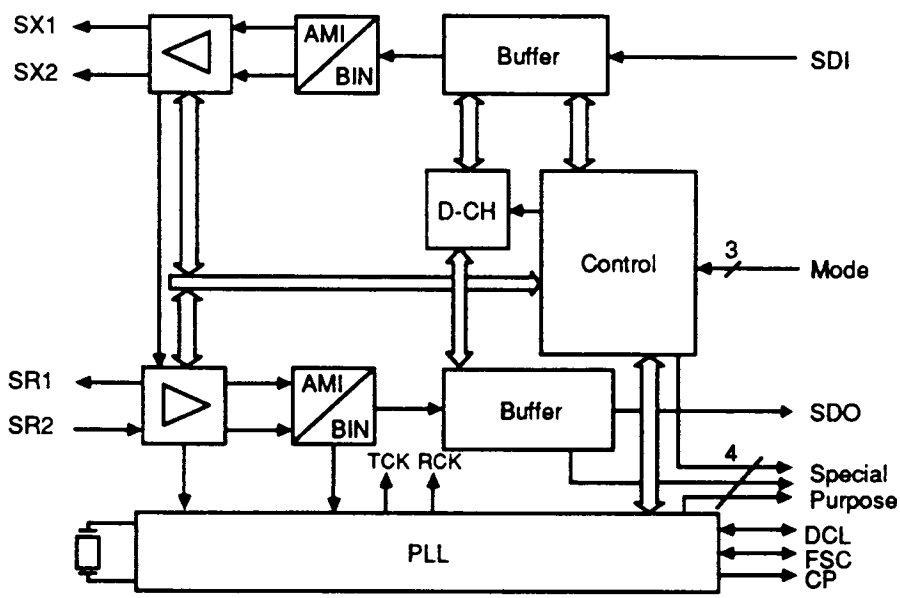
S-Bus Interface Circuit (SBC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Full duplex 2B + D S/T-interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T and IOM™ interfaces
- D-channel access control
- Activation and deactivation procedures according to CCITT I.430
- Built-in wake-up unit for activation from power-down state
- Adaptively switched receive thresholds
- Control via IOM interface
- NT, TE and LT operating modes
- Receive timing recovery according to selected operating mode
- Frame alignment with absorption of phase wander in trunk line applications
- Switching of test loops
- Advanced CMOS technology
- Low power consumption:
  –standby less than 5 mW
  –active max 65 mW

BLOCK DIAGRAM



11135-001A

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GENERAL DESCRIPTION

The Am2080 S-Bus Interface Circuit (SBC™) implements the four-wire S/T-interface used to link voice/data terminals to an ISDN. Through selection of operating mode, the device may be employed in all types of applications involving an S-interface. In particular, two or more SBCs can be used to build a point-to-point, passive bus, extended passive bus, or star configuration.

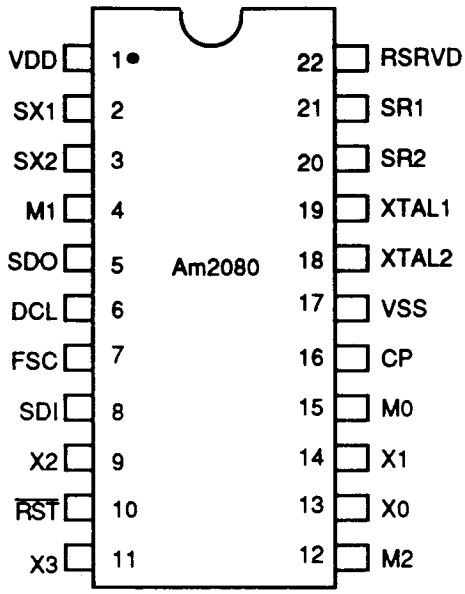
Specific ISDN applications of the SBC include: ISDN terminals, ISDN network termination (central office and PABX applications), and PABX trunk lines to central office.

The device provides all electrical and logical functions according to CCITT recommendation I.430. These include mode-dependent receive timing recovery, D-channel access and priority control, and automatic handling of activation/deactivation procedures. The SBC does not require direct microprocessor control.

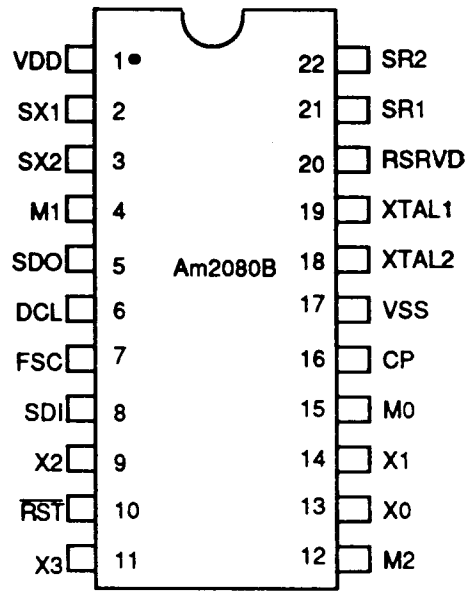
The SBC is an IOM compatible, 22-pin CMOS device. It operates from a single +5-V supply and features a power-down state with very low-power consumption.

CONNECTION DIAGRAMS
Top View

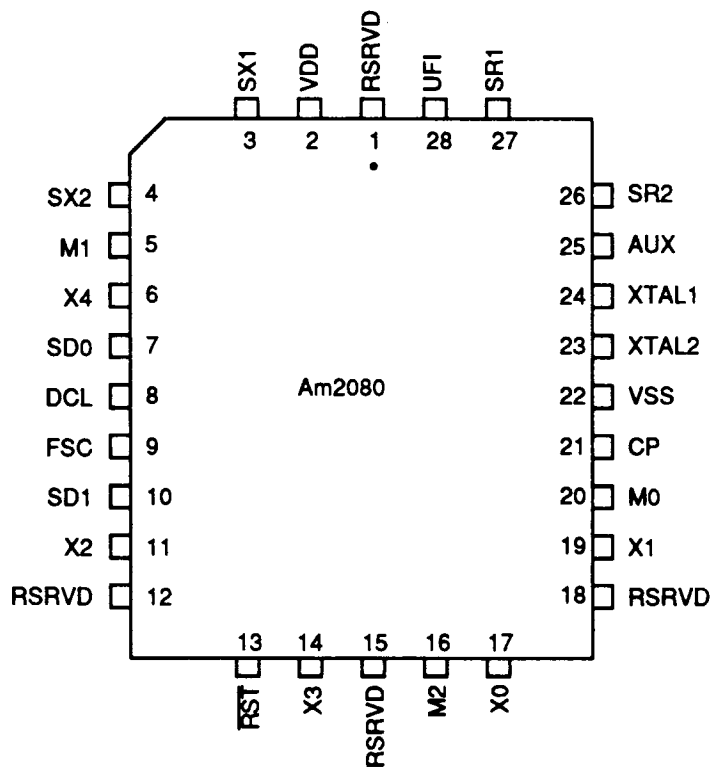
22-Pin DIP



22-Pin DIP

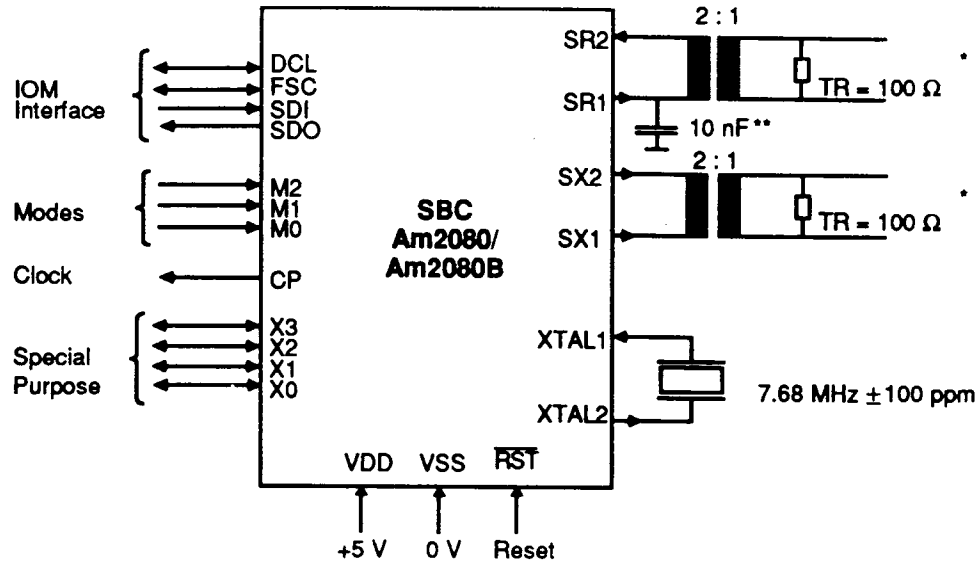


28-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



*Terminating resistors only at the far ends of the connection. (See Figure 2.)
**Required only for Am2080, not necessary for Am2080B.

11135-03A

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number/Description
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM2080/ AM2080B — P — C — B

e. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to + 70°C)

c. PACKAGE TYPE
P = 22-Pin Plastic Dip (PD 022)
J = 28-Pin Plastic Leaded Chip Carrier (PLR 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am2080
S-Bus Interface Circuit (SBC)

Valid Combinations	
AM2080	PC, JC, PCB, JCB
AM2080B	PC ,PCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

AUX
Auxiliary (Input)

VCC or ground to be applied. Available in PLCC only.

CP
(Input/Output)

Clock pulses, depending on selected operating mode; CP provides synchronous clocks.

DCL
Serial Data Clock, IOM Interface (Input/Output)

FSC
Frame Sync, IOM Interface (Input/Output)

M2–M0, X3
Mode (Inputs)

Selects operating mode.

$\overline{\text{RST}}$
Reset, Active Low (Input)

SDI
Serial Data In, IOM Interface (Input)

SDO
Serial Data Out, IOM Interface (Output)

SR1
S-Bus Receiver (Output)

2.5-V reference output.

SR2
S-Bus Receiver (Input)

Signal input.

SX1
S-Bus Transmitter (Positive Output)

SX2
S-Bus Transmitter (Negative Output)

UFI
User Filter (Output)

Opamp output connection for external pre-filter for S-Bus receiver, if used. Available in PLCC only.

VDD
(Input)

Power supply, +5 V ±5%.

VSS
(Input)

Power supply, ground.

X2–X0
Special Purpose (Inputs/Outputs)

Functions depend on the selected operating mode; see Operating Modes section.

X4
External Filter Selection, Active Low (Input)

Must be tied Low (0) if external pre-filter for S-Bus receiver is used (pin UFI).

XTAL1
(Input)

Connection for external crystal or input for external clock generator.

XTAL2
(Output)

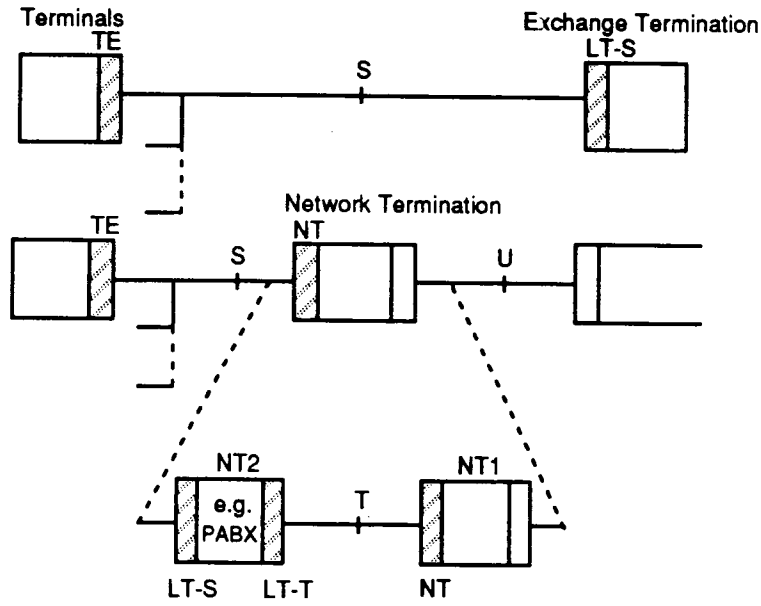
Connection for external crystal, not connected when external clock generator is used.

SYSTEM INTEGRATION

The SBC implements the four-wire S and T interfaces used in the ISDN basic access. It may be used at both ends of these interfaces. The applications include:

- ISDN terminals (TE)
- ISDN network termination (NT)
- ISDN subscriber line termination (LT-S)
- ISDN trunk line termination (LT-T) (PABX connection to Central Office)

These applications are shown in Figure 1 where the usual nomenclature as defined by the CCITT for the basic access functional blocks and reference points has been used.



Note: Shaded areas indicate where SBC can be used.

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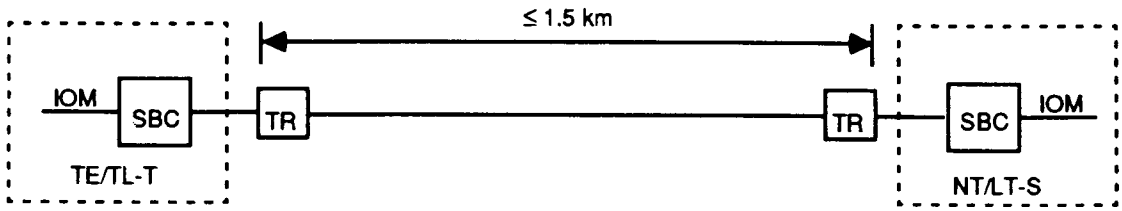
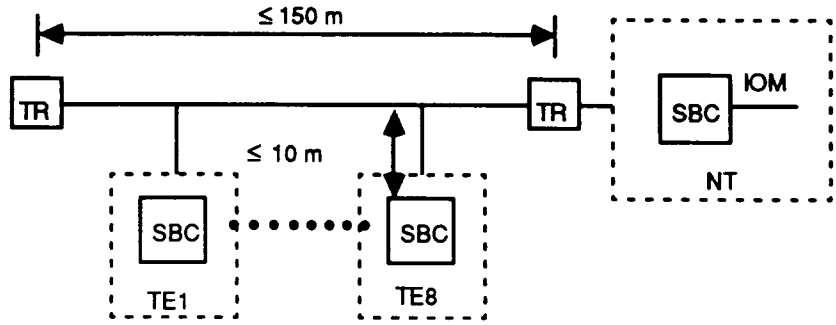
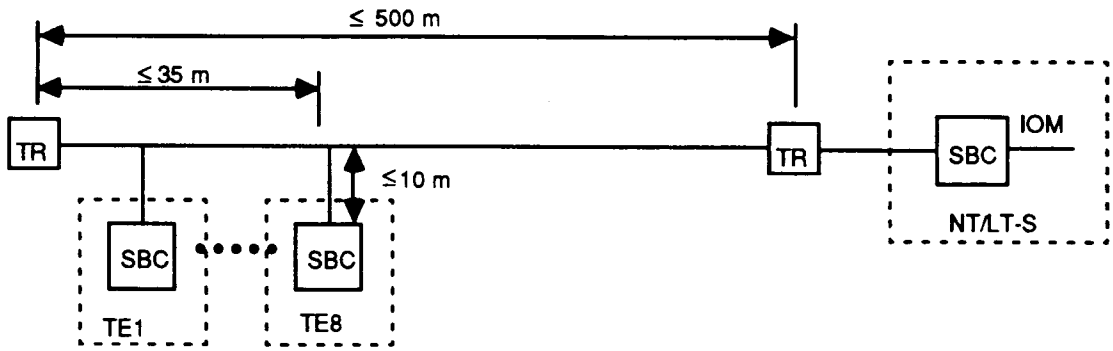
Figure 1. Applications of the Am2080 SBC



Point-to-point Configuration



Short Passive Bus Configuration

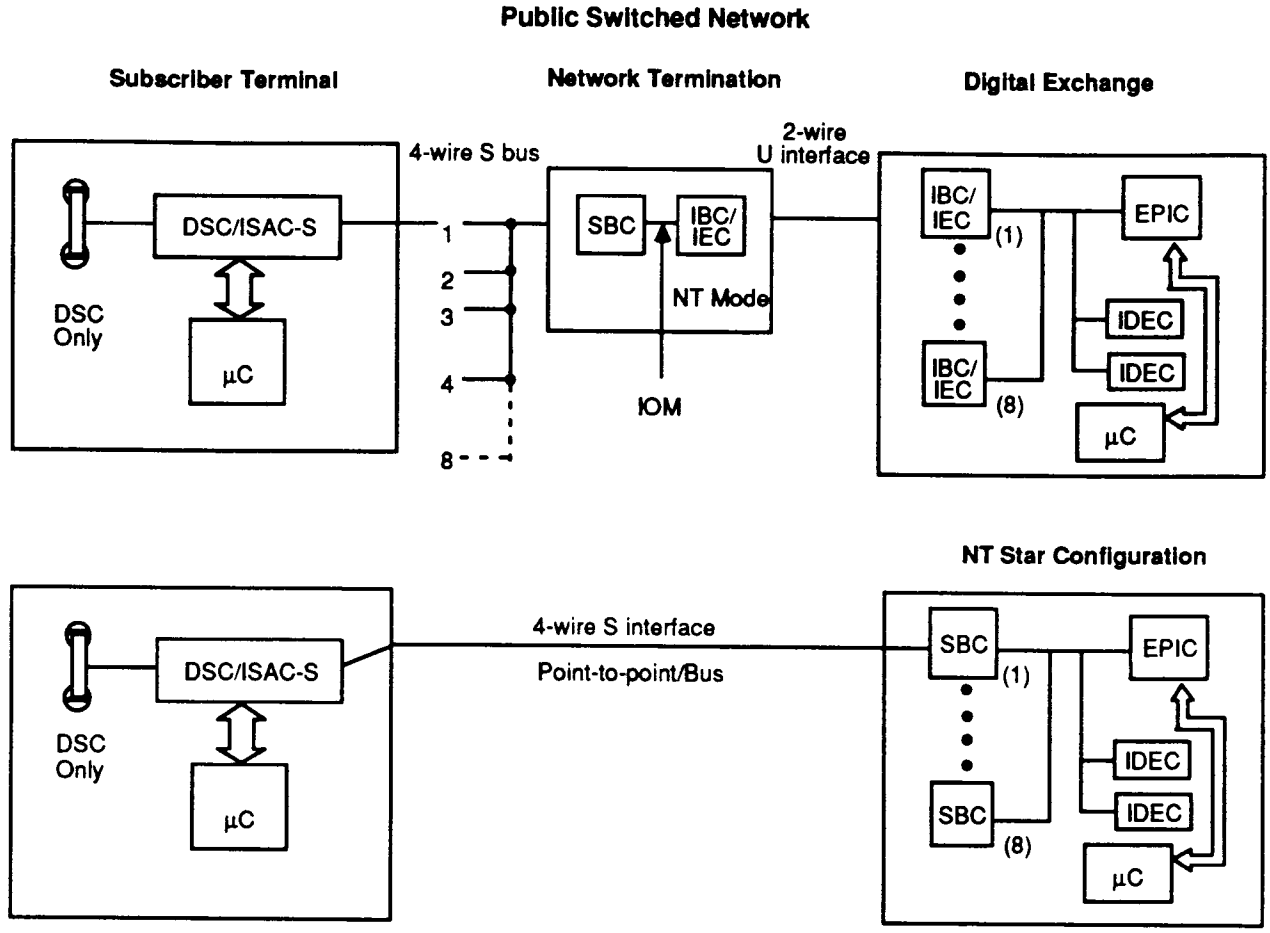


Extended Passive Bus Configuration

Figure 2. Some S-Interface Wiring Configurations 11135-005A

Some of the wiring configurations possible with the SBC for the S-interface are shown in Figure 2 with approximate typical distances. TR stands for terminating resistor of value 100 ohms.The maximum line attenuation tolerated by the SBC is 10 dB at 96 kHz.

Figure 3 gives an example of an application of the SBC in an IOM (ISDN Oriented Modular) architecture. By separate implementation of OSI Layer 1 and Layer 2 functions, and through unified control procedures, the architecture provides flexibility with respect to various transmission techniques. The IOM devices are all low-power, high-integration, single +5 V supply CMOS devices. Through mode switching, each device may be used in several applications. With one limited set of devices, all ISDN basic access configurations are covered. Note that none of the compatible Layer 1 devices (SBC, IBC™, IEC™) require direct microprocessor control. The IOM interface provides all necessary communication functions.



DSC	Am79C30A	Digital Subscriber Controller™
EPIC™	Am2055	Extended PCM Interface Controller
IBC	Am2095	ISDN Burst Transceiver Circuit
IDEC™	Am2075	ISDN D-channel Exchange Controller
IEC	Am2090	ISDN Echo Cancellation Circuit
ISAC-S™	Am2085	ISDN Subscriber Access Controller
SBC	Am2080	S-Bus Interface Circuit

Figure 3. ISDN Oriented Modular (IOM) Architecture

11135-006B

FUNCTIONAL DESCRIPTION

The Am2080 S-bus interface circuit performs the OSI Layer 1 functions for the S/T interface of the ISDN basic access.

General Functions and Device Architecture

The common functions for all operating modes are:

- Line transceiver functions for the S interface according to the electrical specifications of CCITT I.430.
- Dynamically adaptive threshold control for the receiver.
- Conversion of the frame structure between IOM and S interfaces.
- Code conversion from/to binary to/from Alternate Mark Inversion.

Mode-specific functions are:

- Receive timing recovery.
- S-interface timing generation using IOM timing synchronous to system, or vice versa.
- D-channel access control and priority handling.
- D-channel echo bit generation.
- Activation/deactivation procedures, triggered by primitives received over the IOM interface or by INFOs received from the line.
- Frame alignment according to CCITT Q.503.
- Execution of test loops.

Analog Functions

The full-bauded pseudo-ternary pulse shaping is achieved with the integrated transmitter which is realized as a current limited voltage source. A voltage of 2.1 V is delivered between SX2–SX1, which yields a current of 7.5 mA over 280 ohms.

The receiver is designed as a threshold detector with adaptively switched threshold levels. Pin SR1 delivers 2.5 V as an output, which is the virtual ground of the input signal on pin SR2.

An external transformer of ratio 2:1 is needed in both receive and transmit direction to provide for isolation and transform voltage levels according to CCITT recommendations.

Digital Functions

A DPLL circuitry working with a frequency of 7.68 MHz ±100 ppm serves to generate the 192-kHz line clock from the reference clock delivered by the network and to extract the 192-kHz line clock from the receive data stream.

The 7.68-MHz clock may be generated with the use of external crystal between pins XTAL1 and XTAL2. It may also be provided by an external oscillator, in which case XTAL2 is left unconnected.

The Control (Block Diagram) block includes the logic to detect OSI Layer 1 commands and to communicate with external Layer 1 or Layer 2 devices via the IOM interface.

An incorporated finite state machine controls ISDN OSI Layer 1 activation/deactivation.

The D-channel access procedure according to CCITT I.430, including priority management, is fully implemented in the SBC. When used as an S-bus master in a multipoint configuration, the device generates the echo bits necessary for D-channel collision detection. In the NT-mode, the echo channel may be made externally available through an auxiliary pin and thus "Intelligent NTs" (star configuration) may be implemented.

In terminal applications (TE) the Q channel as specified by I.430 is supported. The SBC sends a binary 1 in FA bit position to allow another terminal to use the extra transmission capacity.

The buffer memory serves to adapt the different bit rates of the S and IOM interfaces. In addition, in trunk line applications it absorbs the possible deviation between two system clocks, according to CCITT Q.503 (slip detection).

Operating Modes

The operating modes are determined by pin strapping on pins M0 to M2. The four basic operating modes are: TE, NT, LT-S, and LT-T. In three of these operating modes, the IOM timing mode may be programmed. To see which IOM timing modes are applicable in the four basic operating modes, refer to Table 1. The functions of the operating mode-specific pins are given in Table 1 as well.

Depending on the selected mode, pins CP, X2, and X1 provide auxiliary clocks, either asynchronous or synchronous to the S-interface as shown in Table 2. These auxiliary clocks may be used to drive; e.g., a codec filter or microprocessor system (TE applications). The other uses of the auxiliary pins are listed in Table 3.

Table 1. Operating Modes and Functions of Mode-Specific Pins of the Am2080 SBC

Application	Operation of IOM Interface	M2	M1	M0	DCL	FSC	CP	X3	X2	X1	X0
TE	Inverted Mode	0	0	0	O:512 kHz*	O:8 kHz*	O:1536 kHz*	I:$\overline{\text{ENCK}}$	O:2560 kHz	O:3840 kHz	O:RDY
TE	Inverted Mode	0	0	1	O:512 kHz*	O:8 kHz*	O:1536 kHz*	I:$\overline{\text{ENCK}}$	O:1280 kHz	O:3840 kHz	O:RDY
TE	IOM-1 Mode	0	1	0	O:512 kHz*	O:8 kHz*	O:512 kHz*	I:$\overline{\text{ENCK}}$	O:ECHO	O:3840 kHz	I:CON
LT-T	IOM-2 Mode or Inverted MUX Mode	0	1	1	I:4096 kHz	I:8 kHz	O:512 kHz*	I:fixed at 1	I:TS2	I:TS1	I:TS0
LT-T	IOM-1 Mode	0	1	1	I:512 kHz	I:8 kHz	O:512 kHz*	I:fixed at 0	I:fixed at 0	I:fixed at 0	I:CON
NT	IOM-1 Mode	1	1	1	I:512 kHz	I:8 kHz	I:$\overline{\text{SCZ}}$	I:BUS	I:$\overline{\text{SSZ}}$	I:DEX	I/O:DE
LT-S	IOM-2 Mode or Inverted MUX Mode	1	0	0	I:4096 kHz	I:8 kHz	I:fixed at 0	I:BUS	I:TS2	I:TS1	I:TS0
LT-S	IOM-1 Mode	1	1	0	I:512 kHz	I:8 kHz	I:fixed at 0	I:BUS	I:fixed at 0	O:7680 kHz	I:fixed at 0
LT-S	IOM-1 Mode	1	1	0	I:512 kHz	I:8 kHz	I:fixed at 0	I:BUS	O:192 kHz*	O:7680 kHz	I:fixed at 1

*Synchronized to S
I: Input
O: Output

BUS	Bus configuration specified
CON	Connected to S-bus
DE	D-channel echo bits in NT star configuration
DEX	D-channel echo external/internal
ECHO	E-bits reproduces
$\overline{\text{ENCK}}$	Enable clock at all times
RDY	D-channel status on S-interface
$\overline{\text{SCZ}}$	Send continuous binary zeros (96 kHz) (if CP = 0)
$\overline{\text{SSZ}}$	Send single binary zeros (2 kHz)
TS2–0	Timeslot number on IOM

Table 2. Auxiliary Clock Sources

Clock Rate	Clock Source
3840 kHz 2560 kHz 1280 kHz	Clocks derived from the 7680-kHz crystal
1536 kHz 512 kHz	Clocks synchronized to S-interface

Table 3. Auxiliary Pin Non-Clock Functions

Function	I/O Type	Description
BUS	Input	At 1, specifies a bus configuration (as opposed to point to point or extended passive bus); in NT and LT-S modes, pin X3.
CON	Input	Connected. At 0, prevents the SBC from activating and transmitting on the S-interface. Indicates whether or not the device is connected to the S-interface; X0 in TE and LT-T modes.
DE	Input/Output Open Drain with Integrated Pull-Up Resistor	D-channel Echo. The DE outputs should be tied together (open-drain) in an NT star configuration, to obtain the global echo bit; X0 in NT mode.
DEX	Input	External D-channel echo enable. At 1, makes the E-bit dependent on the DE (X0) input. Used in NT mode to build a star configuration; X1 in NT mode.
ECHO	Output Push-Pull	Reproduces the E-bits received from the S interface synchronously to IOM frame D-bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary 1, in TE mode, pin X2.
$\overline{\text{ENCK}}$	Input	Enable clock. At 0, forces the SBC to deliver IOM timing at all times, regardless of SDI input level; in TE mode, pin X3.
RDY	Output Push-Pull	Ready. Provides a signal logically equal to bit 3 of Monitor channel. Signals the D-channel status (0 = occupied, 1 = free) to Layer 2 component; X0 in TE mode.
$\overline{\text{SSZ}}$	Input	Send single zeros. At 0, forces the SBC to transmit alternating pulses at 250-µs intervals (period 2 kHz) on S-interface for test purposes; X2 in NT mode.
$\overline{\text{SCZ}}$	Input	Send continuous zeros. At 0, forces the the SBC to transmit alternating pulses at 96 kHz on S-interface for test purposes; CP in NT mode.
TS0 to TS2	Inputs	Time slot 0 to 7. IOM interface time slot to be used = 4 · TS2 + 2 · TS1 + TS0; LT-T and LT-S in IOM MUX mode.

Interfaces

S-Interface

According to CCITT recommendation I.430, a modified AMI code with 100% pulse width is used on the S-interface. A logical 1 (one) corresponds to a neutral level (no current), whereas logical 0s are coded as alternating positive and negative pulses. An example of a modified AMI code is shown in Figure 4.

One S-frame consists of 48 bits, at a nominal bit rate of 192 kb/s. Thus each frame carries two octets of B1, two octets of B2, and four D-bits, according to the B1 + B2 + D structure defined for the ISDN basic access (total useful data rate: 144 kb/s). Frame begin is marked using a code violation (no mark inversion). The frame structures (from network to subscriber, and subscriber to network) are shown in Figure 5.

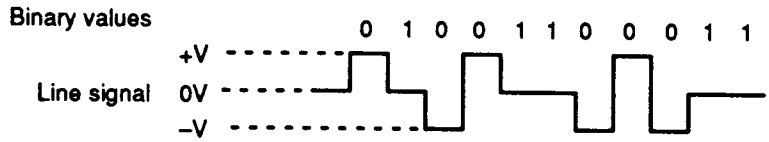


Figure 4. Modified AMI Code

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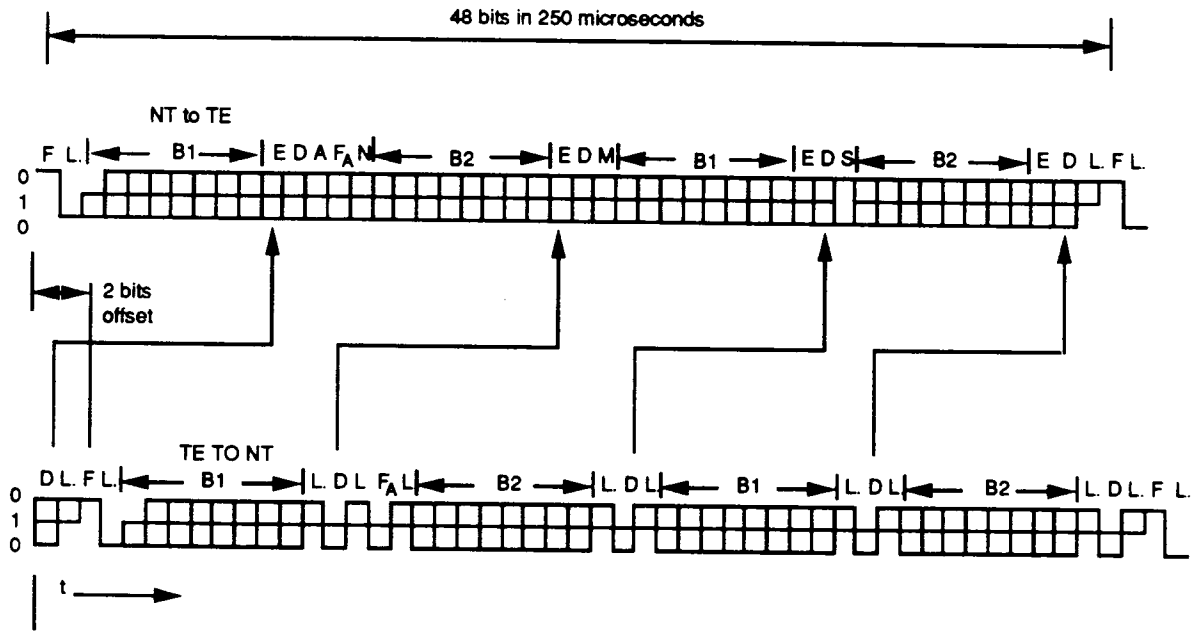


A = Bit used for activation
B1 = Bit within B channel 1
B2 = Bit within B channel 2
D = D-channel bit
E = D-echo-channel bit
F = Framing bit
FA = Auxiliary framing bit or Q-bit
L = DC balancing bit
M = Multiframing bit
N = Binary Value : N = $\overline{FA}$
S = Reserved for future standardization

Note: Dots demarcate those parts of the frame that are independently DC-balanced.

Figure 5. Frame Structure at Reference Points S and T (CCITT I.430)

Digital Interface

The SBC has a digital interface, the IOM interface, for communicating with other ISDN devices realizing OSI Layer 1 functions, such as the Am2090 ISDN Echo Cancellation (IEC), or Layer 2 functions, such as the Am2055 EPIC, the Am2075 IDEC, and the Am2110 ITAC.

The IOM interface is a four-wire serial interface with a bit clock, and one data line per direction as shown in Figure 6. The data in both directions is synchronous and in phase.

For each application, the ISDN user data rate of 144 kb/s (B1 + B2 + D) is transmitted transparently via the interface. In addition, it is necessary to interchange control information for activation and deactivation of OSI Layer 1 and for switching of test loops. This information is transferred using time division multiplexing with a 125 µs total frame length. The basic frame consists of four octets as shown in Figure 7:

1st octet B1: B channel (64 kb/s), most significant bit first.

2nd octet B2: B channel (64 kb/s), most significant bit first.

3rd octet Monitor: Monitor channel (64 kb/s), most significant bit first.

4th octet B*: 2 bit D channel (16 kb/s)
4 bit C/I channel.
T channel, not used with SBC.
E bit, not used with SBC.

The OSI Layer 1 functions are controlled by the state oriented four-bit Command/Indication codes (C/I). The codes originating from OSI Layer 2 devices are called "command" primitives, and those sent by the SBC are termed responses, or "indication" primitives. For a list of the C/I codes and their uses, refer to List of Control Codes.

The IOM interface has four modes. These modes differ only with respect to the physical data rate (256 or 8 · 256 kb/s) and to polarity of the clocks.

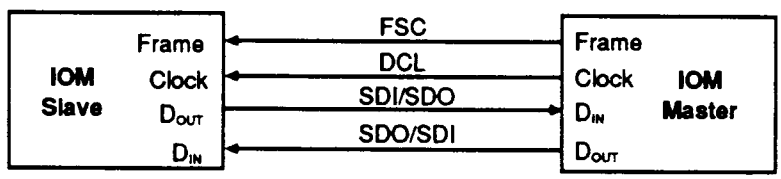
IOM-1 Mode

This timing mode is applicable in all operating modes of the SBC:

Nominal bit rate of data (SDI and SDO):	256 kb/s
Nominal frequency of DCL:	512 kHz
Nominal frequency of FSC:	8 kHz

Transitions of the data occur after even-numbered rising edges of DCL. Even-numbered rising edges of the clock are defined as the second rising edge of FSC and every second rising edge thereafter.

The frame is earmarked by the rising edge of FSC as shown in Figure 8.



In LT-S	SBC	IDEC
In NT	SBC	IEC
In LT-T	SBC	IDEC
In TE	ITAC	SBC

Figure 6. IOM Interface Signals 11135-009A

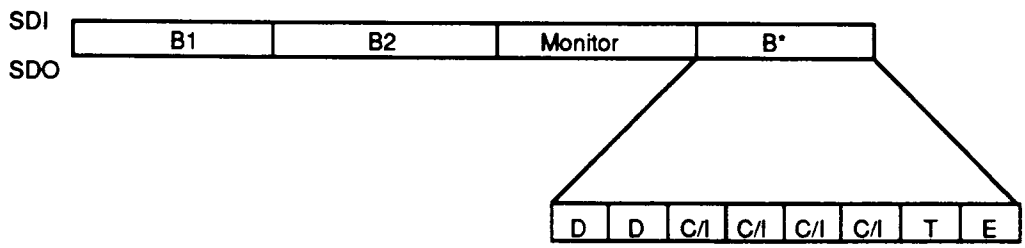


Figure 7. IOM Interface Frame Structure 11135-010A

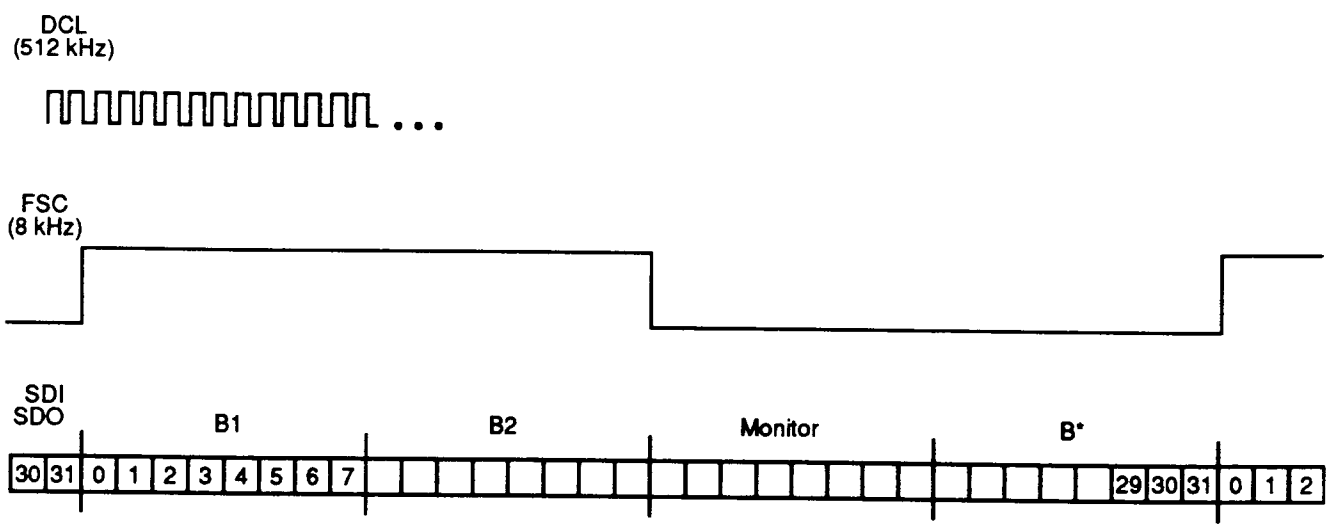


Figure 8. Timing for Data and Clocks of IOM in IOM-1 Mode 11135C-030

Inverted Mode

This timing mode is applicable in TE mode.

The characteristics are the same as IOM-1 mode, except that FSC is not a signal with 50%-duty cycle but an active Low pulse, one DCL clock period long, which occurs in the middle of bit 27 (fourth bit of B*).

Inverted MUX mode

This timing mode is applicable in LT-T and LT-S operating modes:

Nominal bit rate of data bursts (SDI and SDO):	2048 kb/s
Nominal frequency of DCL:	4096 kHz
Nominal frequency of FSC:	8 kHz

The frame clock FSC is an active Low strobe clock. The strobe earmarks the second half of bit 251 in the frame. The Low state of the strobe is detected with the rising edge of DCL. Refer to Figure 9.

The data at the input SDI is valid on the even-numbered rising edges of DCL. Transitions of the data on SDO occur after even-numbered falling edges of DCL. The rising edge earmarked by the frame strobe is an even-numbered rising edge of DCL. The following falling edge is an even-numbered falling edge.

The bursts are allocated to consecutive time slots in a frame by the static inputs X0(TSO), X1(TS1), X2(TS2). Table 4 indicates the allocations. Figure 10 gives the positions of the respective frames.

IOM-2 Mode

This timing mode is applicable in LT-T and LT-S modes:

Nominal bit rate of data bursts (SDI and SDO):	2048 kb/s
Nominal frequency of DCL:	4096 kHz
Nominal frequency of FSC:	8 kHz

As opposed to inverted mode, data changes with rising edges and frame synchronization is defined as in IOM-1 mode (IOM-2 Interface Reference Guide).

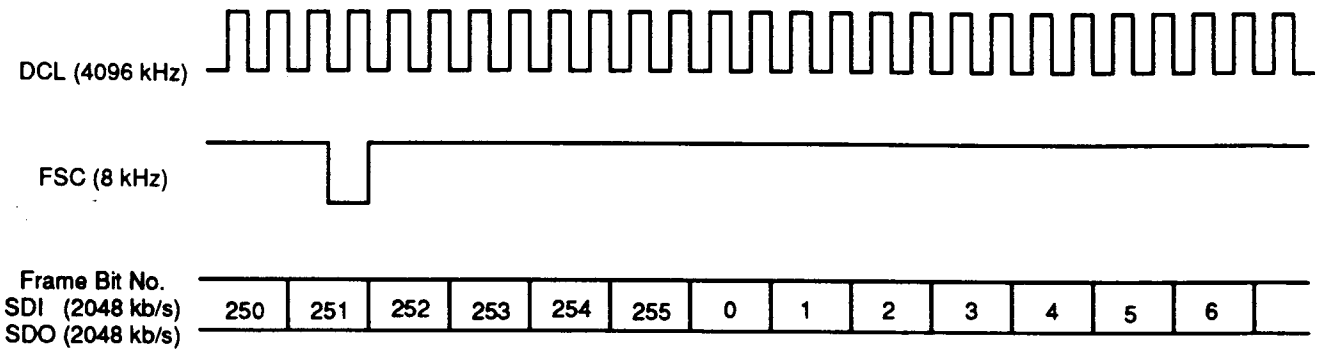


Figure 9. Timing of Data and Clocks of IOM in the Inverted MUX Mode

11135C-031

Table 4. Allocation of Time Slots

Time Slot No.	TS2	TS1	TS0	Bit No.
0	0	0	0	0 . . . 31
1	0	0	1	32 . . . 63
2	0	1	0	64 . . . 95
3	0	1	1	96 . . . 127
4	1	0	0	128 . . . 159
5	1	0	1	160 . . . 191
6	1	1	0	192 . . . 223
7	1	1	1	224 . . . 255

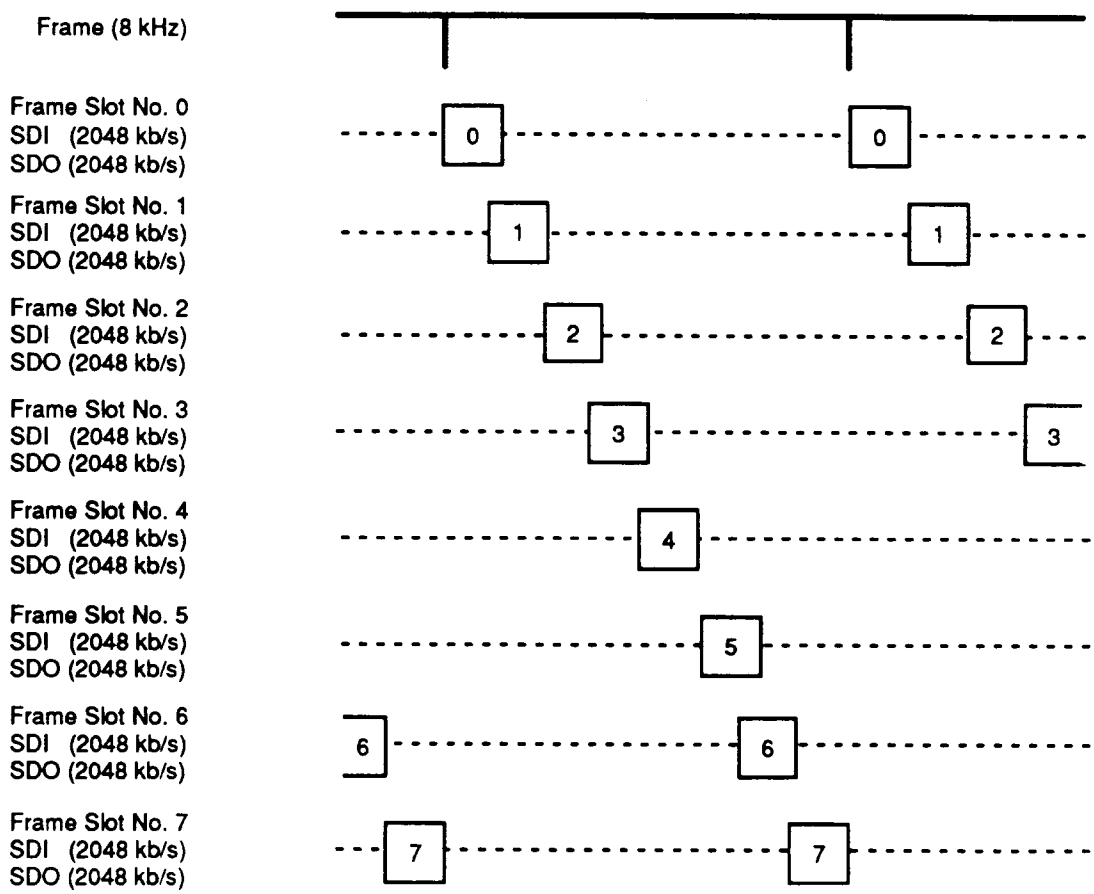


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Figure 10. Position of IOM Frames as a Function of Time Slot Allocation in IOM-2 and Inverted Mode

The IOM-2 Mode may be used to link up to eight SBC's over a single 2048-kb/s interface to an exchange or PABX (Figure 11).

In the LT-T and LT-S IOM-2 or inverted MUX modes, the SBC recognizes automatically whether IOM-2 mode or inverted MUX mode timing signals are applied.

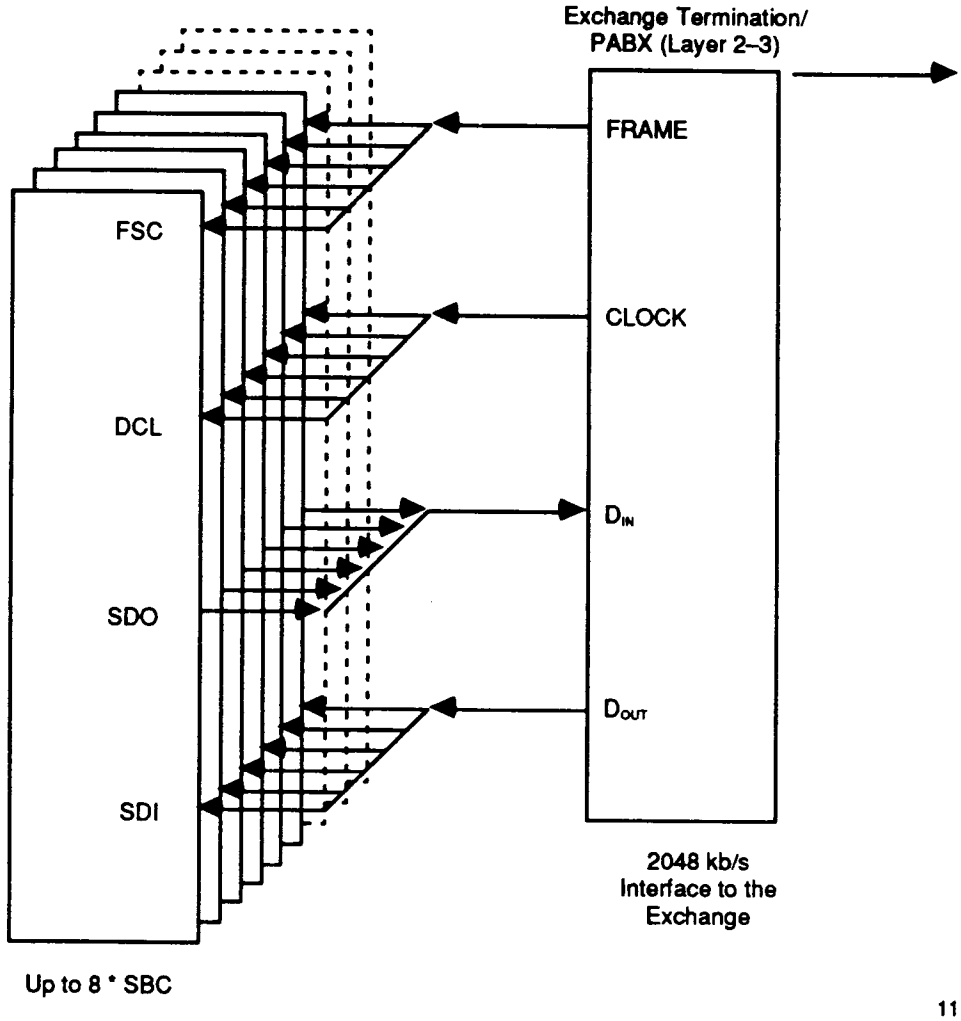


Figure 11. IOM Interface 2048 kb/s Inverted MUX Mode

Individual Functions

The SBC transmits data between the IOM interface and the line interface. Data clock pulses are received from the IOM interface and applied to clock the line S-interface (NT, LT-S) or vice versa (TE, LT-T). In the active state the data of the B-channels is switched through transparently. The data of the D-channel is handled in the same manner in the NT, LT-S and LT-T application. In the TE mode, switching of the D-channel is subject to S-bus D-channel access procedure and collision detection. (See TE Application section.)

Clock and frame synchronization varies from application to application. The timing relations in the different modes are summarized in Figure 12.

The frame positions have been selected to minimize the round-trip delays of the B channels, which are:

–125 µs for TE, NT and LT-S in IOM-1 mode,

–Max 250 µs for LT-T in IOM-1 mode and LT-S in inverted MUX mode,

–and Max 375 µs for LT-T in inverted MUX mode.

NT and LT-S Applications

The 192-kHz transmit bit clock is synchronized to the IOM clock DCL as shown in the application example in Figure 13. In the receive direction two cases have to be distinguished depending whether a bus or a point-to-point operation is programmed (pin X3:BUS).

Bus Operation

The 192-kHz receive bit clock is identical to the transmit bit clock, shifted by 4.6 µs with respect to the transmit edge. According to CCITT 1.430, the receive frame shall be shifted by two bits with respect to the transmit frame.

Point-to-Point Operation

The 192-kHz receive bit clock is recovered from the receive data stream on the S-interface. (The sampling instant for the receive bits is shifted by 3.9 µs with respect to the leading edge of the derived receive clock). According to CCITT 1.430, the receive frame can be shifted by 2–8 bits with respect to the transmit frame at the NT (LT-S). (Other shifts are allowed by SBC, including 0.)

This operation mode should also be used in extended passive bus applications.

E-Channel Handling

For D channel access collision resolution, the received D bit is in all cases transmitted as the E-bit in the S-frames.

In addition, in the NT mode the echo bit may be made externally available, thus allowing for the implementation of a star configuration.

TE Application

The transmit and receive bit clocks are derived, with the help of the DPLL, from the S-interface receive data stream.

The transmit frame is shifted by two bits with respect to the received frame. The output clocks CP, DCL and FSC are synchronous to the S-interface timing.

D-Channel Access Control

The D-channel access control ensures that only one terminal shall have access to the D-channel at any time. This is achieved through collision detection by each terminal (CCITT I.430). The SBC monitors the received D-echo channel, and, when transmission in the D-channel is started, compares the echo bits to the transmitted D-bits.

A mismatch between D bit and D-echo bit means that another terminal is also transmitting and a collision has taken place. This can only happen if D = 1 and D-echo = 0, since on the S-bus a logical 0 overrides a logical 1 (thus the comparison of D-echo with D bit is performed only when D-echo = logical 0). The SBC immediately ceases transmission, returns to the D-channel monitoring state and sends 1's in the D-channel. D-channel access is possible only after x consecutive 1's have been received in the echo channel. Depending on the priority class, x can either be eight or ten. If a terminal has successfully transmitted a complete HDLC frame, x is automatically increased by 1. Then x is reset to its initial value of eight (ten) when nine (eleven) consecutive 1's are received in the echo channel.

To enable initiating and interrupting HDLC frame transmission in the D channel, the SBC has to inform the Layer 2 controller of the D-channel status—ready or busy. For this, bit 20 of the IOM frame, in other words the fourth bit from the right in the Monitor channel, is used; see Figure 14.

By sending the BUSY bit at 0 to the Layer 2 controller in anticipation of the S-bus D-channel ready state, the first valid D bits will emerge from the SBC at exactly the moment an access is allowed.

D-channel switching (blocked: D = 1, or transparent: D = HDLC) is described by the state diagram in Figure 15a with BUSY bit states ready and busy as input variables. Figure 15b shows the status diagram for ready and busy, with the following variables:

P: priority (8 or 10), set by a C/I channel command.

C: number of consecutive ones appearing in the echo channel.

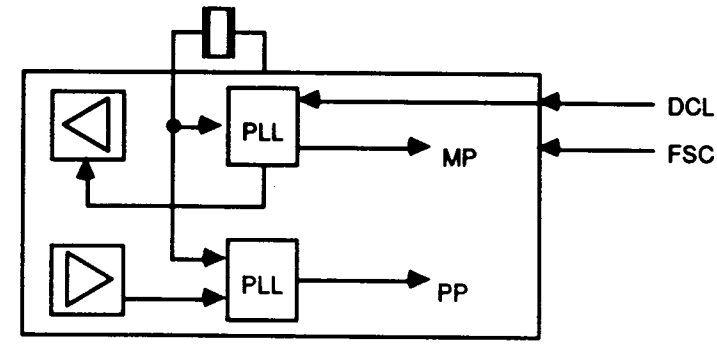
V: V = 1 if transmitted D bit = received D-echo bit, V = 0 otherwise.

Dp: priority decrement for priority class P, (P = 8 or 10).

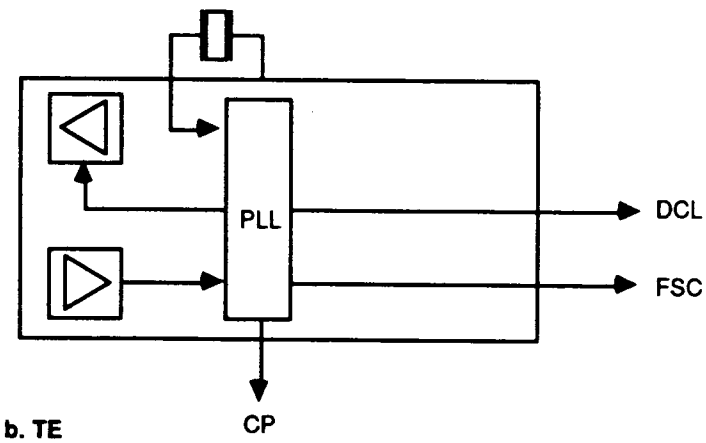
Thus state 1 is the state where a D channel access may be attempted. The transition 1-2 occurs at the first zero of an opening flag (C = 0: zero observed in D-echo channel, and V = 1: a zero has actually been transmitted). Transition i-0 (i = 1, 2, 3) occurs at the first monitored zero in the echo channel when the station is idle (1-0), or if a collision either within an opening flag (2-0) or between the opening and closing flags (3-0) of an HDLC frame is observed. The successful transmission of a closing flag (3-0 conditioned by C = 6) must be followed by a decrement in the priority class (Dp = 1). Dp is reset when 9 or 11 consecutive 1's are observed (state 1): cf., CCITT I.430.

Q Channel

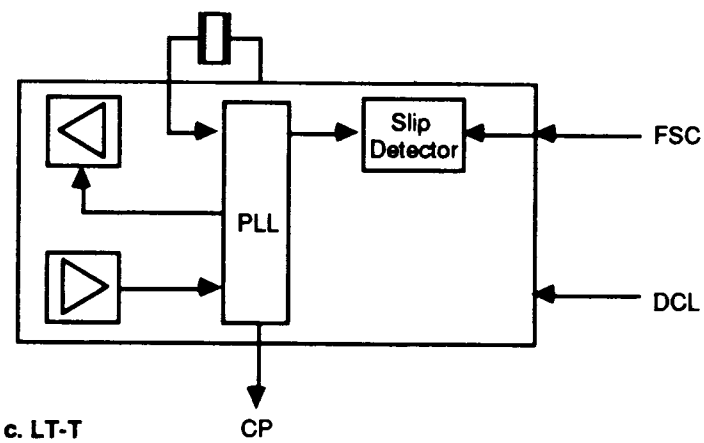
The SBC provides Q channel support by transmitting a binary 1 in each frame in which a 1 is received in the FA-bit position of the NT-to-TE frame. Thus interference of FA bits from one TE with the Q bits in passive bus configurations is avoided.



a. NT, LT-S: MP-receive clock for passive bus configuration
PP-receive clock for point-to-point configuration



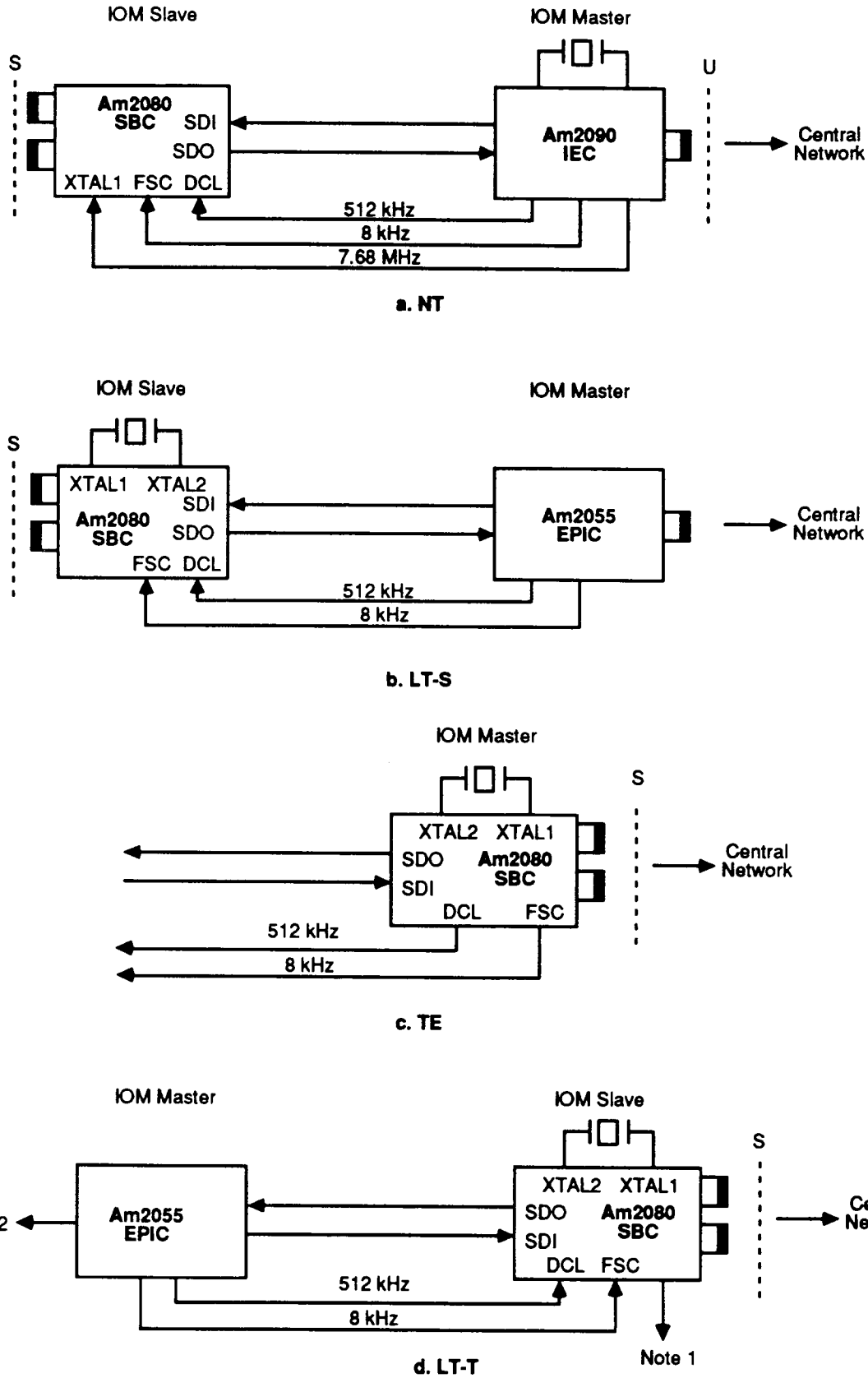
b. TE



c. LT-T

11135C-034

Figure 12. Clocking of the SBC



IEC = ISDN Echo Cancellation Circuit Am2090
ICC = ISDN Communication Controller Am2070

Note 1: Reference clock (512 kHz, duty cycle 1:2) may be used to drive; e.g., NT2 clock generator.

Figure 13. Clocking of SBC in Different Operating Modes 11135-011B

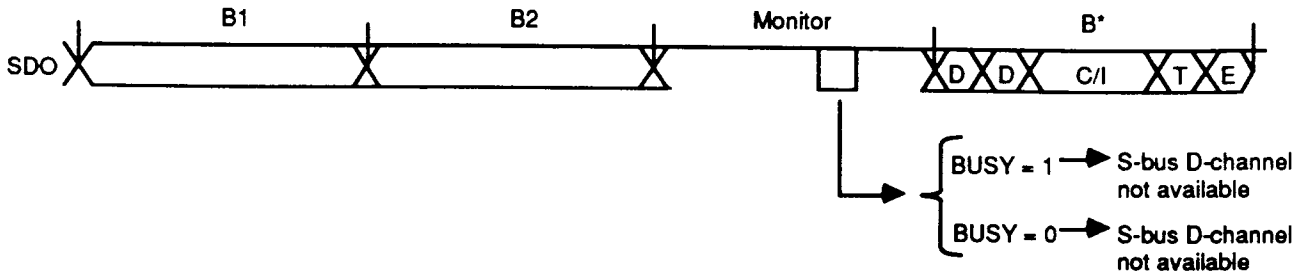


Figure 14. Position of BUSY Bit in IOM Frame

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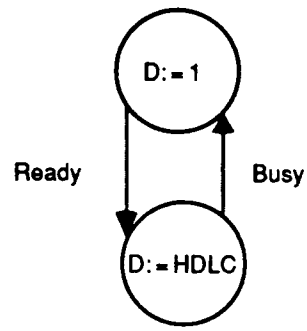
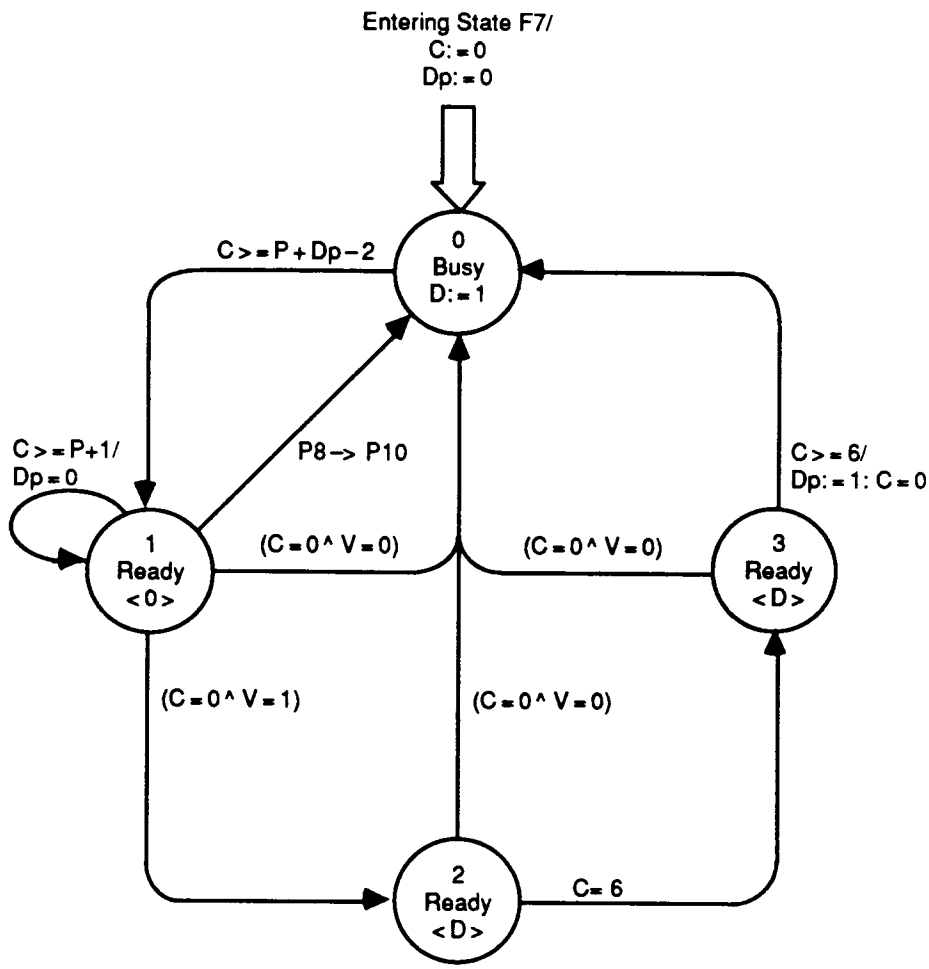


a.



b.

11135C-036

Figure 15. D-Channel Access Control of the SBC

LT-T Application

As in TE applications, the receive 192-kHz clock is adaptively derived from the S interface data. The transmit frame is shifted by two bits with respect to the receive frame.

The SBC provides a 512-kHz clock, CP, derived from the 192-kHz receive line clock with the DPLL. If necessary, this reference clock may be used to synchronize the central system (NT2) clock generator. The system timing is input over IOM interface bit and frame clocks, DCL and FSC. The relative position of the S and IOM frame is arbitrary. Moreover, the SBC prevents a slip from occurring if the wander between the DCL and CP clocks does not exceed a limit. (The SBC enables the intermediate storage of: 3xB1, 3xB2 and four-D bits, for phase difference and wander absorption). In case a wander greater than 24 µs is exceeded (cf., CCITT Q.503), a warning is sent twice by the SBC in the C/I channel (slip).

If the analog test loop (TL3, cf., Test Functions) is closed, the 192-kHz line clock is internally derived from DCL; therefore, no slips can occur in this case.

Since only point-to-point configurations can be realized with the LT-T application, bus availability indication is not required. However, the D-echo bit is still monitored and interference-free transmission is indicated by the BUSY bit.

Test Functions

Two kinds of test loops may be closed in the SBC, which depend on the selected mode of operation. In both test loops, all three channels (B1, B2 and D) are looped back. In a "transparent" loop, the data is also sent forward (in addition to being looped back), whereas in a "non-transparent" loop, the forward data path is blocked. These test loops are shown in Figure 16.

Test loop 3 is activated with the C/I channel command Active Request Loop (ARL). An S interface is not required since INFO3 is looped back to the receiver. When the receiver has synchronized itself to this signal, the message Test Indication (or Awake Test Indication) is delivered in the C/I channel. No signal is transmitted over the S interface.

Test loop 2 is likewise activated over the IOM interface with Active Request Loop (ARL). No S line is required. INFO4 is looped back to the receiver and also sent to the S-interface. When the receiver is synchronized, the message AIU is sent in the C/I channel. In the test loop mode the S-interface awake detector is disabled, and echo bits are set to logical 0.

Two kinds of test signals may be sent by the SBC: continuous zeros according to modified AMI coding (96-kHz repetition rate) and single AMI zeros (2-kHz repetition rate). The zeros are one S-interface bit period wide.

Single zeros can be sent in all applications. The corresponding C/I command in TE, LT-S and LT-T applications is SSZ (send single zeros). In the NT mode, this test mode is entered by pulling pin $\overline{SSZ}$ (pin X2, NT mode only) to logical 0.

Continuous zeros may be transmitted in all applications. This test mode is entered in LT-S, LT-T and TE applications with the C/I command SCZ. In the NT mode, this test mode is entered by pulling pin $\overline{SCZ}$ (pin CP, NT mode only) to logical 0.

On activation of SCZ or SCC (via pins X2 or CP) the SBC pulls SDO to zero in order to get clocks from the IOM master device.

Special Applications

The mode specific pins X3–0 allow for special applications to be implemented, some of which are mentioned in the following.

Star Configuration

In NT mode, the SBC transmits the D bit state over pin X0 (DE). A star configuration may be implemented by connecting pins X0 of several SBC's together (open drain with integrated pull-up). With X1 (DEX, D-E–External mirroring) tied to logical 1, the SBC transmits the resulting DE (wired AND for all SBC's) as the S-interface echo-bit. See Figure 17.

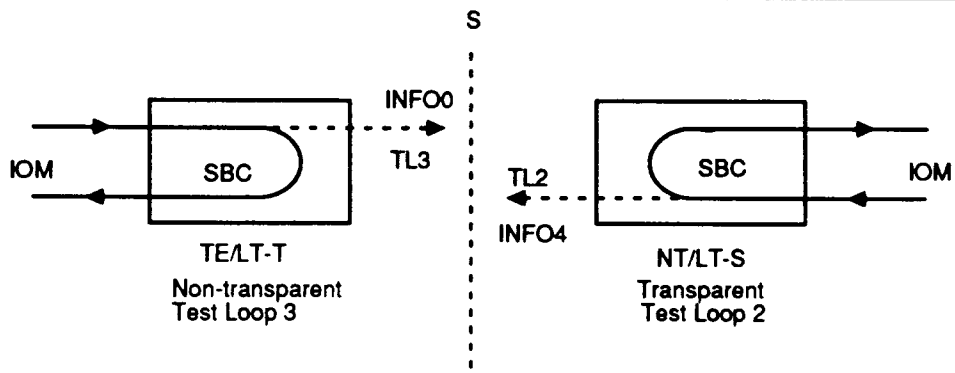


Figure 16. Test Loops of Am2080 SBC

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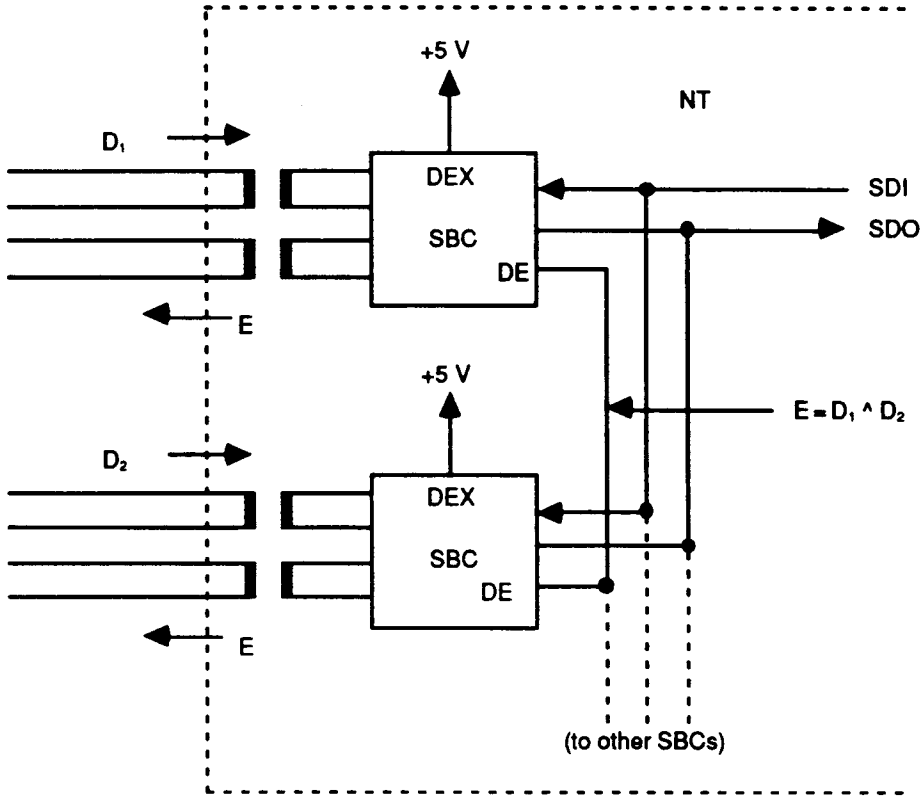

Figure 17. Star Configuration in NT

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Use of ECHO

Local communication of terminals connected to an S-bus may be implemented by using the auxiliary ECHO output (pin X2, in TE mode only). The timing of ECHO is identical to that of output SDO; however, the signal is 1 everywhere except in bit positions 24 and 25 of the IOM frame, where it is equal to the echo bits received from the S-interface. Thus a Layer 2 device connected to ECHO is able to receive or hear all other terminals. As a special application (shown in Figure 18), an S-bus local area network may be built using several TE SBC's and one NT (or an NT star configuration). Communication in the D and E channel is half duplex.

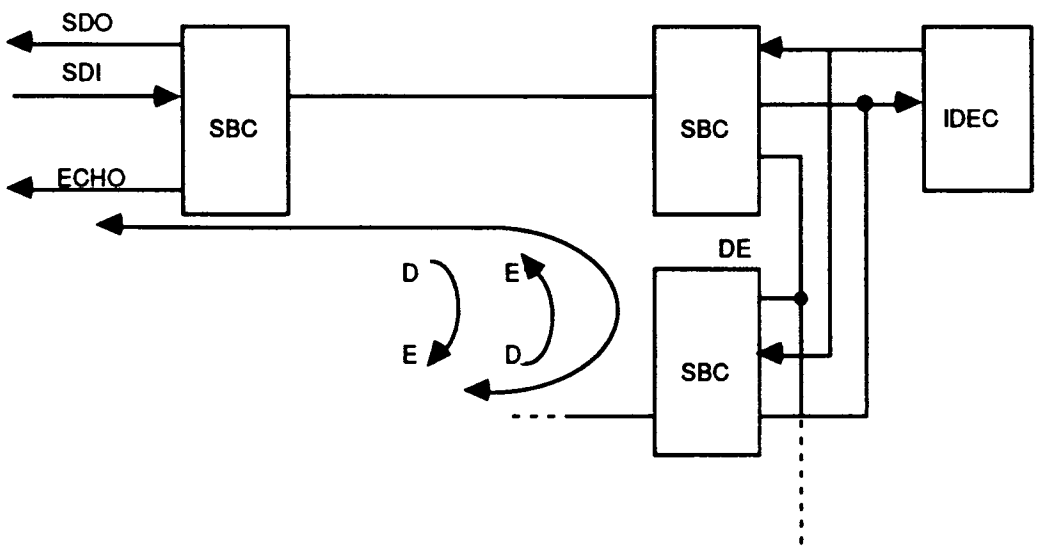

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Figure 18. Star Configuration in NT

OPERATIONAL DESCRIPTION

The internal finite state machine of the SBC controls the activation/deactivation procedures, switching of test loops and transmission of special pulse patterns. Such actions can be initiated by signals on the S-transmission line (INFO's) or by control (C/I) codes sent over the IOM interface.

Clocking, Reset and Initialization

In LT-T and LT-S modes the IOM interface should be kept active, i.e., the clocks DCL and FSC are always present. In this case commands in the C/I channel may also be handed over to the SBC in the power-down state (state F3 for LT-T/state G1 for LT-S; see Figures 23 and 24).

In TE and NT modes the IOM interface can be switched off in the inactive state, reducing power consumption to a minimum (below 5 mW). In this deactivated state the clock lines are Low and data lines are High.

For the TE case the procedure is shown in Figure 19. After detecting the code DIU (Deactivate Indication Upstream, i.e., from TE and NT/LT-S) from the downstream unit, the SBC responds by transmitting DID (Deactivate Indication Downstream) during subsequent frames and stops the timing signals synchronously with the end of the last C/I channel bit of the fourth frame.

The clock pulses are enabled again when the SBC recognizes a low level on SDI (command Timing TIM = 0000) or when a non-zero level on the S line interface is detected. The clocks are turned on after approximately 0.5 to 4 ms (dependent on the capacitances on XTAL1/XTAL2) as shown in Figure 20.

After the clocks have been enabled (this is indicated by the PU code in the C/I channel), the downstream unit may then insert a valid code in the C/I channel. The continuous supply of timing signals by the SBC is ensured as long as there is no DIU command in the C/I channel. If timing signals are no longer required and activation is not yet requested, the downstream unit may indicate this by sending DIU.

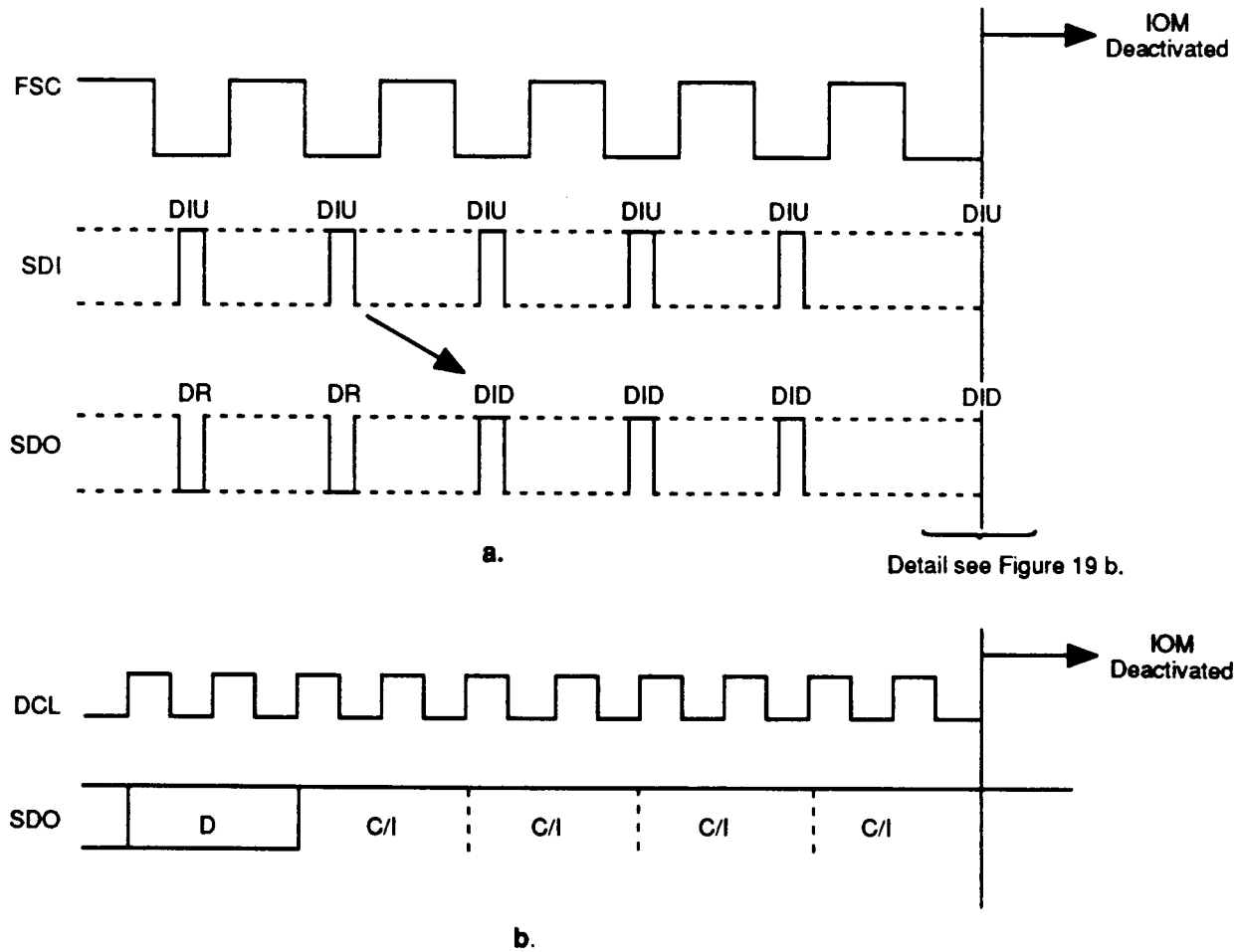

Figure 19. Deactivation of the IOM Interface

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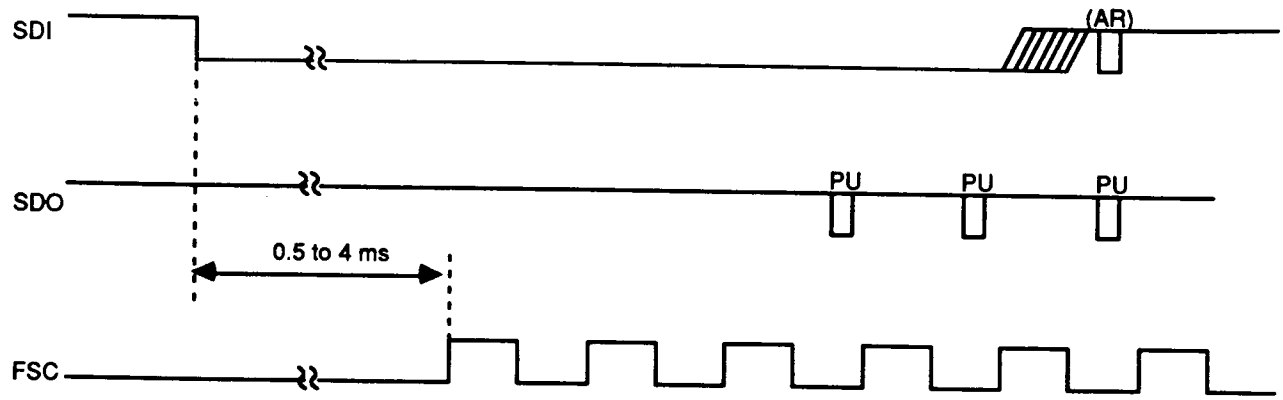


Figure 20. Activation of the IOM Interface 11135C-040

As an alternative to clock activation via SDI, the asynchronous wake-up pin $\overline{ENCK}$ (X3 in TE mode) can be grounded. In this case, the timing given in Figure 21 applies. When $\overline{ENCK}$ is tied to ground the IOM clock pulses are delivered by SBC at all times.

In NT mode the IOM interface is activated by the upstream unit turning on the clocking signals. Simultaneously, the upstream unit must send the desired command in the C/I channel. In the case where activation is requested from a terminal, the NT SBC first requests timing on the IOM interface by pulling SDO to a static low level. The SBC enters the power-up state immediately after timing has been applied. The clock signals may be switched off after the code Deactivation Indication Downstream has been sent twice by the upstream unit.

At power up, a reset pulse ($\overline{RST}$) should be applied to bring the SBC to a well defined state. This state is G1 for NT or LT-S mode, and F3 for TE or LT-T mode. The oscillator and energy intensive analog components are disabled and the S-line awake detector is active after the pulse. All outputs are in high impedance state during the hardware reset pulse. In TE mode, when $\overline{ENCK}$ is grounded, however, the SBC will still supply IOM timing during a reset pulse, and the message Error indication (EI) is present in the C/I channel. Similarly, in NT mode, activation of pin CP brings the outputs to low impedance during a reset pulse and the message EI is sent in the C/I channel.

State Diagrams

The state diagrams are shown in Figures 23 to 25 following their respective mode definitions. The activation/deactivation implemented by the SBC in its different operating modes agrees with the requirements set forth in CCITT recommendations. State identifiers F1–F8 (TE/LT-T) and G1–G4 (NT/LT-S) are in keeping with CCITT I.430. In the NT mode the four states have been expanded to implement a full handshake between the ends of the subscriber loop.

In the state diagrams a notation is employed which explicitly specifies the inputs and outputs on the S interface and in the C/I channel; see Figure 22.

TE/LT-T Mode

F3 Power Down

This is the deactivated state of the physical protocol. The receive line awake unit is active except during a $\overline{RST}$ pulse. Clocks are disabled if $\overline{ENCK}$ = 1 (TE mode). The power consumption in this state is approximately 22 mW when the clock is running, and 4 mW otherwise.

F3 Power Up

This state is identical to F3 power down except for the C/I output message. The state is invoked by a C/I command TIM = 0000 (or SDI static low). After the subsequent activation of the clocks, the PU message is sent. This occurs 0.5 ms to 4 ms after application of TIM, depending on crystal capacitances. If, however, the SBC is disconnected from the S interface (CON = 0), the C/I message DIS is outputted.

F3 Pending Deactivation

The SBC reaches this state after receiving INFO0 (from states F5 to F8) for 16 ms (64 frames). This time constant is a flywheel to prevent accidental deactivation. From this state an activation is only possible from the line (transition F3 pending deactivation to F5 unsynchronized). The power down state may be reached only after receiving DIU.

F4 Pending Activation

Activation has been requested from the terminal; INFO1 is transmitted; INFO0 is still received; Power Up is transmitted in the C/I channel. This state is stable: timer T3 (I.430) is to be implemented in software.

F5 Unsynchronized

At the reception of any signal from the NT, the SBC ceases to transmit INFO1 and awaits identification of INFO2 or INFO4. This state is reached at most 50 sec after a signal different from INFO0 is present at the receiver of the SBC.

F6 Synchronized

When SBC receives an activation signal (INFO2), it responds with INFO3 and waits for normal frames (INFO4). This state is reached at most 6 ms after an INFO2 arrives at the SBC (when the oscillator was disabled in F3 power down).

F7 Activated

This is the normal active state with the Layer 1 protocol activated in both directions. From state F6 synchronized, state F7 is reached at most 0.5 ms after reception of INFO4. From state F3 power down with the oscillator disabled, state F7 is reached at most 6 ms after the SBC is directly activated by INFO4.

F8 Lost Framing

This is the condition where SBC has lost frame synchronization and is awaiting re-synchronization by INFO2 or INFO4 or deactivation by INFO0.

Unconditional States

Loop 3 Closed

On Activate Request Loop command, INFO3 is sent by the line transmitter internally to the line receiver (INFO0 is transmitted to the line). The receiver is not yet synchronized.

Loop 3 Activated

The receiver is synchronized on INFO3 which is looped back internally from the transmitter. Data may be sent. The indication TI or ATI is output depending whether or not a signal different from INFO0 is detected on the S-interface.

Test Mode Continuous Zeros

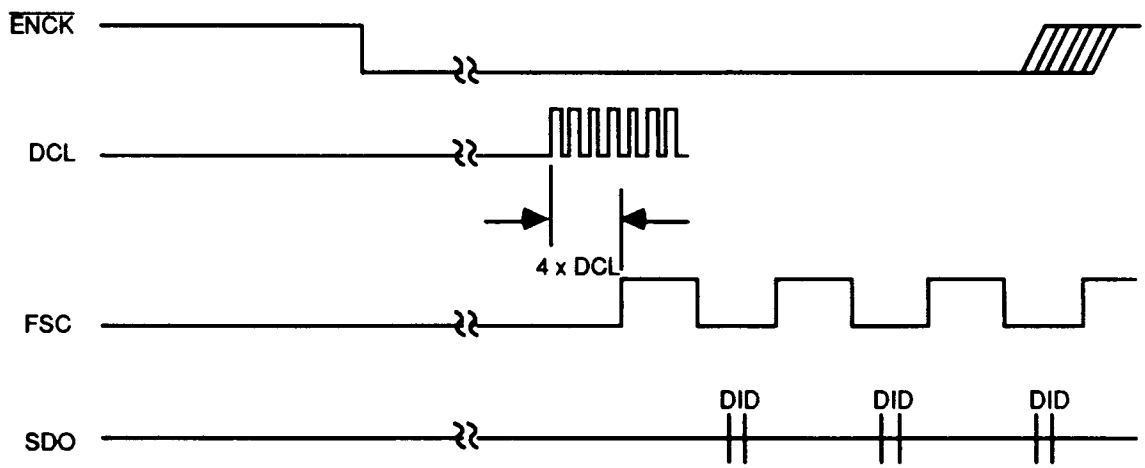
Continuous alternating zeros are sent at 96 kHz.

Test Mode Single Zeros

Single alternating zeros are sent (2-kHz repetition rate).

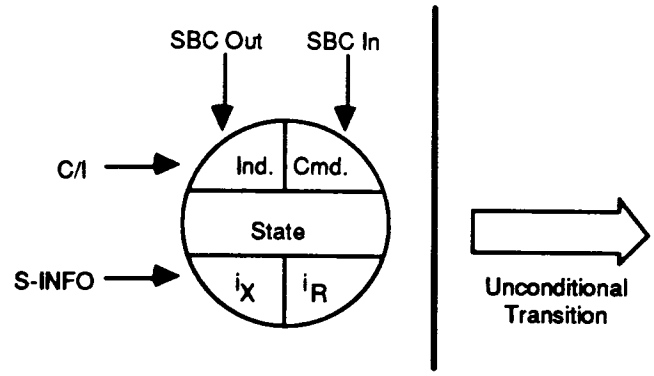
Reset State

A software reset (RS) forces the SBC to an idle state where the analog components are disabled (transmission of INFO0) and the S line awake detector is inactive. Thus activation from the NT is not possible. Clocks are still supplied (TE mode) and the outputs are in a low impedance state.



11135C-041

Figure 21. Activation of the IOM Interface via $\overline{\text{ENCK}}$ (pin X3) in TE Mode (NB: DCL out of scale)



11135C-042

Figure 22. The Inputs and Outputs on the S-Interface and in the C/I Channel

LT-S Mode

G1 Deactivated

The SBC is not transmitting. No signal is detected on the S-interface, and no activation command is received in C/I channel.

G2 Synchronized

As a result of an INFO1 detected on the S line or an ARD command, the SBC begins transmitting INFO2 and waits for reception of INFO3. INFO2 is sent after the awake detector has detected pulses during 4 ms. The timer to supervise reception of INFO3 is to be implemented in software.

G3 Activated

Normal state where INFO4 is transmitted to the S-interface. This state is reached less than 2 ms after an INFO3 first arrives at the SBC receiver. The SBC remains in this state as long as neither a deactivation or a test mode is requested, nor a reset pulse is issued.

When receiver synchronism is lost, INFO2 is sent automatically. After reception of INFO3, the transmitter keeps on sending INFO4.

G4 Pending Deactivation

This state is triggered by a deactivation request DR. It is an unstable state: indication DIU (state G4 unacknowledge) is issued by the SBC when:

–either INFO0 is received during 16 ms,

–or an internal timer of 32 ms expires.

G4 Unacknowledged

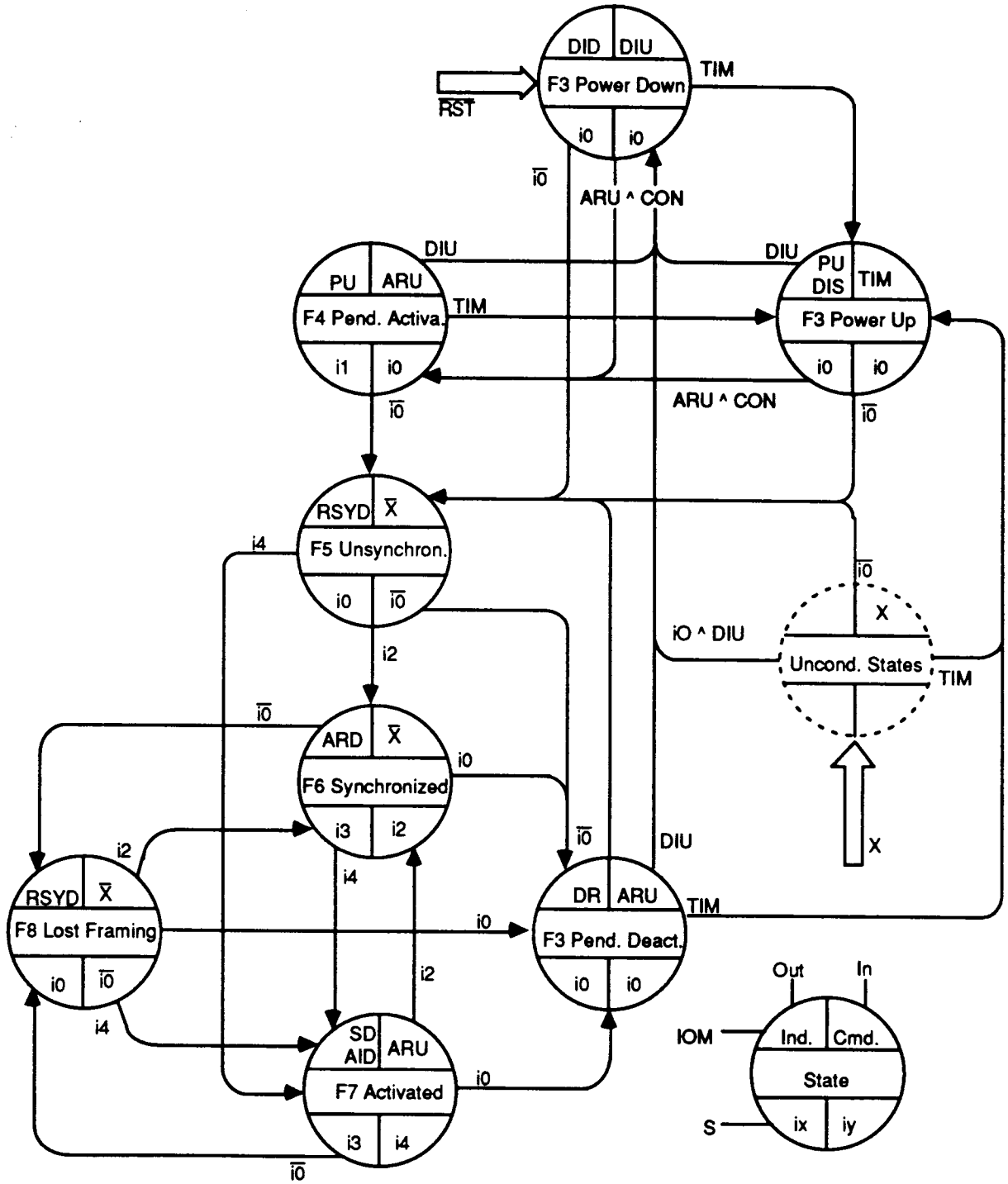
Final state after a deactivation request. The SBC remains in this state until a response to DIU (in other words DID) is issued, without which a new activation is impossible.

Test Mode Continuous Zeros

Continuous alternating zeros are sent at 96 kHz.

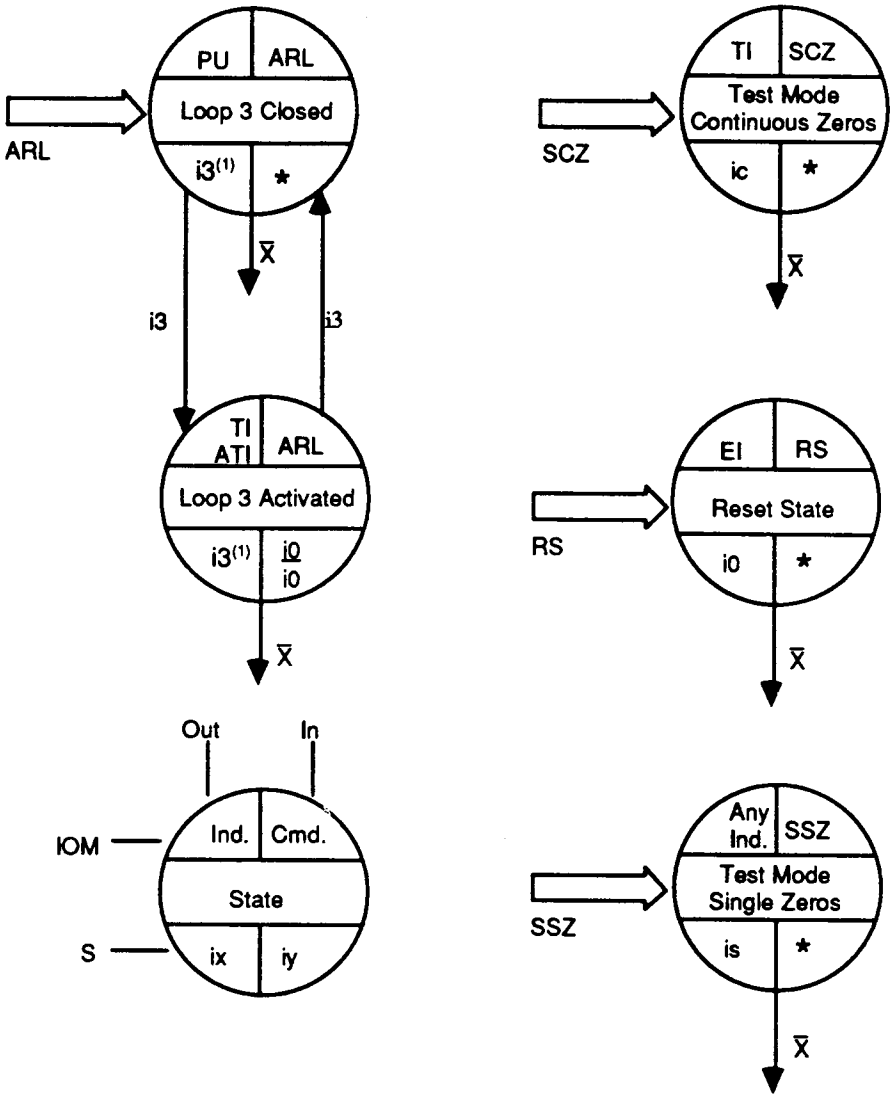
Test Mode Single Zeros

Single alternating zeros are sent (2-kHz repetition rate).



X: Unconditional command can be:
ARL, RS, SCZ, SSZ
ARU: AR8 or AR10
AID: AI8 or AI10

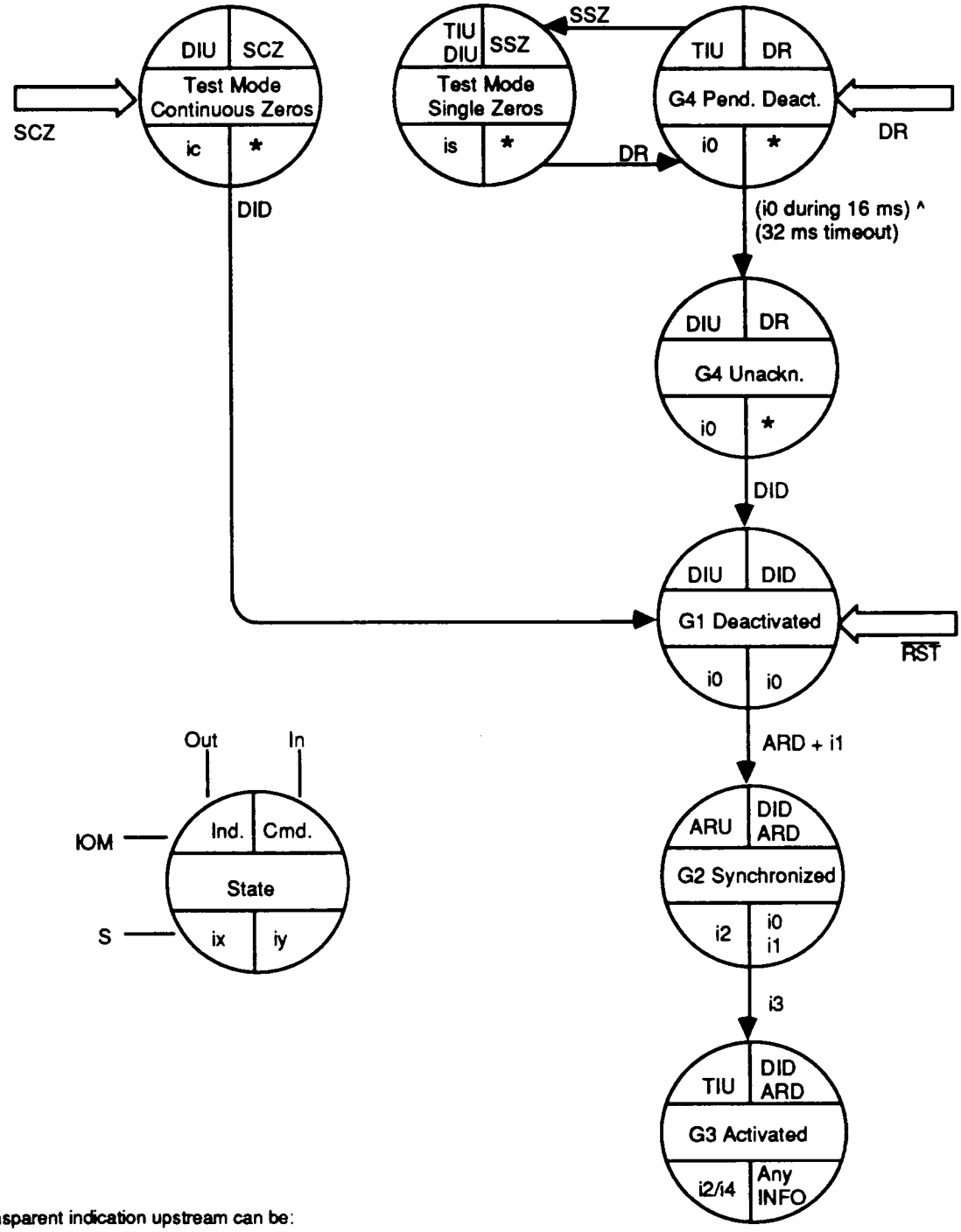
Figure 23a. State Diagram of TE/LT-T Mode



(1): Only internally
X: Unconditional commands can be:
ARL, RS, SCZ, SSZ
is: Single zeros, 2 kHz
ic: Continuous zeros, 96 kHz

11135C-044

Figure 23b. State Diagram of TE/LT-T Mode: Unconditional Transitions



TIU: Transparent indication upstream can be:
AIU, RSYU, LSL
is Single zeros, 2 kHz
ic: Continuous zeros, 96 kHz

11135C-045

Figure 24. State Diagram of LT-S Mode

NT Mode

G1 Deactivated

The SBC is not transmitting. No signal is detected on the S/T interface, and no activation command is received in C/I channel. EI is output as a response to $\overline{RST}$, DIU is output in the normal deactivated state, and TIM is output as a first step when an activation is requested from the S/T interface.

G1 I1 Detected

An INFO1 is detected on the S/T interface, translated to an Activation Request Upstream indication in the C/I channel. The SBC is waiting for an ARD command, which normally indicates that the transmission line upstream (usually a two-wire interface) is synchronized.

G2 Pending Activation

As a result of the ARD command, an INFO2 is sent on the S/T interface. INFO3 is not yet received.

G2 Synchronized

INFO3 was received, INFO2 continues to be transmitted while the SBC waits for a switch-through command AID from the device upstream.

G3 Activated

INFO4 is sent on the S/T interface as a result of the switch-through command AID; the B and D channels are transparent. In case of loss of synchronism of the NT receiver, INFO2 is sent.

Lost Framing U

On receiving a RSYD command which usually indicates that synchronization has been lost on the two-wire interface, the SBC transmits continuous alternating pulses.

G4 Pending Deactivation

This state is triggered by a deactivation request DR, and is an unstable state. Indication DIU (state G4 unacknowledged) is issued by the SBC when:

–either INFO0 is received during 16 ms,

–or an internal timer of 32 ms expires.

G4 Unacknowledged

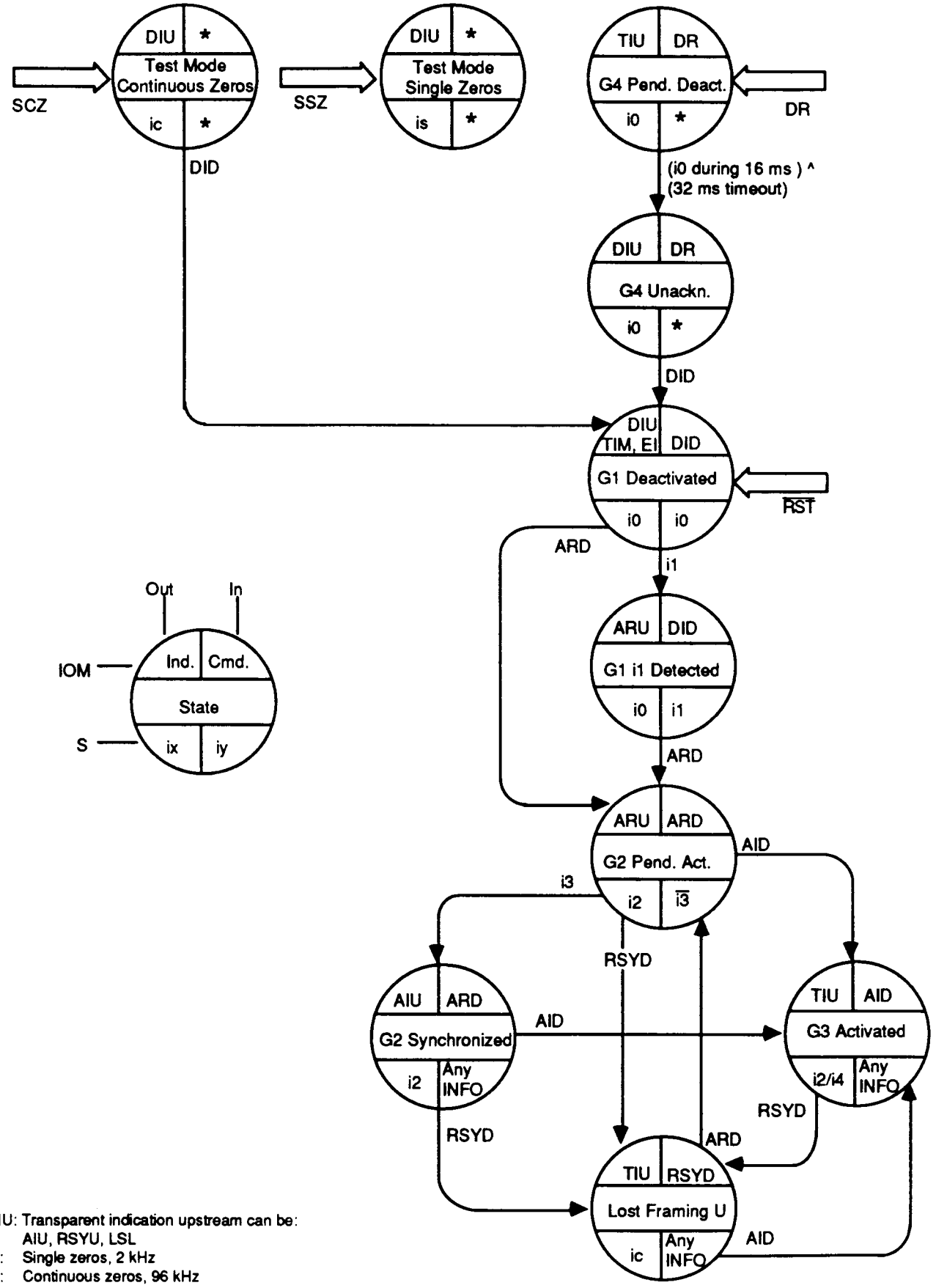
Final state after a deactivation request. The SBC remains in this state until an acknowledgment to DIU (DID) is issued, without which a new activation is impossible.

Test Mode Continuous Zeros

Continuous alternating zeros are sent.

Test Mode Single Zeros

Single alternating zeros are sent (2-kHz repetition rate).



TIU: Transparent indication upstream can be:
AIU, RSYU, LSL
is: Single zeros, 2 kHz
ic: Continuous zeros, 96 kHz

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Figure 25. State Diagram of NT Mode

Example of Activation/Deactivation

An example of an activation/deactivation of the S interface, with the respective commands, indications and time relationships, is shown in Figure 26.

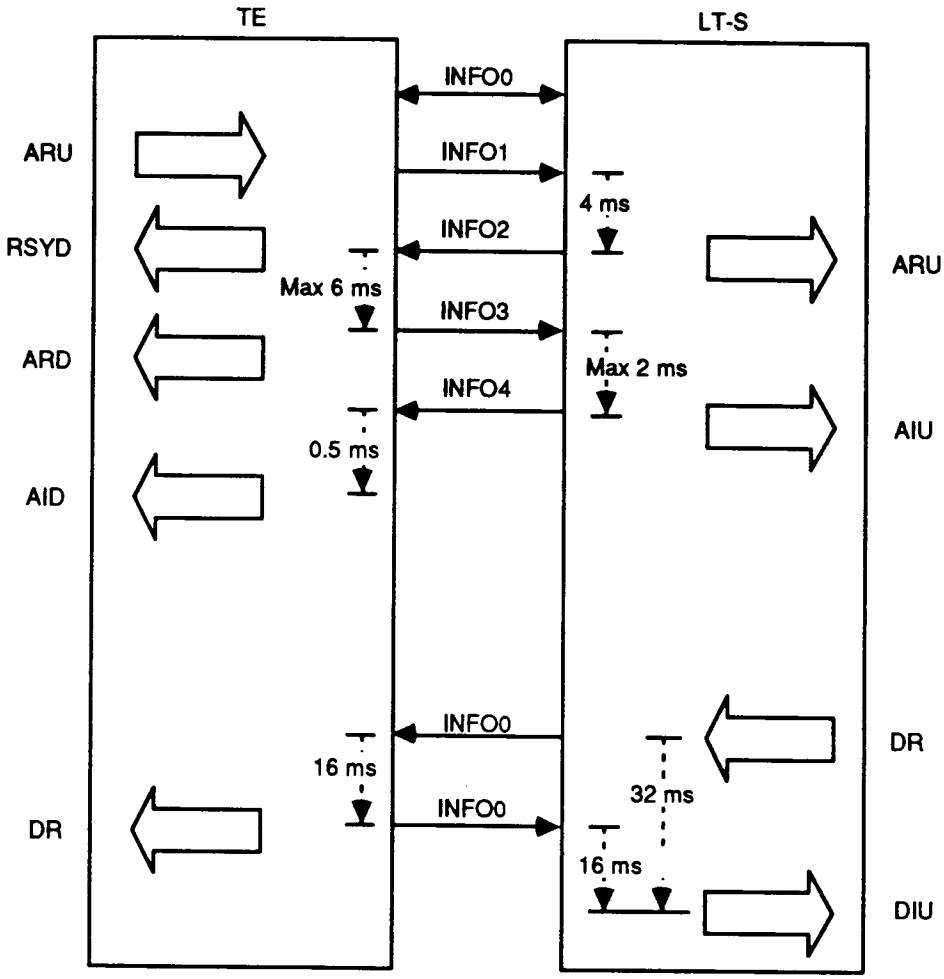

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Figure 26. Example of Activation/Deactivation

List of Control Codes

The exchange of control information in the C/I channel is state oriented. This means that a code in the C/I channel is repeated in every IOM frame until a change is necessary. To detect a change in a C/I code, the new code must be found in two consecutive IOM frames to be considered valid (double last look criterion). The Command/Indication codes are listed in Tables 4 through 6.

Table 4. Commands and Indications in LT-S Mode

	Abbr.	Code	Remark
Command (downstream)			
Deactivation request	DR	0000	(*)
Send continuous zeros	SCZ	0001	Transmission of AMI zeros at 96-kHz frequency (*)
Send single zeros	SSZ	0010	Transmission of AMI zeros at 2-kHz frequency (*)
Activate request	ARD	1000	
Activate request loop	ARL	1010	Activation request for loop 2
Deactivate indication	DID	1111	Deactivation acknowledgment, quiescent state
Indication (upstream)			
Lost signal level	LSL	0001	No receive signal
Lost framing	RSYU	0100	Receiver is not synchronous
Activate request	ARU	1000	INFO1 received
Activate indication	AIU	1100	Synchronous receiver
Deactivate indication	DIU	1111	Timer (32 ms) expired or INFO0 received during 16 ms after deactivation request

(*) Unconditional commands

Table 5. Commands and Indications in NT Mode

	Abbr.	Code	Remark
Command (downstream)			
Deactivation request	DR	0000	(*)
Resynchronization of U-interface	RSYD	0100	Transmission of AMI zeros at 96 kHz frequency after loss of synchronism of the U-interface
Activate request	ARD	1000	Transmission of INFO2
Activate request loop	ARL	1010	Transmission of INFO2, switching of test loop 2
Deactivate indication	DID	1111	Deactivation acknowledgment, quiescent state
Activate indication	AID	1100	Transmission of INFO4
Activate indication loop	AIL	1110	Transmission of INFO4, switching of test loop 2
Send single zeros	SSZ	0010	Transmission of AMI zeros at 2-kHz frequency (*)
Indication (upstream)			
Timing	TIM	0000	SBC requires clock pulses
Lost signal level	LSL	0001	No receive level
Lost framing	RSYU	0100	Receiver is not synchronous
Error indication	EI	0110	RST and SCZ both active
Activate request	ARU	1000	INFO1 received
Activate indication	AIU	1100	Synchronous receiver
Deactivate indication	DIU	1111	Timer (32 ms) expired or INFO0 received during 16 ms after deactivation request

(*) Unconditional commands

Table 6. Commands and Indications in TE/LT-T Mode

	Abbr.	Code	Remark
Command (upstream)			
Timing	TIM	0000	Clocking of all output clocks is required
Reset	RS	0001	(*)
Send continuous zeros	SCZ	0100	Transmission of AMI zeros at 96-kHz frequency (*)
Send single zeros	SSZ	0010	Transmission of AMI zeros at 2-kHz frequency (*)
Activate request, set priority 8	AR8	1000	Activation command, set D-channel priority to 8
Activate request, set priority 10	AR10	1001	Activation command, set D-channel priority to 10
Activate request loop	ARL	1010	Activation of test loop 3 (*)
Deactivate indication	DIU	1111	IOM clocks can be disabled
Indication (downstream)			
Power up	PU	0111	IOM clocking is provided
Deactivate request	DR	0000	Deactivation request by S interface
Slip detected	SD	0010	Wander is larger than 18 µs peak-to-peak
Disconnected	DIS	0011	Pin CON connected to GND
Error indication	EI	0110	($\overline{RST} = 0 \wedge \overline{ENCK} = 0$) in TE, or RS
Level detected	RSY	0100	Signal received, receiver not synchronous
Activate request	ARD	1000	INFO2 received
Test indication	TI	1010	Test loop activated or continuous zeros transmitted
Awake test indication	ATI	1011	Level detected during test loop
Activate indication with priority priority class 8	AI 8	1100	INFO4 received, D-channel priority is 8 or 9
Activate indication with priority class 10	AI 10	1101	INFO4 received, D-channel priority is 10 or 11
Deactivate indication	DID	1111	Clocks are disabled (in TE), quiescent state

(*) Unconditional commands

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65 to +125°C
DC Voltage Applied to Any
Pin Relative to V_{ss} ..... –0.4 to Vcc±0.4 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{cc}) ..... +5 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse (Figure 27).

Transmitter Input Current

The destruction limits for negative input signals are given in Figure 28. Ri≥2 ohms.

The destruction limits for positive input signals are given in Figure 29. Ri≥200 ohms.

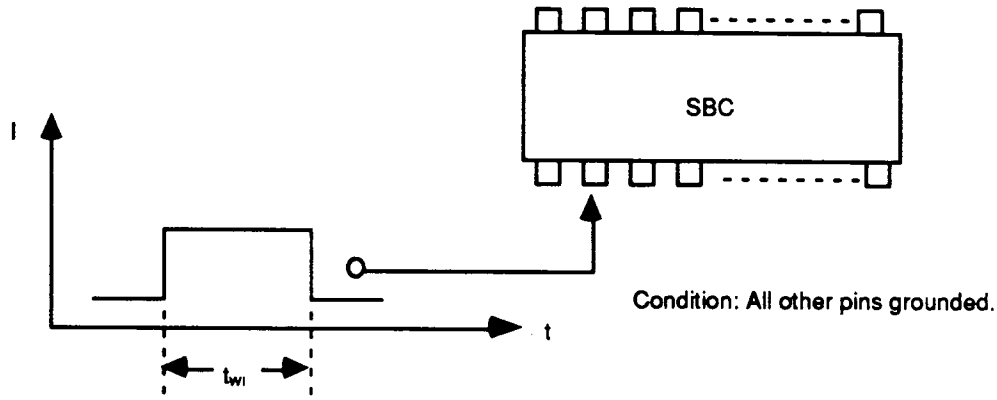

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Figure 27. Test Condition for Maximum Input Current

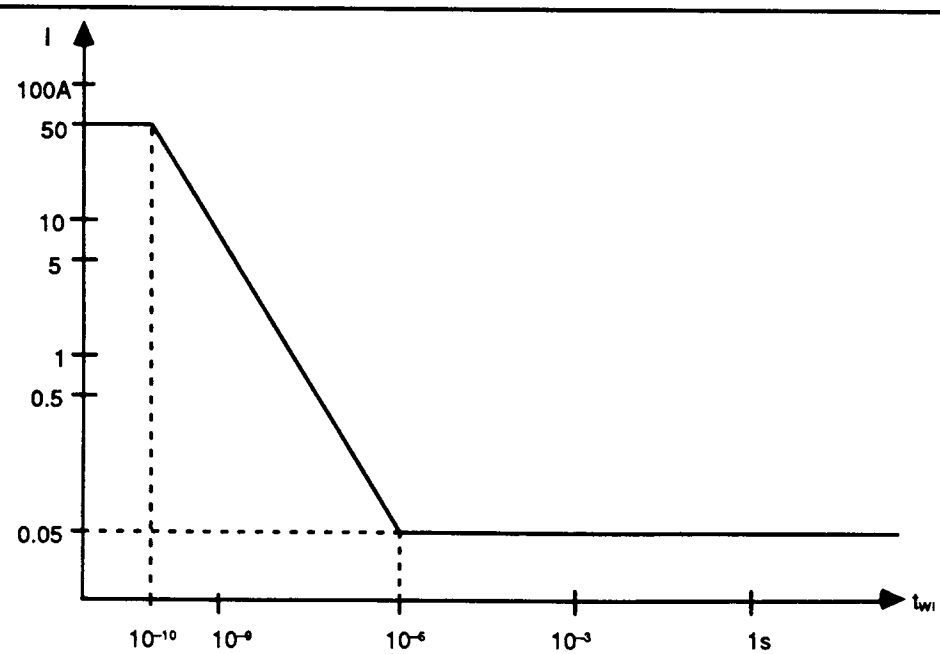

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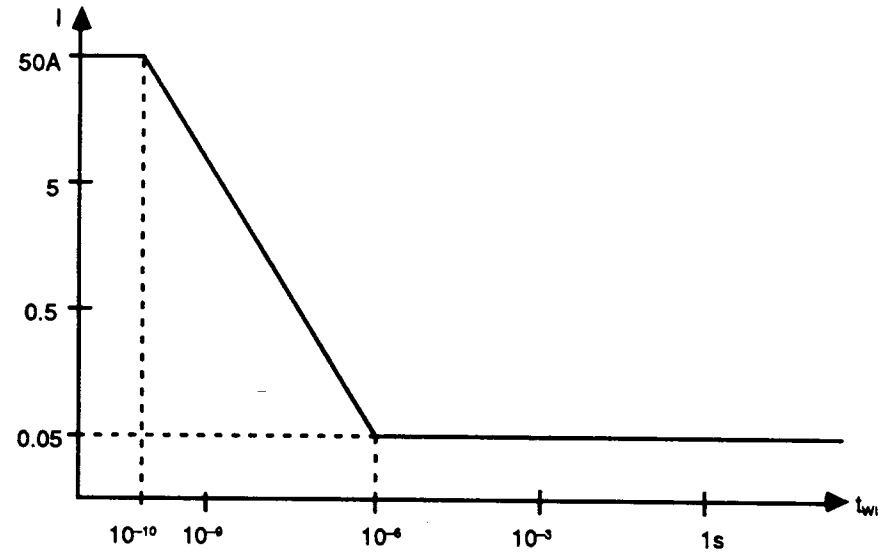
Figure 28. Destruction Limits for Negative Input Signals

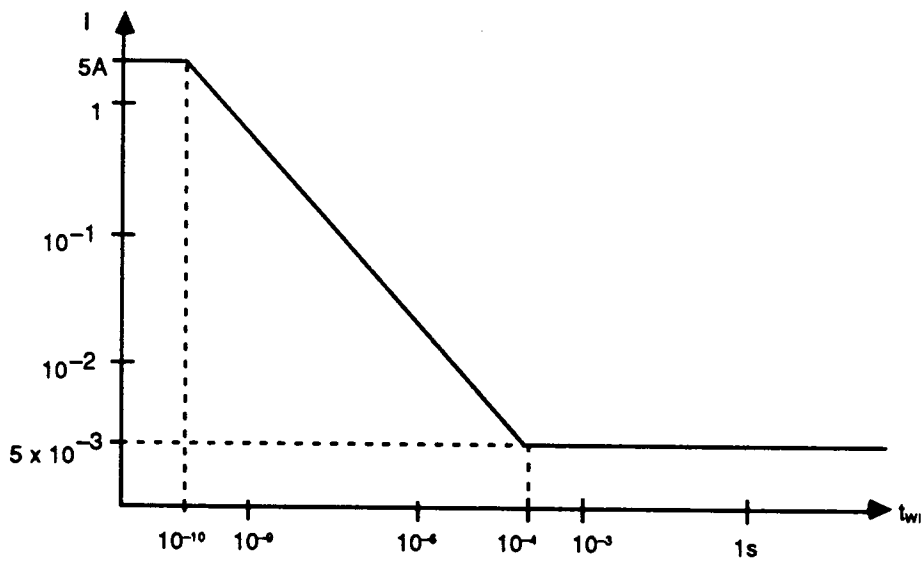


11135C-050

Figure 29. Destruction Limits for Positive Input Signals

Receiver Input Current

The destruction limits are given in Figure 30. Ri ≥ 300 ohms.



11135C-051

Figure 30. Destruction Limits

DC CHARACTERISTICS over operating ranges

T_A = 0 to +70°C; V_{CC} = +5 V ±5%, V_{SS} = 0 V

Parameter Symbol	Parameter Descriptions	Test Conditions	Limit Values Min	Max	Unit
All pins except S_{X1}, S_{X2}, S_{R1}, S_{R2}					
V_{IL}	Input Low Voltage		–0.4	+0.8	V
V_{IH}	Input High Voltage		+2.0	V_{CC} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.45	V
V_{OL1}	Output Low Voltage (SDO only)	I_{OL} = 7 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	+2.4		V
V_{OH1}	Output High Voltage	I_{OH} = –100 µA	V_{CC} –.5		V
I_{CC}	Power Supply Current: Operational Power Down	Inputs at GND/V_{CC} V_{CC} = 5 V No output loads		 13 ±1.0	 mA mA
I_{LI}	Input Leakage Current	0 V < V_{IN} < V_{CC} to 0 V		±10	µA
I_{LO}	Output Leakage Current	0 V < V_{OUT} < V_{CC} to 0 V		±10	µA
S_{X1}, S_{X2}					
V_X	Absolute Value Of Output Pulse Amplitude (V_{SX2} – V_{SX1})	 R_L = 200 ohm* R_L = 1600 ohm*	 2.03 2.10	 2.31 2.39	 V V
I_X	Transmitter Output Current	R_L = 22.4 ohm	7.5	13.4	mA
R_X	Transmitter Output Impedance	Inactive or during binary one During binary zero R_L = 200 ohm**	10 0		kohm ohm
S_{R1}, S_{R2}					
V_{SR1}	Receiver Bias Voltage	I_O < 5 µA	2.35	2.6	V
V_{TR}	Receiver Threshold voltage V_{SR2} – V_{SR1}	Dependent on peak level	+225	+375	mV

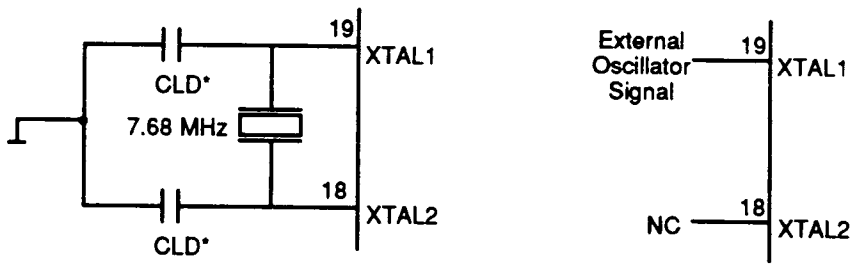
*Load resistance on S-interface line is divided by four. The required 20 ohm output impedance is realized by external components.
**The 80 ohm output impedance is realized by external components.

CAPACITANCE*

T_A = 0 to 70°C, V_{CC} = +5 V ±5%, V_{SS} = 0 V, f_c = 1 MHz

Parameter Symbol	Parameter Descriptions	Test Conditions	Limit Values Min	Max	Unit
All pins except S_{X1}, S_{X2}					
C_{IN}	Input Capacitance			7	pF
$C_{I/O}$	I/O Capacitance			7	pF
S_{X1}, S_{X2}					
C_{OUT}	Output Capacitance against V_{SSA}			10	pF
XTAL1, XTAL2					
C_{LD}	External Load Capacitance			50	pF

*Parameters are not "Tested." Unmeasured pins returned to ground.



Crystal Oscillator Mode

Driving From External Source

*CLD ≤ 50 pF. The integrated oscillator uses a parallel resonance crystal.

11135-014A

Figure 31. Recommended Oscillator Circuits

Table 7. Output Stages

Application	Operation of IOM Interface	M2	M1	M0	DCL	FSC	CP	X2	X1	X0	SDO
TE	Inverted Mode	0	0	0	Push/pull	Push/pull	Push/pull	Push/pull	Push/pull	Push/pull	Push/pull
TE	Inverted Mode	0	0	1	Push/pull	Push/pull	Push/pull	Push/pull	Push/pull	Push/pull	Push/pull
TE	IOM-1 Mode	0	1	0	Push/pull	Push/pull	Push/pull	Push/pull	Push/pull		Push/pull
LT-T	IOM-2 Mode or Inverted MUX Mode	0	1	1			Push/pull				Open drain
LT-T	IOM-1 Mode	0	1	1			Push/pull				Push/pull
NT	IOM-1 Mode	1	1	1						*Open drain	*Open drain
LT-S	IOM-2 Mode or Inverted MUX Mode	1	0	0							Open drain
LT-S	IOM-1 Mode	1	1	0					Push/pull		Push/pull
LT-S	IOM-1 Mode	1	1	0				Push/pull	Push/pull		

*With internal pull-up.

Table 8. SBC Clock Signals

Application	Operation of IOM Interface	M2	M1	M0	DCL	FSC	CP	X2	X1	X0
TE	Inverted Mode	0	0	0	O:512 kHz* 1:2	O:8 kHz* 63:1	O:1536 kHz* 3:2	O:2560 kHz 1:2	O:3840 kHz 1:1	
TE	Inverted Mode	0	0	1	O:512 kHz* 1:2	O:8 kHz* 63:1	O:1536 kHz* 3:2	O:1280 kHz 1:2	O:3840 kHz 1:1	
TE	IOM-1 Mode	0	1	0	O:512 kHz* 2:1	O:8 kHz* 1:1	O:1536 kHz* 3:2		O:3840 kHz 1:1	
LT-T	IOM-2 Mode or Inverted MUX Mode	0	1	1	I:4096 kHz	I:8 kHz	O:512 kHz 2:1			
LT-T	IOM-1 Mode	0	1	1	I:512 kHz	I:8 kHz	O:512 kHz* 2:1			
NT	IOM-1 Mode	1	1	1	I:512 kHz	I:8 kHz				
LT-S	IOM-2 Mode or Inverted MUX Mode	1	0	0	I:4096 kHz	I:8 kHz				
LT-S	IOM-1 Mode	1	1	0	I:512 kHz	I:8 kHz			O:7680 kHz 1:1	I:fixed at 0
LT-S	IOM-1 Mode	1	1	0	I:512 kHz	I:8 kHz		O:192 kHz* 1:1	O:7680 kHz 1:1	I:fixed at 1

*Synchronous to receive "S" line.

Input and Output Pin Configurations

In TE, LT-T and LT-S IOM-1 modes, an integrated pull-up resistor is connected to SDI. For output pin configurations, see Table 7.

SWITCHING CHARACTERISTICS

T_A = 0 to +70°C, V_{CC} = 5 V + 5%

The AC testing input/output waveform is shown below.

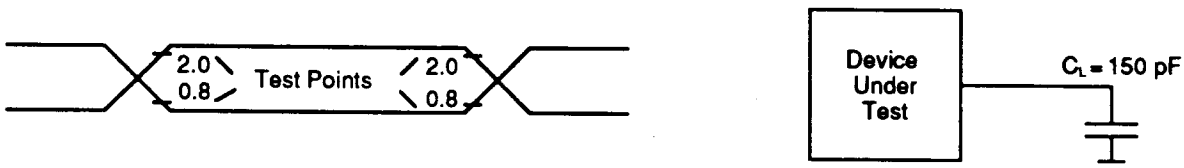
Jitter

In TE mode, the timing extraction jitter of the SBC conforms to CCITT Recommendation I.430 (–7% to +7% of the S-interface bit period). In the NT and LT-S applications, the clock input DCL is used as a reference clock to provide the 192-kHz clock for the S-line interface. In the case of a plesiochronous 7.68-kHz clock generated by an oscillator, the clock DCL should have a jitter of less than 100 ns peak-to-peak. (In the case of a zero input jitter on DCL, SBC generates at most 130 ns self-jitter on S-interface.) In case of a synchronous (fixed divider ratio of 15 between XTAL1 and DCL) 7.68-MHz clock (input XTAL1), the SBC transfers the input jitter of XTAL1, DCL and FSC to the S-interface. The maximum jitter of the NT/LT-S output is limited to 260-ns peak-to-peak (CCITT I.430).

Clock Timing

The clocks in the different operating modes are summarized in Table 6, with the respective duty ratios. Clock CP is phase-locked to the receive S signal, and is derived using the internal DPLL and the 7.68 MHz ±100 ppm crystal (TE and LT-T).

A phase tracking of CP with respect to "S" is performed once in 250 µs. As a consequence of this tracking, the high state of CP may be either reduced or extended by one 7.68 MHz period (CP duty ratio 2:2 or 4:2 instead of 3:2) once every 250 µs. Since DCL and FSC are derived from CP (TE mode), the high state (FSC) or the high or low state (DCL) may likewise be reduced or extended by the same amount once every 250 µs. The phase adjustment may take place either in the sixth, seventh, or eighth CP cycle counting from the beginning of an IOM frame in TE. The phase relationships of the auxiliary clocks are shown in Figure 32. Tables 9–13 give the timing characteristics of the clocks.



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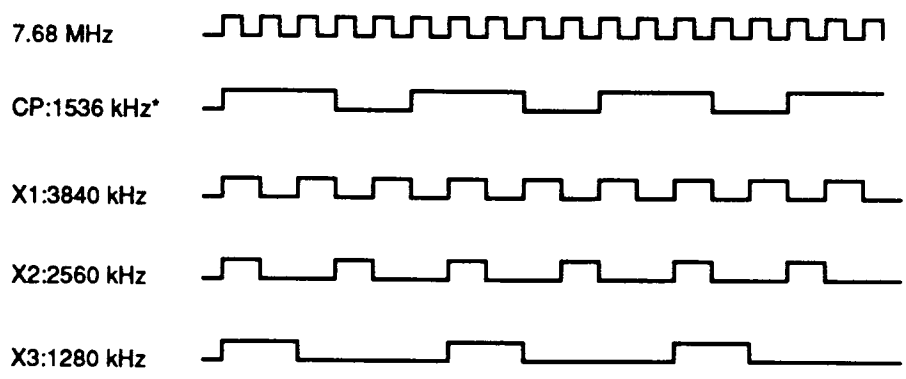


*Synchronous to receive S, see Jitter. Duty ratio 3:2 normally.

Figure 32. Phase Relationships of Auxiliary Clocks

11135-016A

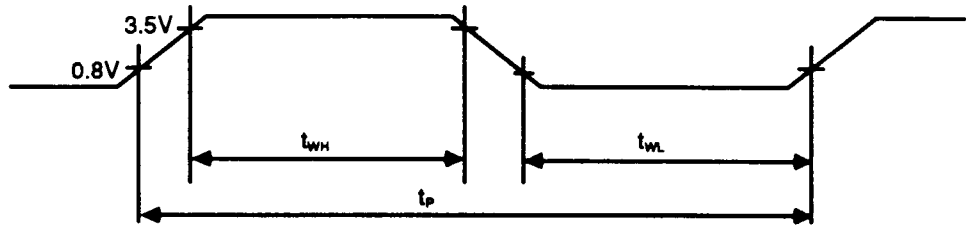


Figure 33. Definition of Clock Period and Width

11135-017A

Table 9. XTAL1 and XTAL2 Timing Characteristics

Symbol	Description	Min	Max	Units	Conditions
t_{WH} Input	High Phase of Crystal/Clock	20		ns	
t_{WL} Input	Low Phase Crystal/Clock	20		ns	

Table 10. DCL Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
t_P Output	(TE) 512 kHz	1822	1953	2084	ns	osc ±100 ppm
t_{WH} Output	(TE) 512 kHz 2:1	1121	1302	1483	ns	osc ±100 ppm
t_{WL} Output	(TE) 512 kHz 2:1	470	651	832	ns	osc ±100 ppm
t_{WH} Output	(TE) 512 kHz 1:2	470	651	832	ns	osc ±100 ppm
t_{WL} Output	(TE) 512 kHz 1:2	1121	1302	1483	ns	osc ±100 ppm
t_{WH} Input	(NT, LT-S, LT-T)	90			ns	
t_{WL} Input	(NT, LT-S, LT-T)	90			ns	

Table 11. CP Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
t_P Output	(TE) 1536 kHz	520	651	782	ns	osc ±100ppm
t_{WH} Output	(TE) 1536 kHz 2:1	240	391	541	ns	osc ±100 ppm
t_{WL} Output	(TE) 1536 kHz 2:1	240	260	231	ns	osc ±100 ppm
t_R, t_F	(TE, LT-T)			20	ns	C_L = 100 pF
				10	ns	C_L = 50 pF
t_P Output	(LT-T) 512 kHz	1822	1953	2084	ns	osc ±100 ppm
t_{WH} Output	(LT-T) 512 kHz	1121	1302	1483	ns	osc ±100 ppm
t_{WL} Output	(LT-T) 512 kHz	470	651	832	ns	osc ±100 ppm

Table 12. X1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
t_P Output	(TE) 3840 kHz	−100 ppm	260	+100 ppm	ns	osc ±100 ppm
t_{WH} Output	(TE) 3840 kHz	120	130	140	ns	osc ±100 ppm
t_{WL} Output	(TE) 3840 kHz	120	130	140	ns	osc ±100 ppm

Table 13. X2 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
t_P Output	(TE) 2560 kHz	−100 ppm	391	+100 ppm	ns	osc ±100 ppm
t_{WH} Output	(TE) 2560 kHz	110	130	150	ns	osc ±100 ppm
t_{WL} Output	(TE) 2560 kHz	250	260	270	ns	osc ±100 ppm
t_P Output	(TE) 1280 kHz	−100 ppm	781	+100 ppm	ns	osc ±100 ppm
t_{WH} Output	(TE) 1280 kHz	250	260	270	ns	osc ±100 ppm
t_{WL} Output	(TE) 1280 kHz	511	521	531	ns	osc ±100 ppm

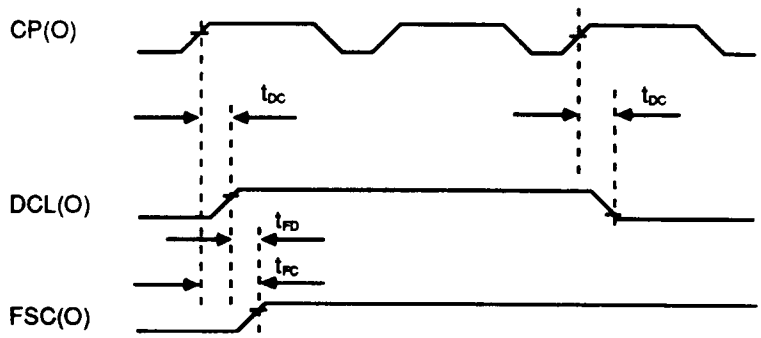


Figure 34. CP, DCL, and FSC Relationships in IOM Master Mode 11135-018A

Table 14. IOM Master Mode Timing Characteristics

Symbol	Description	Min	Max	Unit	Conditions
t_{DC}	Clock delay CP-DCL	0	50	ns	C_L = 100 pF
t_{FC}	Clock delay CP-FSC	0	50	ns	C_L = 100 pF
t_{FD}	Delay DCL-FSC	–20	20	ns	C_L = 100 pF

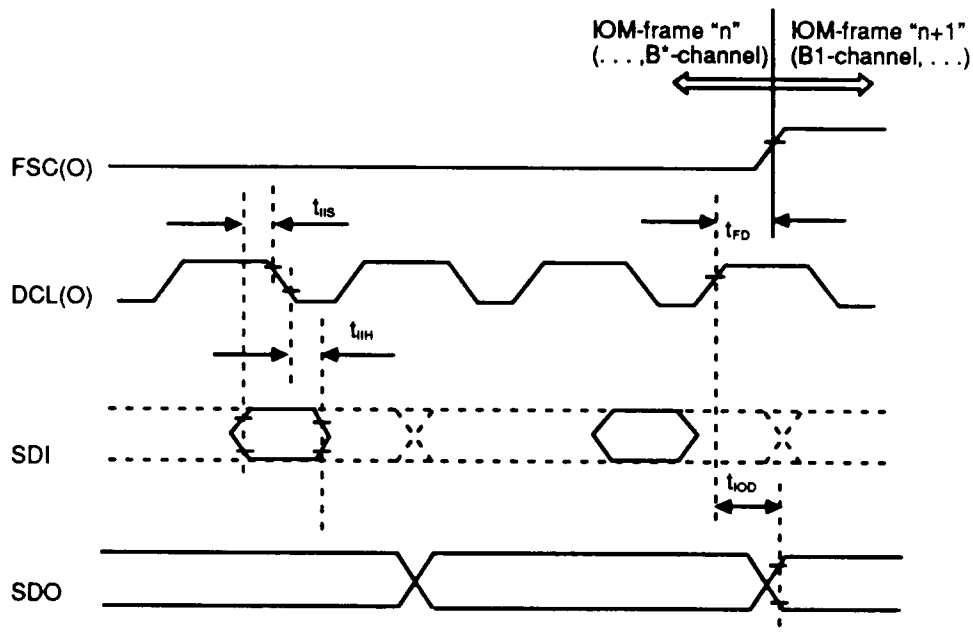


Figure 35. IOM-1 Master Mode (TE)

11135-019A

Table 15. IOM-1 Master Mode (TE) Timing Characteristics

Symbol	Parameter	Min	Max	Unit	Conditions
t_{FD}	Frame sync delay	–20	20	ns	C_L = 100 pF
t_{IOD}	IOM output data delay		200	ns	C_L = 100 pF
t_{IIS}	IOM input data setup	20		ns	
t_{IIH}	IOM input data hold	50		ns	

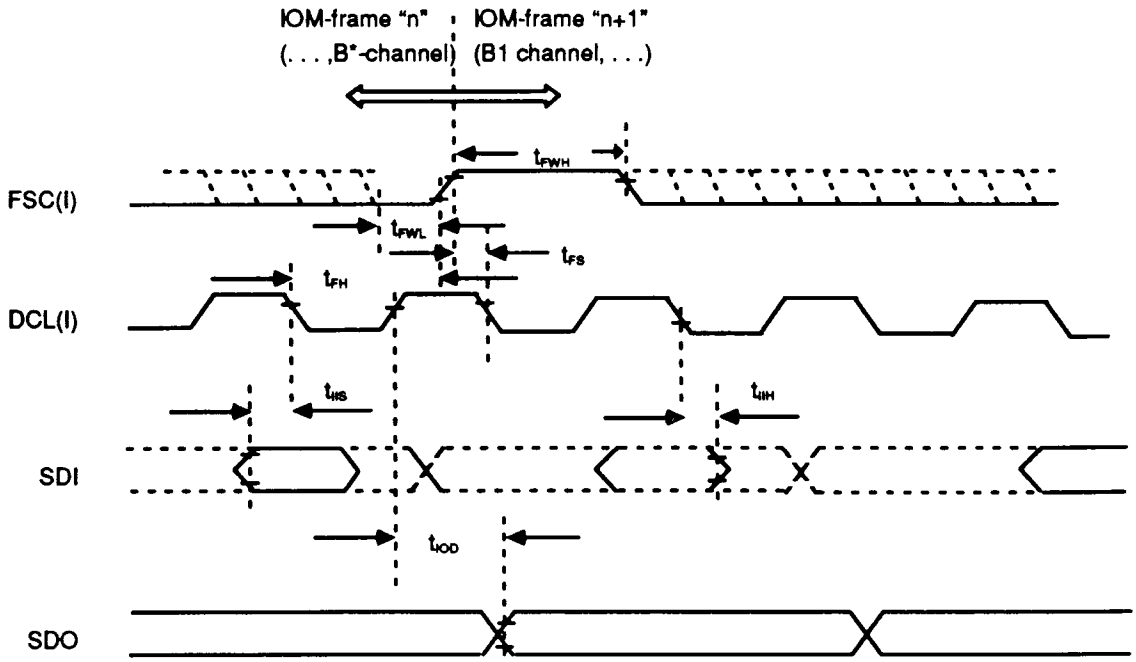


Figure 36. Slave Mode (NT, LT-S, LT-T) 11135-020A

Table 16. Slave Mode (NT, LT-S, LT-T) Timing Characteristics

Symbol	Parameter	Min	Max	Unit
t_{FH}	Frame sync hold	30		ns
t_{FS}	Frame sync setup	50		ns
t_{FWH}	Frame sync High	40		ns
t_{FWL}	Frame sync Low	2150		ns
t_{IOD}	IOM output data delay		200	ns*
t_{IIS}	IOM input data setup	20		ns
t_{IIH}	IOM input data hold	50		ns

*For push-pull output. For open drain output with integrated pull-up resistor, the maximum value is 900 ns.

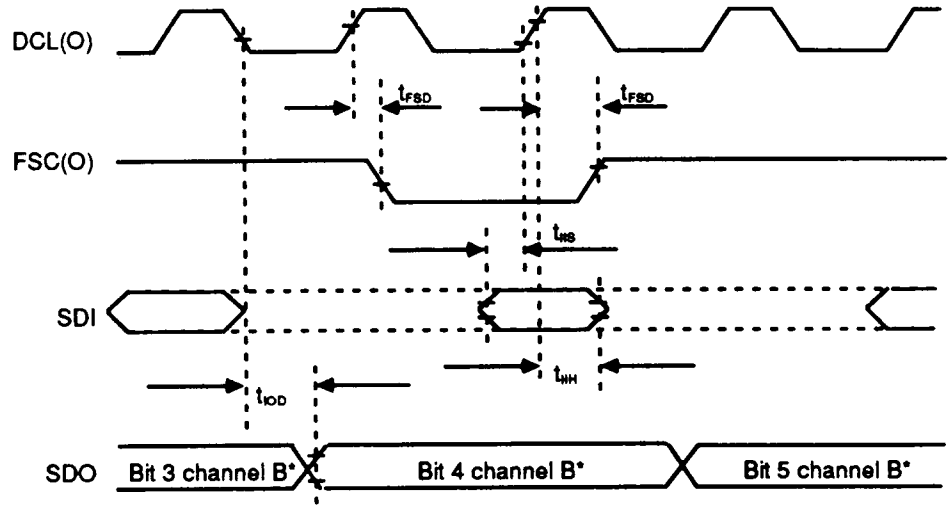


Figure 37. Inverted Mode

11135-021A

Table 17. Inverted Mode

Symbol	Parameter	Min	Max	Unit	Conditions
t_{FSD}	Frame sync delay	–20	20	ns	C_L = 100 pF
t_{IOD}	IOM output data delay		200	ns	C_L = 100 pF
t_{IIS}	IOM input data setup	20		ns	
t_{IIH}	IOM input data hold	50		ns	

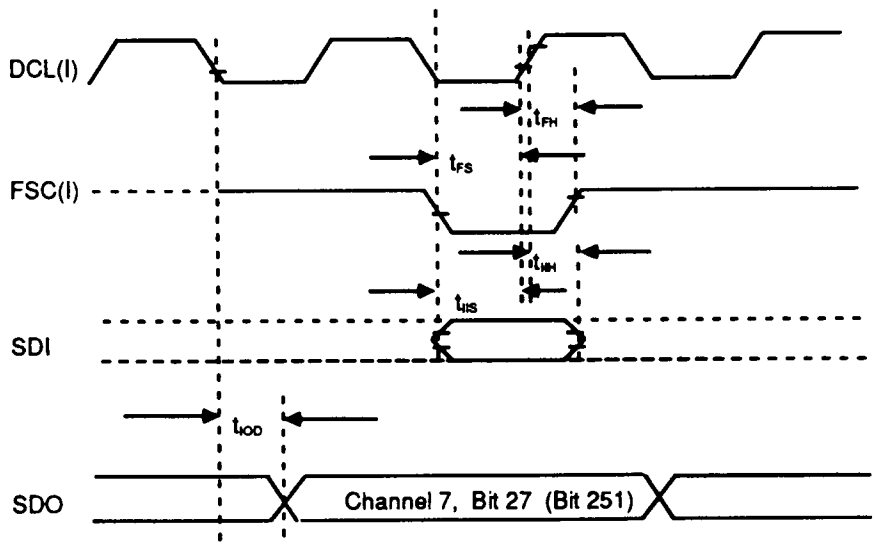


Figure 38. Inverted MUX Mode

11135-022A

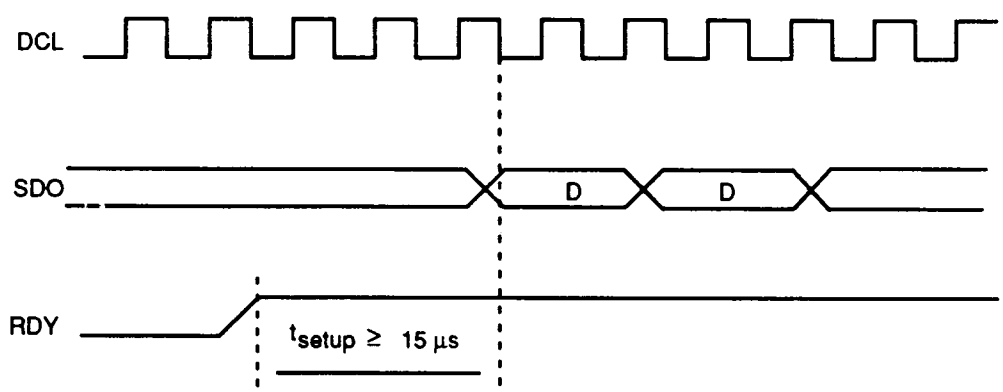
Table 18. Inverted MUX Mode

Symbol	Parameter	Min	Max	Unit	Conditions
t_{FH}	Frame sync hold	50		ns	
t_{FS}	Frame sync setup	20		ns	
t_{FWH}	Frame sync High	124.8		µs	
t_{FWL}	Frame sync Low	70	200	ns	
t_{IOD}	IOM output data delay		200	ns	C_L = 150 pF; I_{OL} = 7 mA
t_{IIS}	IOM input data setup	20		ns	
t_{IIH}	IOM output data hold	50		ns	

Timing of Special Function Pins

Table 19. $\overline{RST}$ Timing

Symbol	Parameter	Min	Max	Unit
t_{WL}	Length of Low state	1		ms



11135-023A

Figure 39. RDY Timing (X0 in TE Inverted Mode)

Table 20. RDY Timing

Symbol	Parameter	Min	Max	Unit
t_{WL}	Length of Low state	360		µs
t_{WH}	Length of High state	60		µs

DE

The timing for DE (pin X0, NT mode) is given by Figure 38 for the case of two S-interfaces having a minimum frame delay and a maximum frame delay, respectively. The corresponding star configuration is shown in Figure 40. DE timing is shown in Figure 43. The AC characteristics of DE output and input are shown in Figures 41, 42 and Table 20.

ECHO

The timing of the ECHO output (pin X2, TE mode) is identical with that of output SDO; however, the signal is 1 everywhere except in bit positions 24 and 25 of IOM frame, where it is equal to the E-bits received from the S interface.

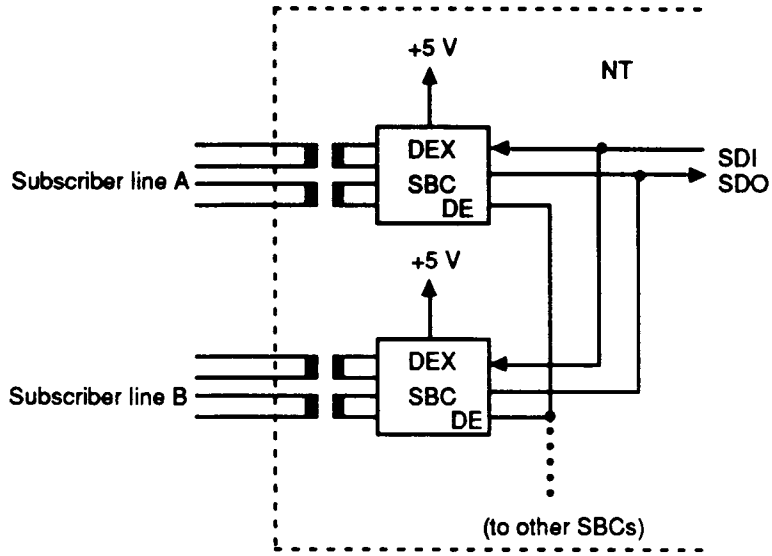


Figure 40. Star Configuration in NT

11135-024A

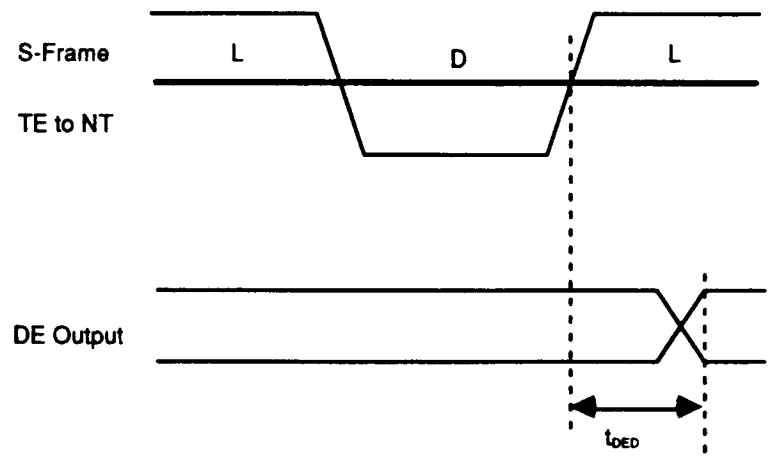
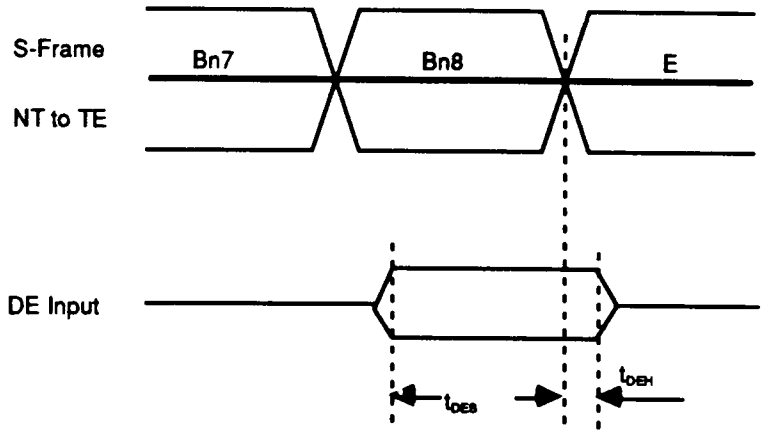


Figure 41. Timing of DE Output

11135A-025



11135A-026

Figure 42. Timing of DE Input

Table 20. DE Timing

Symbol	Parameter	Min	Max	Unit	Conditions
t_{DED}	DE Delay		2	µs	C_L = 100 pF
t_{DES}	DE Setup	3		µs	
t_{DEH}	DE Hold	0		µs	

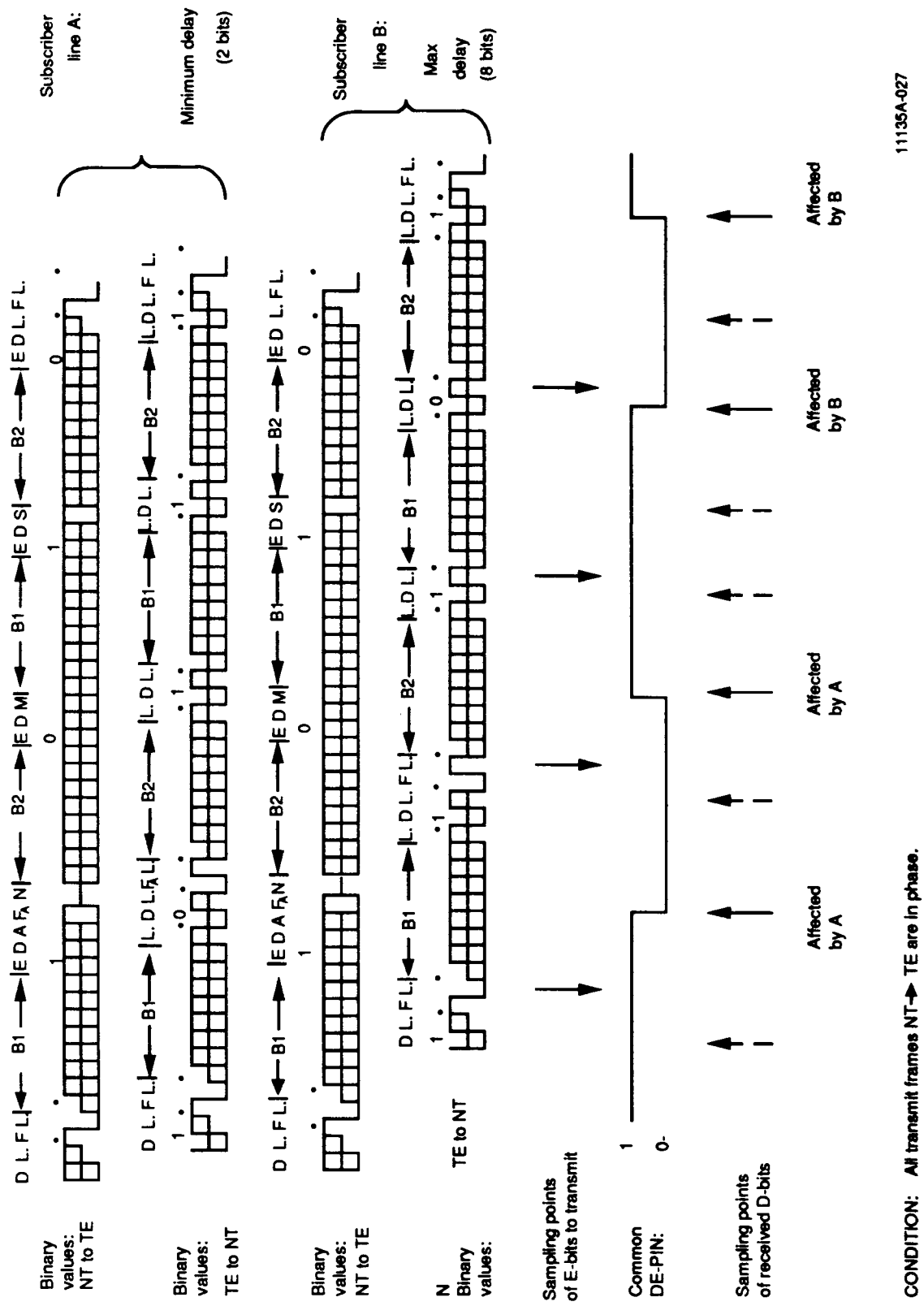
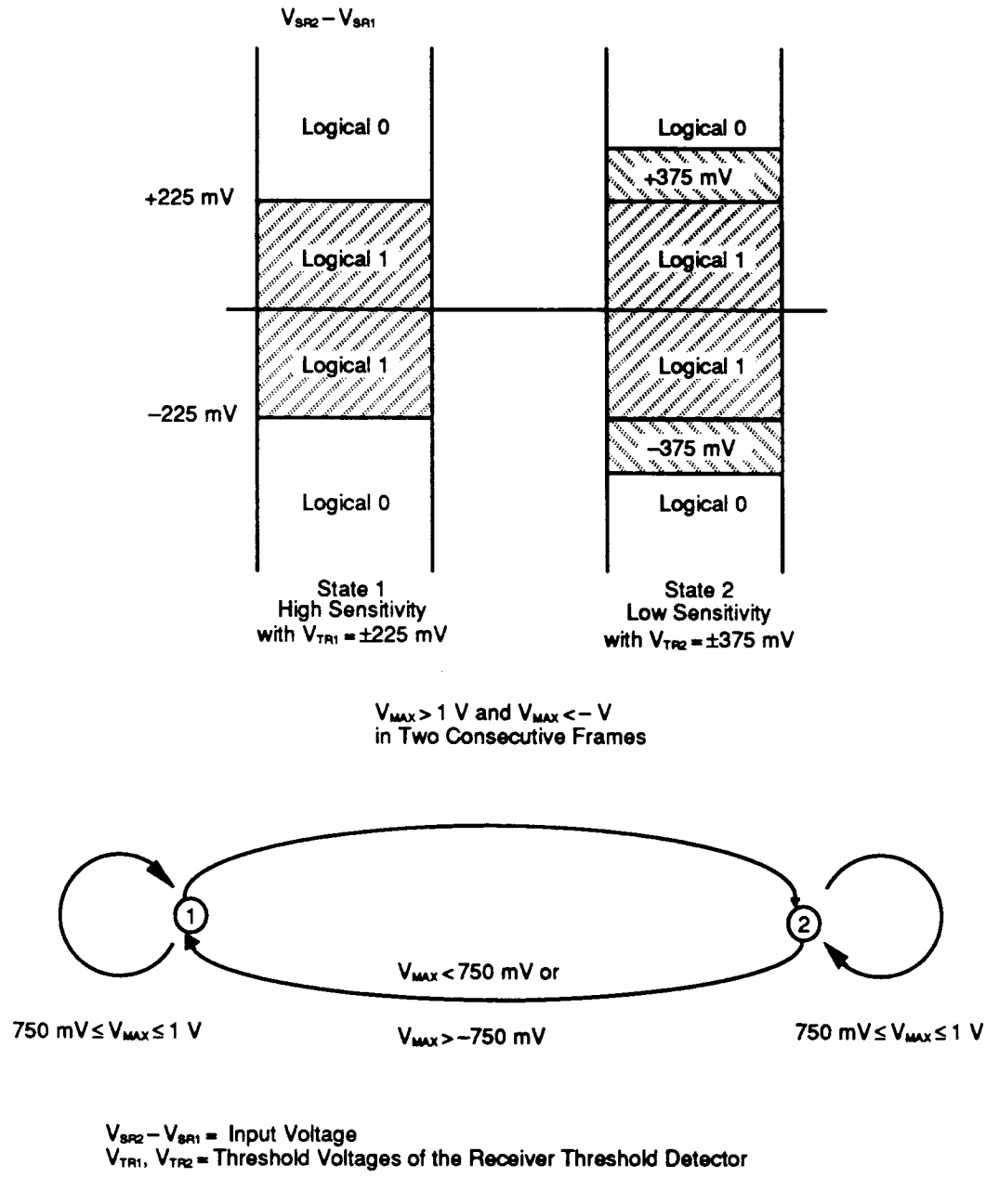


Figure 43. Functional Timing of DE

Adaptive Receiver Characteristics

The integrated receiver uses an adaptively switched threshold detector. The detector controls the switching of the receiver between two sensitivity levels. The hysteresis characteristics of the receiver are shown in Figure 44.



$V_{SR2} - V_{SR1}$ = Input Voltage
V_{TR1}, V_{TR2} = Threshold Voltages of the Receiver Threshold Detector

V_{MAX} = Maximum Value of $V_{SR2} - V_{SR1}$ during one Frame

11135A-028

Figure 44. Switching of the Receiver Between High Sensitivity and Low Sensitivity

SBC S-Bus Interface Circuit

According to CCITT I.430 the electrical characteristics of the S/T interface transmitter are to fulfill the following requirements:*

- The output impedance, when the transmitter is inactive or transmitting a binary 1, should exceed 2500 ohms. Note that this also applies to TEs with local power sources when the local power is switched off, although the TE is connected to an activated S-bus.
- The output impedance, when the transmitter is transmitting a binary 0, should be ≥ 20 ohms. Note that this also applies in the case of a 400 ohm load when the transmitter reaches a current- or voltage-limiting state.
- Pulse shape and amplitude shall be in accordance with the given pulse masks. Note that in TE applications the effective test load for the transmitter not only consists of twice the terminating resistance (50 ohms) but also of the series resistances of other external components such as the transformer and the cord (maximum length 7 m).

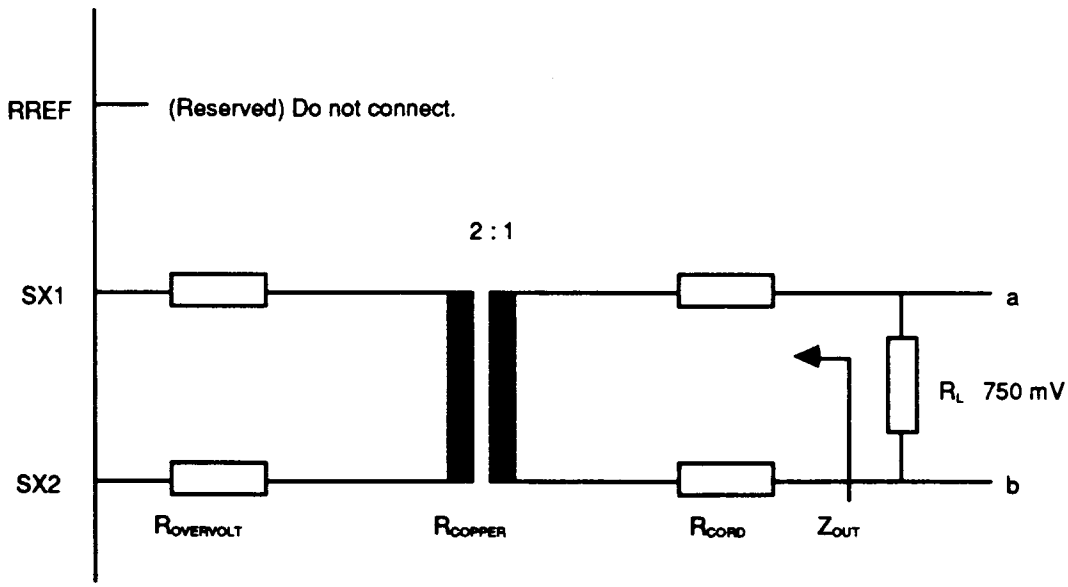
The transmitter circuitry of the Am2080 SBC meets these requirements in full.

The transmitter essentially is a current-limited voltage source, delivering nominally 1.5 V to the 2:1 transformer. The high-output impedance when transmitting a binary 1, including when the power supply is switched off, is guaranteed by the circuit design.

When transmitting a binary 0, the output impedance (Z_{OUT}) has to be in the range of 20–25 ohms in order that the pulse mask be fulfilled. Since the internal output impedance of the transmitter is negligible for a binary 0, the impedance is realized by the total sum of external resistances (Figure 45). For example:

- Resistance of cord (TE only) (R_{CORD}) 4–7 Ω
- Copper resistance of transformer (R_{COPPER}) 1–3 Ω
- Resistances for overvoltage protection of the transmitter, transformed to the primary (line) side with 4:1 ($R_{OVERVOLT}$) 15 Ω

The 50-ohms pulse mark conforms to CCITT I.430 (no overshoot).



11135A-029

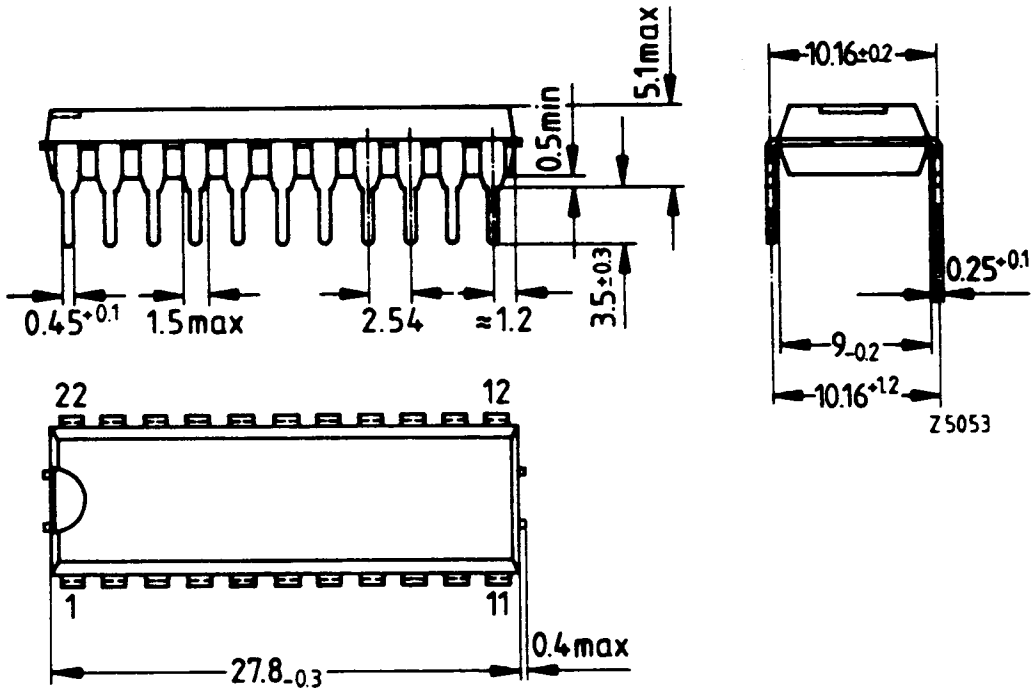
Figure 45. Transmitter Environment Model of the SBC

*ISDN User-Network Interfaces: Layer 1 Recommendations.
CCITT Recommendations of the Series I—Volume III Fascicle III.5 Integrated Services Digital Network (ISDN). VIIIth Plenay Assembly Malaga-Torrelmolinos, 8–10 October 1984.

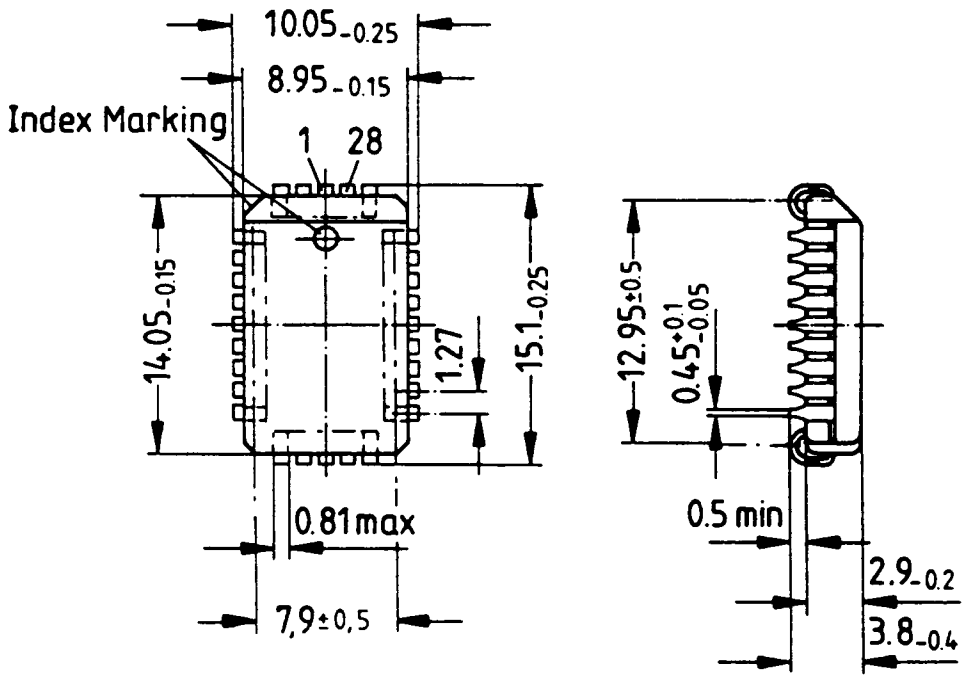
PHYSICAL DIMENSIONS

For reference only. All dimensions measured in mm. BSC is an ANSI standard for Basic Space Centering.
Preliminary; subject to change.

PD022



PLR028



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