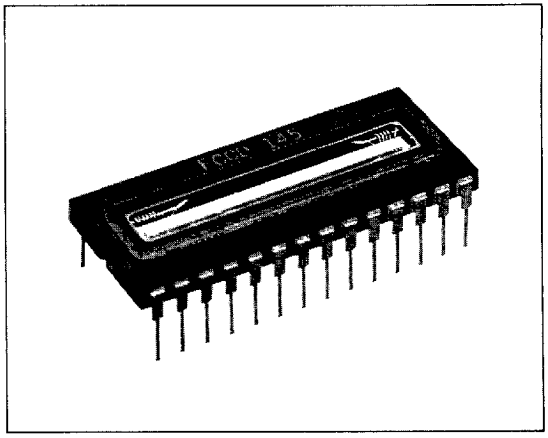
LORAL
Fairchild Imaging Sensors

CCD145
2048-Element
Linear Image Sensor



FEATURES

- **2048 × 1 photosite array**
- **13μm × 13μm photosites on 13μm pitch**
- **Anti-blooming and integration control**
- **Enhanced Spectral Response (particularly in the blue region)**
- **Low dark signal**
- **Excellent low-light-level performance**
- **High responsivity**
- **Dynamic range typical: 7500:1**
- **Over 1V peak-to-peak outputs**
- **Special selections available — consult factory.**

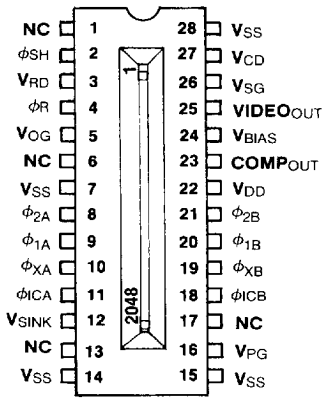
DESCRIPTION

The CCD145 is a 2048-element line image sensor designed for page scanning applications including facsimile, optical character recognition, and other imaging applications which require high resolution, high sensitivity and high dynamic range. The incorporation of on-chip anti-blooming and integration control allow the CCD145 to be extremely useful in an industrial measurement and control environment or in environments where lighting conditions are difficult to control.

The photoelement size is 13μm (0.51 mils) by 13μm (0.51 mils) on 13μm (0.51 mils) centers. The device is manufactured using Loral Fairchild's advanced charge-coupled device n-channel Isoplanar buried-channel technology.

PIN NAMES	DESCRIPTION
V_{PG}	Photogate
ϕXA, ϕXB	Transfer Clocks
ϕ1A, ϕ2A	Transport Clocks
ϕ1B, ϕ2B	
ϕR	Reset Clock
ϕSH	Sample-and-Hold Clock
ϕICAϕICB	Integration Control Clocks
$VIDEO_{OUT}$	Output Amplifier Source
$COMP_{OUT}$	Compensation Amplifier Source
V_{DD}	Output Amplifier Drain
V_{CD}	Compensation Amplifier Drain
RD	Reset Drain
OG	Output Gate
V_{SINK}	Anti-Blooming Sink
V_{BIAS}	Amplifier Bias
V_{SG}	Amplifier Signal Ground
V_{SS}	Substrate Ground
NC	No Connection

PIN CONNECTION DIAGRAM
(TOP VIEW)



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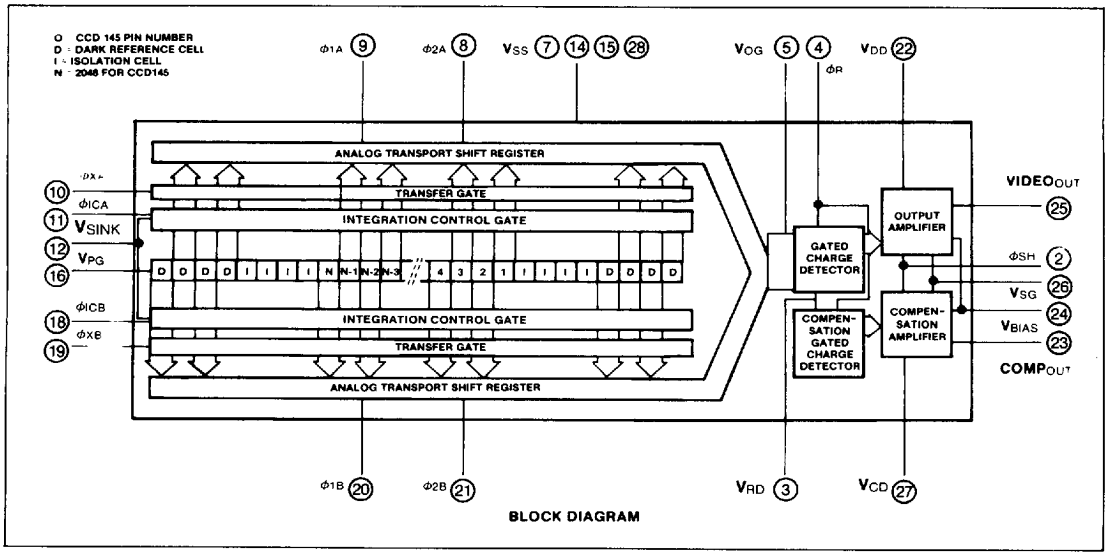


FUNCTIONAL DESCRIPTION

The CCD145 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 2048 image sensor elements separated by a diffused channel stop and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon, creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates — Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers whenever the transfer gate voltages go HIGH. Alternate charge packets are transferred to the A and B transport registers.

Integration and Anti-Blooming Control — In many applications the dynamic range in parts of the image is larger than the dynamic range of the CCD, which may cause more electrons to be generated in the photosite area than can be stored in the CCD shift register. This is particularly common in industrial inspection and satellite applications. The excess electrons generated by bright illumination tend to "bloom" or "spill over" to neighboring pixels along the shift register, thus "smearing" the information. This smearing can be eliminated by using two methods:

Anti-Blooming Operation:

A DC voltage applied to the integration control gate (approximately 5 to 7 volts) will cause excess charge generated in the photosites to be diverted to the anti-blooming sink (V_{SINK}) instead of to the shift registers. This acts as a "clipping circuit" for the CCD output (see Fig. 2).

Integration Control Operation:

Variable integration times which are less than the CCD exposure time may be attained by supplying a clock to the integration control gate. Clocking ϕ_{IC} reduces the photosite signal in all photosites by the ratio $t_{EXPOSURE}/t_{INT}$. Greater than 10:1 reduction in the average photosite signal can be achieved with integration control.

The integration-control and anti-blooming features can be implemented simultaneously. This is done by setting the ϕ_{IC} clock-low level to approximately 5 to 7 volts. (See application note for further discussion).

Two Analog Transport Shift Registers — One on each side of the line of image sensor elements and are separated from it by a transfer gate. The two registers, called the transport registers, are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector/amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets to establish the original serial sequence of the line of video in the output circuit.

A Gated Charge Detector/Amplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal at the output $VIDEO_{OUT}$. A reset transistor is driven by the reset clock (ϕ_R) and recharges the charge detector diode before the arrival of each new signal charge packet from the transport registers.

DEFINITION OF TERMS

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Transfer Clocks ϕ_{XA}, ϕ_{XB} — The voltage waveforms applied to the transfer gates to move the accumulated charge from the image sensor elements to the CCD transport registers.

Transport Clocks ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase waveforms applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the gated charge detector/amplifier.

Sample-and-Hold Clock ϕ_{SH} — The voltage waveform applied to the sample-and-hold gate in the output amplifier to create a continuous sampled video signal at the output. The sample-and-hold feature may be defeated by connecting ϕ_{SH} to V_{DD}.

Reset Clock ϕ_R — The voltage waveform required to reset the voltage on the charge detector.

Dark Reference — Video output level generated from sensing elements covered with opaque metalization which provides a reference voltage equivalent to device operation in the dark. This permits use of external DC restoration circuitry.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range — The saturation exposure divided by the rms noise equivalent exposure. Dynamic range is sometimes defined in terms of peak-to-peak noise. Peak-to-peak noise is generally equal to four to six times rms noise.

RMS Noise Equivalent Exposure — The exposure level that gives an output signal equal to the rms noise level of the output in the dark.

Saturation Exposure — The minimum exposure level that will provide a saturation output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements.

Dark Signal — The output signal in the dark caused by thermally generated electrons. It is a linear function of the integration time and is highly sensitive to temperature.

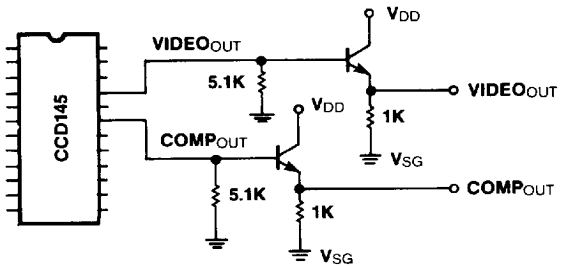
Saturation Output Voltage — The maximum useable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Exposure Time — The time interval between the falling edges of any two transfer pulses ϕ_{XA} or ϕ_{XB} as shown in the timing diagram. The exposure time is the time between transfers of signal charge from the photosites into the transport registers.

Pixel — A picture element (photosite).

Integration Time — The time elapsed from the falling edge of the integration control clock to the falling edge of the transfer clock. The integration time is the time in which charge is accumulated in the photosites.

TEST LOAD CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	-25° C to +125° C
Operating Temperature (See curves)	-25° C to +70° C
CCD 145: Pins 2, 3, 4, 5, 8, 9, 10, 11, 12, 16, 18, 19, 20, 21, 22, 24, 27	-0.3V to 18V
Pin 26	0.0V to 1V
Pins 7, 14, 15, 28	-3.0V to 0V
Pins 1, 6, 13, 17, 23, 25	NC
Pins 23, 25	See caution note.

CAUTION NOTE:
These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT}$ and $COMP_{OUT}$ to V_{SS}, V_{CD} or V_{DD} during operation of the devices. Shorting these pins even temporarily may destroy the output amplifiers.

DC CHARACTERISTICS: Tp = 25° C (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITIONS
		MIN	TYP	MAX		
V_{DD}	Output Amplifier Drain Supply Voltage	13.5	14.0	14.5	V	Note 2
I_{DD}	Output Amplifier Drain Supply Current		6.0		mA	
V_{CD}	Compensation Amplifier Drain Supply Voltage	13.5	14.0	14.5	V	Note 2
I_{CD}	Compensation Amplifier Drain Supply Current		6.0		mA	
V_{PG}	Photogate Bias Voltage	5.5	6.0	6.5	V	Note 11
V_{RD}	Output Reset Drain Supply Voltage	12.0	12.5	13.0	V	
V_{OG}	Output Gate Bias Voltage	5.0	5.5	6.0	V	
V_{SINK}	Anti-Blooming Sink Voltage	13.5	14.0	14.5	V	

CLOCK CHARACTERISTICS: Tp = 25° C

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITIONS
		MIN	TYP	MAX		
$\phi 1AL$, $V_{\phi 1BL}$ $\phi 2AL$, $V_{\phi 2BL}$	Transport Clocks LOW	0.0	0.3	0.7	V	Notes 4, 5
$\phi 1AH$, $V_{\phi 1BH}$ $\phi 2AH$, $V_{\phi 2BH}$	Transport Clocks HIGH	11.0	11.5	12.0	V	Note 5
ϕXAL, $V_{\phi XBL}$	Transfer Clocks LOW	0.0	0.3	0.7	V	Notes 4, 5
ϕXAH, $V_{\phi XBH}$	Transfer Clocks HIGH	11.0	11.5	12.0	V	Note 5
$V_{\phi RL}$	Reset Clock LOW	0.0	0.3	0.7	V	Notes 4, 5
$V_{\phi RH}$	Reset Clock HIGH	11.0	11.5	12.0	V	Note 5
$V_{\phi SHL}$	Sample Clock LOW	0.0	0.3	0.7	V	Notes 4, 5
$V_{\phi SHH}$	Sample Clock HIGH	11.0	11.5	12.0	V	Notes 5, 6
$f_{\phi 1A}$, $f_{\phi 1B}$ $f_{\phi 2A}$, $f_{\phi 2B}$	Maximum Transport Clock Frequency		4.0		MHz	Notes 7, 8
$f_{\phi R}$	Maximum Reset Clock Frequency (Ouput Data Rate)		5.0		MHz	Notes 7, 8
t_R, t_F (ϕA, $\phi 1A$, $\phi 1B$, $\phi 2B$, ϕXA, ϕXB)	Transport and Transfer Clocks Rise and Fall Times	> 20	50		ns	
$V_{\phi ICAL}$, $V_{\phi ICBL}$	Integration Control Clocks LOW		5 to 7		V	Note 9
$V_{\phi ICAH}$, $V_{\phi ICBH}$	Integration Control Clocks HIGH	11.0	11.5	12.0	V	

AC CHARACTERISTICS: Tp = 25° C, f_{data}=2.5 MHz, t_{int}=1.0ms, Light Source* = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters. All operating voltages nominal specified values. All tests done using "Test Load Configuration."

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range Relative to peak-to-peak noise Relative to rms noise		 1500:1 7500:1			
NEE	RMS Noise Equivalent exposure		 0.00004		 μJ/cm²	 Note 10
SE	Saturation Exposure		0.33		μJ/cm²	
CTE	Charge Transfer Efficiency	.99996	.99999			Note 11
V_O	Output DC Level	4.0	7.0	10	V	
P	On-Chip Power Dissipation: Amplifiers		 85	 250	 mW	
Z	Output Impedance		1		kΩ	
N	Peak-to-Peak Temporal Noise		1		mV	

PERFORMANCE CHARACTERISTICS: Tp = 25° C, f_{data}=2.5 MHz, t_{int}=1.0ms, Light Source* = 2854° K + 2.0mm thick Schott BG-38 and OCLI WBHM Filters. All operating voltages nominal specified values. Sample & Hold Clock is used.

SYMBOL	CHARACTERISTIC	RANGE			UNIT	CONDITIONS
		MIN	TYP	MAX		
PRNU**	Photoresponse Non-uniformity					
	Peak-to-peak		60	160	mV	
	Peak-to-peak without single pixel and Positive and Negative Pulses		40		mV	
	Single-pixel Positive Pulses		10	20	mV	
	Single-pixel Negative Pulses		20	40	mV	
	Register Imbalance ("Odd/Even")		20	40	mV	
DS	Dark Signal:					Note 12
	DC Component		1	2	mV	
	Low Frequency Component		1	2	mV	
SPDSNU	Single Pixel DS Non-Uniformity		1	2	mV	
R	Responsivity	3.0	4.5	7.0	V/μJcm²	
M Video	Video Mismatch		20	40		
V_{SAT}	Saturation Output Voltage	1.0	1.5	3.0	V	Note 13

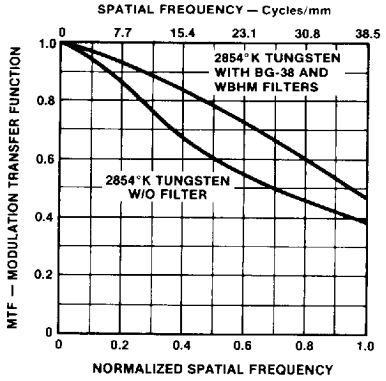
* OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror.

** All PRNU measurements are taken at an 800mV output level using an f/5.0 lens and exclude the outputs from the first and last elements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

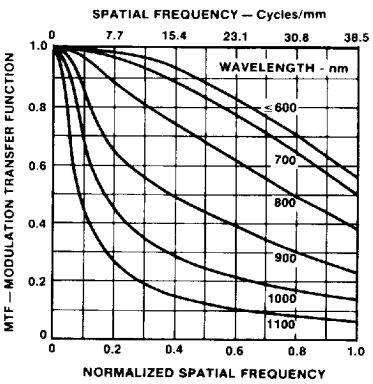
NOTES:
1. T_P is defined as the package temperature measured on a copper block in good thermal contact with the entire backside of the device.
2. V_{DD} must be connected to V_{CD}.
3. All V_{SS} pins must be connected to the same potential. V_{SS} may be less than 0.0 V.
4. Negative transients on any clock pin going below 0.0 V may cause charge injection that results in an increase in apparent dark signal.
5. $C_{\phi 1A} = C_{\phi 2A} = C_{\phi 1B} = C_{\phi 2B}$ = 250pF; $C_{\phi XA} = C_{\phi XB}$ = 150pF; $C_{\phi R} = C_{\phi SH}$ = 5pF.
6. ϕ_{SH} may be held high for operation with external sample and hold circuitry. This employed for the highest linearity. See output photographs.
7. Minimum block frequency is limited by increase in dark signal.
8. $0.5f_{\phi R} = F_{\phi 1A} = F_{\phi 2A} = F_{\phi 1B} = F_{\phi 2B}$.
9. See Maximum Output Voltage vs. ϕ_{IC} Voltage curve.
10. 1μJ/cm² = 42 lux-s/cm² for a 2854° K source with 2.0mm Schott BG-8 and OCLI WBHM filters.
11. CTE is defined for a one-stage transfer.
12. Dark signal doubles for every 7° C increase in T_P typically.
13. See test load configuration.

TYPICAL PERFORMANCE CURVES

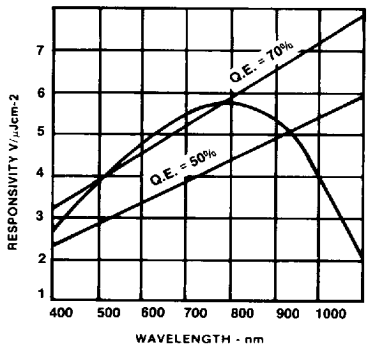
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



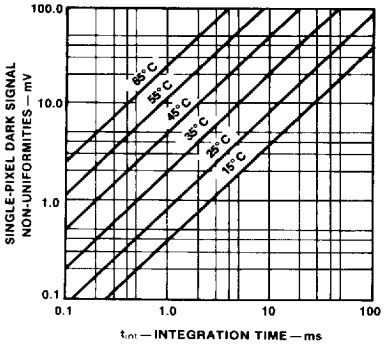
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



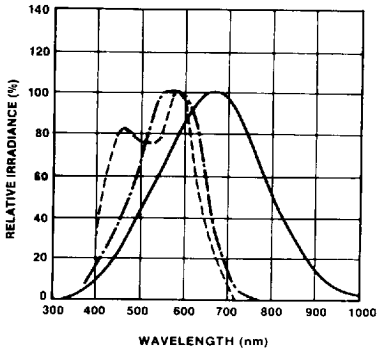
TYPICAL SPECTRAL RESPONSE



SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME

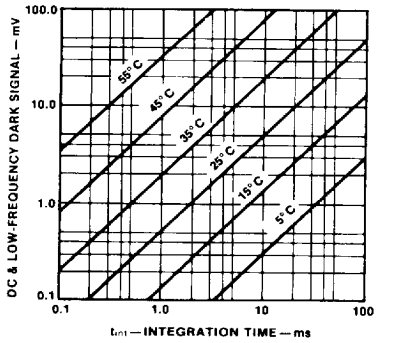


*RELATIVE RADIANT FLUX VS WAVELENGTH

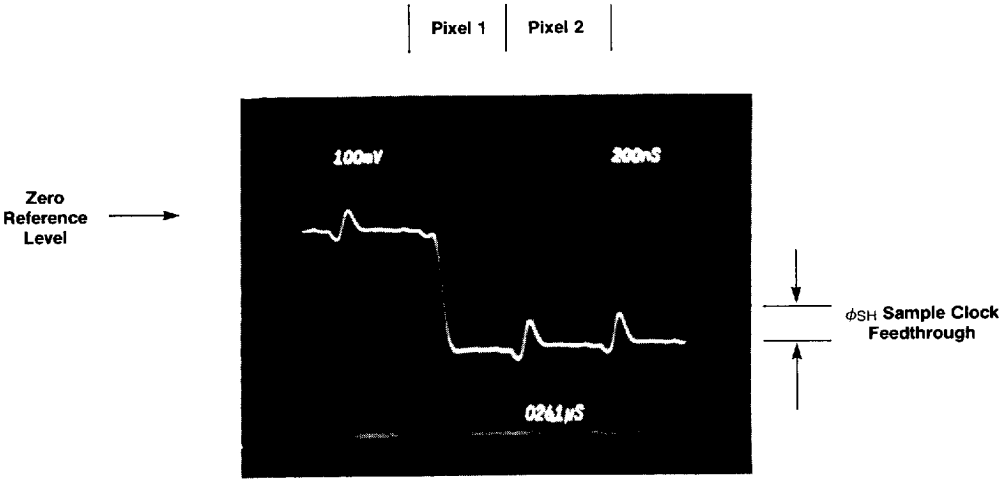


— — — TYPICAL "DAYLIGHT FLUORESCENT" BULB
— · — 2854°K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38
——— 2854°K LIGHT SOURCE + 3.0 mm THICK 1-75

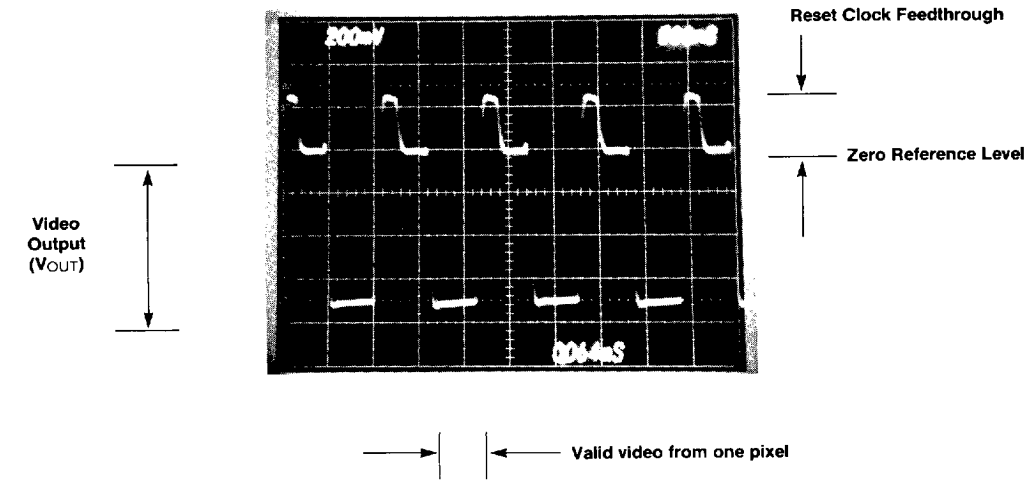
DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME



CCD145 OUTPUT PHOTOGRAPHS

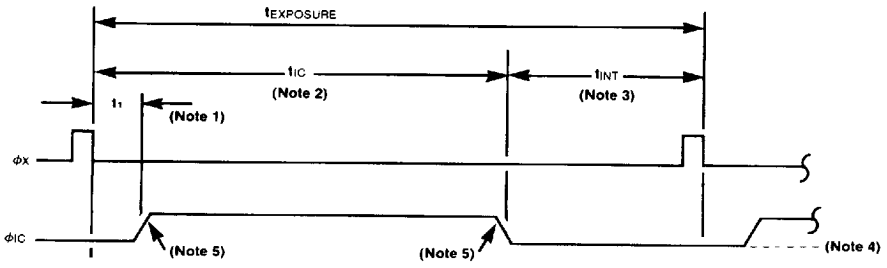


V_{OUT} with ϕ_{SH} employed.



V_{OUT} with ϕ_{SH} held high.

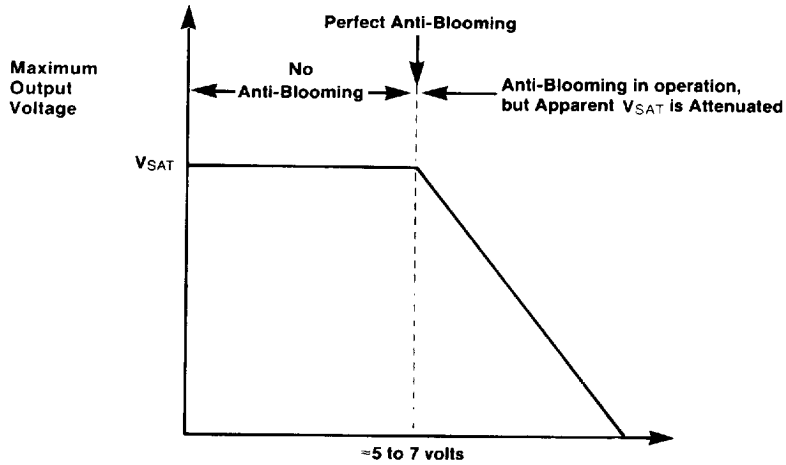
FIGURE 1: INTEGRATION CONTROL TIMING DIAGRAM



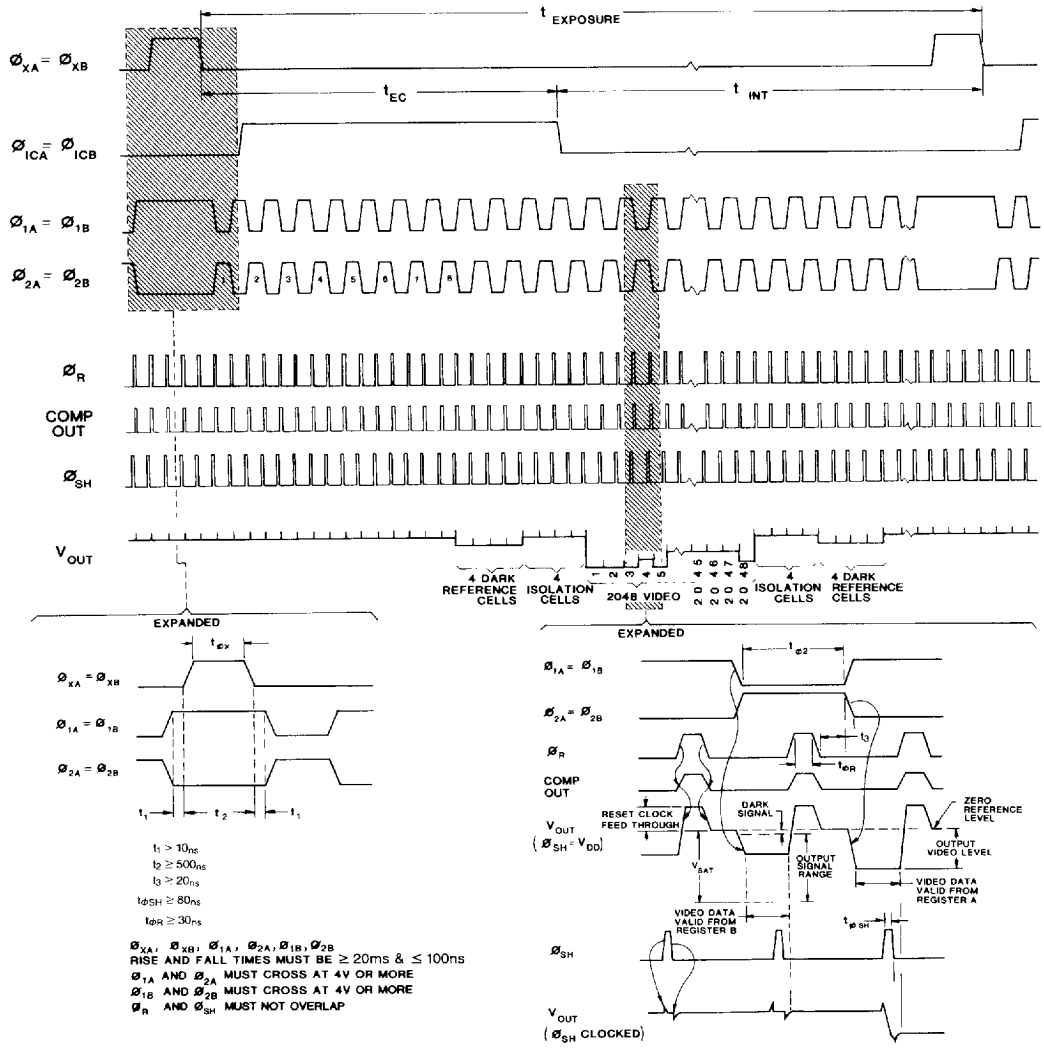
NOTES:

1. $t_1 > (t_{fall}$ of $\phi x)$.
2. All charge generated in photosites during t_{IC} is dumped in V_{SINK}.
3. All charge generated in photosites < Q_{SAT} during t_{INT} is transferred into the shift registers during ϕx clock-high period. Photosite charge > Q_{SAT} (shift reg.) generated during t_{INT} goes into V_{SINK} if anti-blooming voltage is optimized.
4. ϕ_{IC} clock-low ≈ 5 to 7 volts will give best anti-blooming operation.
5. ϕ_{IC} t_{rise} & $t_{fall} > 4\mu s$ to minimize clock coupling of ϕ_{IC} into V_{OUT}.
6. To eliminate integration control, but retain anti-blooming $\phi_{IC} \approx +5$ VDC.
7. To eliminate both integration control and anti-blooming, ϕ_{IC} = 0VDC or V_{SS}(−2V).
8. To use integration control without anti-blooming, use ϕ_{IC} clock-low = 0.0 to 0.7 volts and ϕ_{IC} clock-high = same range as ϕ_T or ϕ_1 clock-high voltage.

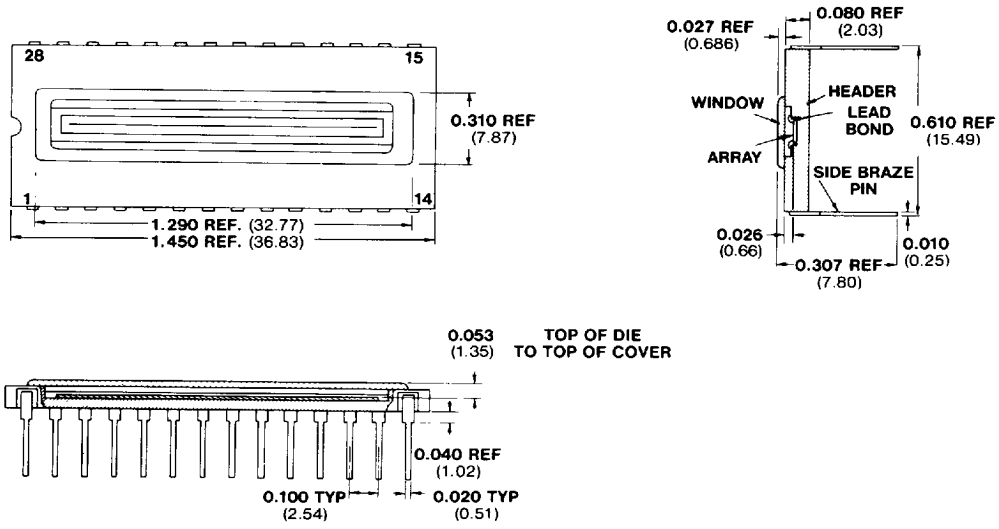
FIGURE 2: MAXIMUM OUTPUT VOLTAGE vs. ϕ_{IC} VOLTAGE



TIMING DIAGRAM



CCD145DC PACKAGE OUTLINE
28-Pin Dual In-line Ceramic Package



NOTES

All dimensions in inches (bold) and millimeters (parentheses). Header is black ceramic (Al_2O_3) Window is glass The amplifier of the device is located near the notched end of the package

DEVICE CARE AND OPERATION:

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with de-ionized water. Allow the glass to dry preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal DC and low frequency components approximately double for every 5° C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8° C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION:

Order CCD145 DC where "D" stands for a ceramic package and "C" for commercial temperature range.

WARRANTY

Within twelve months of delivery to the end customer, Loral Fairchild will repair or replace, at our option, any Loral Fairchild camera product if any part is found to be defective in materials or workmanship. Contact factory for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Loral Fairchild Division certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specification under which it is furnished.

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Fairchild Imaging Sensors