CPL22V10

CMOS PROGRAMMABLE LOGIC ARRAY WITH OUTPUT MACROCELLS (24-PIN)

FEATURES/BENEFITS

- **Low power CMOS programmable alternative to bipolar 22V10 PLDs**
- **Two speed grades:**
  t_{PD} = 25ns Max, t_{PD} = 35ns Max
- **Two power grades: 55mA Max, 90mA Max**
- **CMOS, UV-erasable EPROM cell allows reprogrammability in windowed packages**
- **10 input/output macrocells for maximum flexibility**
  - **Up to 22 inputs and 10 outputs**
  - **Programmable output polarity**
  - **Registered or combinatorial output selection**
  - **Programmable feedback path**
- **Variable product term distribution**
  - **From 8 to 16 product terms available per output**
- **Global synchronous preset and asynchronous reset of all registers**
- **Registers reset on power-up**
- **Test arrays and preloadable output registers improve testability**
- **100% functional, AC, DC, and programming tests improve reliability and programming yields**
- **>2000V ESD input protection**
- **Security bit prevents CPL pattern duplication**

DESCRIPTION

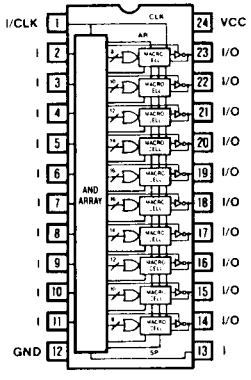
The CPL22V10 is a high-speed CMOS electrically programmable, UV-erasable device with an advanced architecture. The device is manufactured using Samsung's 1.2 micron EPROM technology offering low power dissipation combined with high performance. The UV-erasability of the device allows for 100% programming, functional, DC, and AC testing, resulting in a highly reliable end product and 100% programming yields.

The CPL22V10 uses the standard programmable AND/Fixed OR logic array structure familiar to most programmable logic users to implement complex logic functions. The array is made up of 10 sets of product terms, each connected to a programmable macrocell via an OR gate. Each set contains from 8 to 16 product terms where each product term can be connected to 22 inputs, true or complement. Each of the 10 OR array outputs feeds a programmable macrocell enabling it to be programmed as a combinatorial or registered, active high or low output.

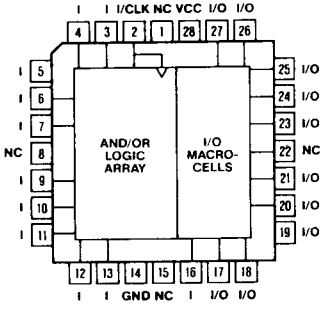
The CPL22V10 device can be housed in a 24-pin plastic DIP, 28-pin PLCC, or a windowed 24-pin CERDIP package. The windowed-CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The CPL device in a plastic package is One-Time-Programmable (OTP) and may not be erased.

3

PIN CONFIGURATIONS

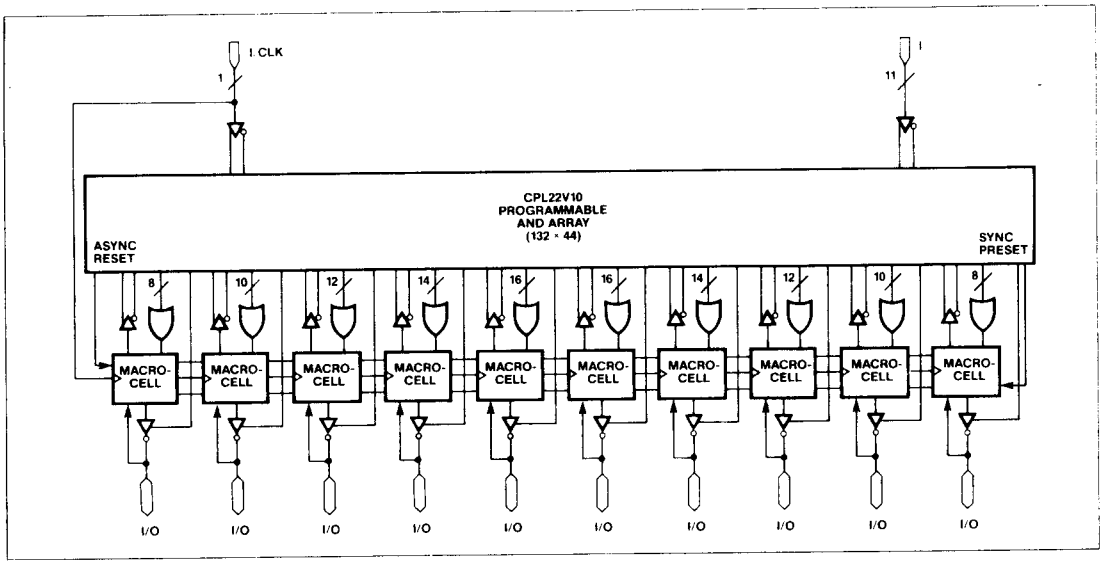


Dual In-Line Package



Plastic Leaded Chip Carrier

Figure 1. Block Diagram



The block diagram of the CPL22V10 device is shown in Figure 1. There are 12 dedicated inputs and 10 programmable macrocell outputs, which also serve as inputs. In addition, pin 1 acts either as a clock for each of the D-type registers or as another input. Each input and its complement is connected to a programmable AND array which contains a total of 120 product terms. Specifically, 8, 10, 12, 14, or 16 product terms drive each OR gate, which subsequently drives an output macrocell.

CONFIGURABLE OUTPUT MACROCELLS

One of the CPL22V10's unique features is its 10 user-configurable output macrocells. Each macrocell is programmed on an individual basis to provide one of four output configurations: combinatorial active low, combinatorial active high, registered active low, or registered active high as in Figure 2. Each output configuration is achieved by the programming of two additional bits (B0 and B1) as shown in Figure 3. Bit B1 controls whether the output will be registered or combinatorial, and bit B0 controls the output polarity, either active high or active low. These programmable functions are specified by the user in the design file specification during the design process.

When a registered output is chosen, the signal is shifted out on the positive clock transition to the I/O pin and also fed back into the array, providing current status information to the programmable array. This is important for state machine applications. When a combinatorial output is chosen or when the output is disabled and the signal is on the I/O pin, the signal is also fed back into the array. Note that the appropriate feedback path changes with the output mode.

PROGRAMMABLE OUTPUT ENABLE

Also associated with each of the 10 outputs in the CPL22V10 is an output enable (OE) product term, connected to the three-state output buffer. The OE product term can be implemented to represent any function of device inputs and output feedback combinations. As a result, each output can be selected as a bi-directional input/output or an output with feedback, when the buffer is enabled. Each output can be used as an input, when the buffer is disabled.

VARIABLE PRODUCT TERM DISTRIBUTION

The CPL22V10 not only provides an increased number of product terms on average, from eight in previous generation PLDs to the current 12 per output, but also provides variable product term distribution. The actual product term distribution varies from eight to sixteen, with one set of 8, 10, 12, 14, or 16 product terms available to each OR gate. This provides an advantage to the user who can now efficiently optimize his/her design to fit higher complexity functions or applications.

Figure 2. Configuration Options

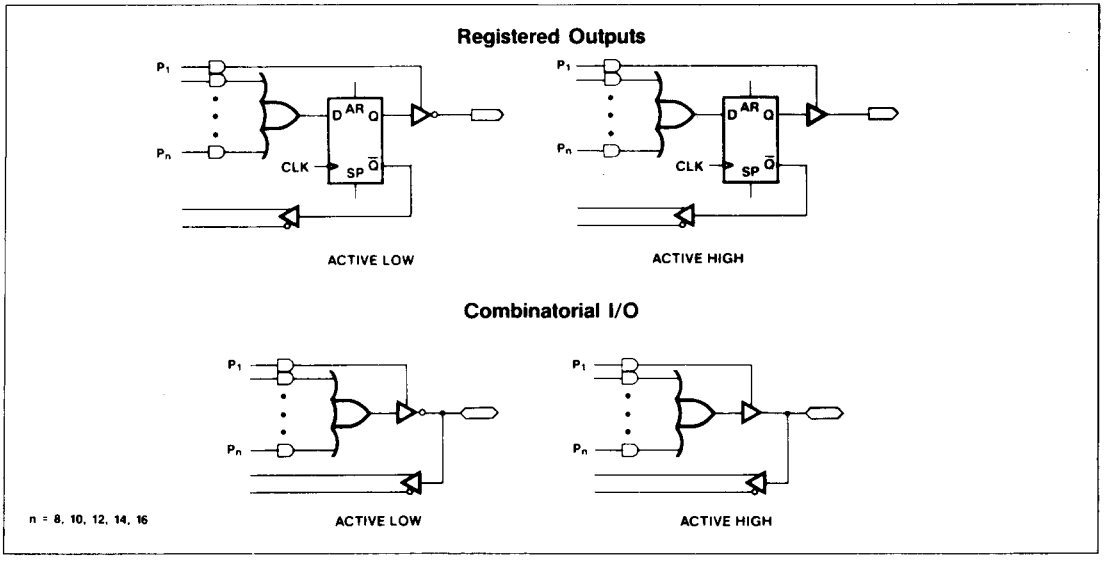
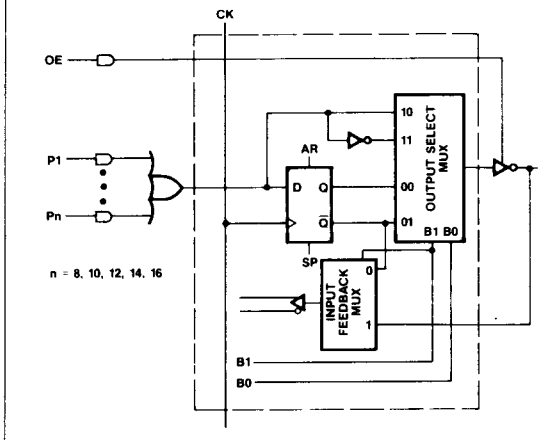


Figure 3. Output Macrocell with Configuration Bits



B_1	B_0	Output Macrocell Configuration
0	0	Registered/Active Low Output
0	1	Registered/Active High Output
1	0	Combinatorial/Active Low Output
1	1	Combinatorial/Active High Output

PROGRAMMABLE PRESET/RESET CONTROL

The final two product terms in the CPL22V10 device are used for RESET and PRESET control operations, and are shared among all ten output macrocell registers for easy system initialization. These product terms can be implemented to represent any product of device inputs and output feedbacks. When the Asynchronous Reset (AR) product term is asserted, the register of each macrocell will be forced low, independent of the clock signal. When the synchronous PRESET product term (SP) is asserted, the register of each macrocell will be forced high after the low-to-high clock transition. Depending on the output polarity chosen, the actual device outputs may be low or high.

POWER-UP RESET

During system power-up, each register in the CPL22V10 will be reset to a logic low, to ensure predictable system initialization. Actual output states, however, will be low or high, depending on the polarity chosen at each output. For reliable resets, the V_{CC} rise must be monotonic and the clock input must not change for 1μs.

SECURITY BIT

To prevent a proprietary CPL22V10 design from being copied without authorization, a security bit has been provided. The security bit is programmed via the designer's logic programmer. Once this is done, the read, verify, and preload operations are disabled, which completely secures the device. Also, since the CPL22V10 does not have visible fuses, enhanced security is offered over what is available on bipolar 22V10s.

TEST FEATURES

Register Preload

To ease functional testing, the CPL22V10 device is equipped with a register preload feature that allows an arbitrary state value to be loaded into any or all of its registers from the output pins. This makes it possible to check and verify any logical state transition, without having to run through an entire test vector sequence. Also, by using register preload, all possible states can be tested to guarantee proper in-system operation.

Test Array

Another feature of the CPL22V10 is the on-chip test array which increases device reliability by allowing each product term to be tested. The test array is programmed by Samsung to verify final functional and AC yields of the packaged device before shipping. When using the test array to test the device (even if the security bit has been programmed), only the input terms in the shaded portion of the functional block diagram are accessed. During normal operation, the test arrays are not accessed. As a result, the test array facilitates simple and shortened testing.

Input Term Testing

Finally, the CPL22V10 has additional product terms, one on output 14 and the other on output 23, which are controlled by the device's input terms. These product terms allow testing of all input structures and are programmed for functional and AC testing of the packaged device, before shipping. The additional product terms are not accessed as part of the normal operation. Having both input term testing and test arrays allows Samsung to provide a packaged device of the highest quality.

ERASURE (windowed-CERDIP only)

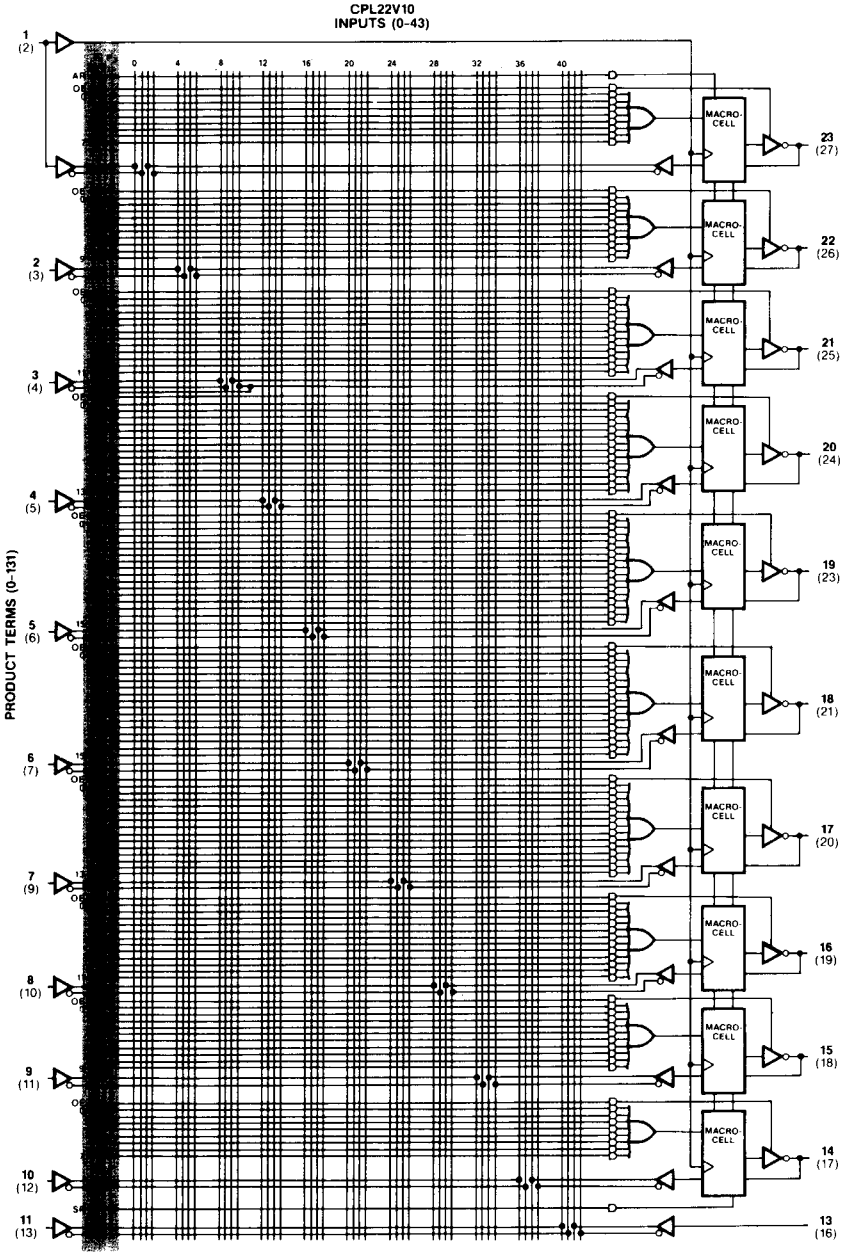
The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:

Wavelength of 2537 Angstroms
(minimum dose — 25Wsec/cm^2)

If an ultraviolet lamp with a 12mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL22V10 FUNCTIONAL LOGIC DIAGRAM
DIP AND PLCC PINOUTS



CPL22V10 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leqq 20mA$)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage	V_{PP}	14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Low Level Input Voltage	V_{IL}	(Note 4)				0.8	V
High Level Input Voltage	V_{IH}	(Note 4)			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$			-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.2mA		2.4		V
Off-State Output Leakage Current	I_{OZ}	V_{CC} = Max	$V_{SS} \leqq V_O \leqq V_{CC}$		-40	40	μA
Power Supply Current	I_{CC}	V_{IN} = GND, I_{OUT} = 0mA	V_{CC} = MAX	"L" STD		55 90	mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

Capacitance

Parameter	Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz		8	

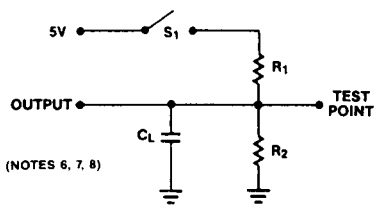
CPL22V10 AC Electrical Characteristics

Over Recommended Operating Conditions (Note 5)

Parameter	Symbol	-25		-35		Unit
		Min	Max	Min	Max	
Input or Feedback to Non-Registered Output	t_{PD} (Note 8)		25		35	ns
Clock to Registered Output or Feedback	t_{CO}		15		25	ns
Input to Output Enabled	t_{PZX}		25		35	ns
Input to Output Disabled	t_{PXZ}		25		35	ns
Setup Time from Input Feedback, or SP to Clock	t_{SU}	15		30		ns
Hold Time	t_H	0		0		ns
Clock Pulse Width (High or Low)	t_W	15		25		ns
Clock Period (t_{SU} + t_{CO})	t_P	30		55		ns
Maximum Frequency	f_{MAX}	33.3		18		MHz
Asynchronous Reset to Registered Output	t_{RO}		25		35	ns
Asynchronous Reset Pulse Width	t_{AW}	25		35		ns
Asynchronous Reset Recovery Time	t_{AR}	25		35		ns
Synchronous Preset Recovery Time	t_{SR}	25		35		ns

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6ns$

AC Test Circuit



Resistor Values (Ω)

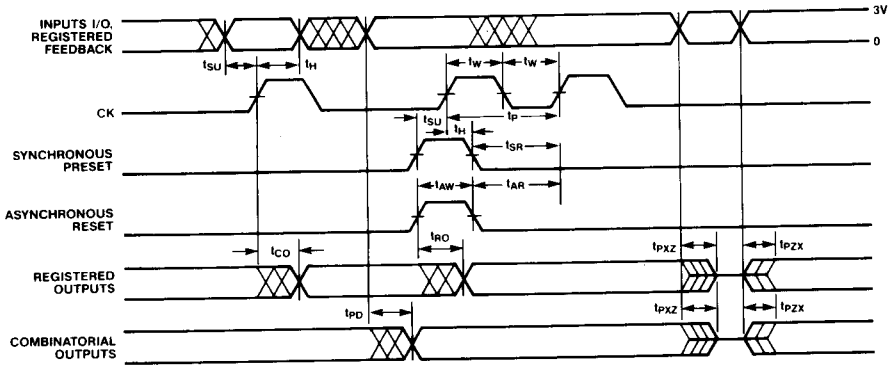
R1	R2
238	170

Note 6: C_L includes load and test jig capacitance.

Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

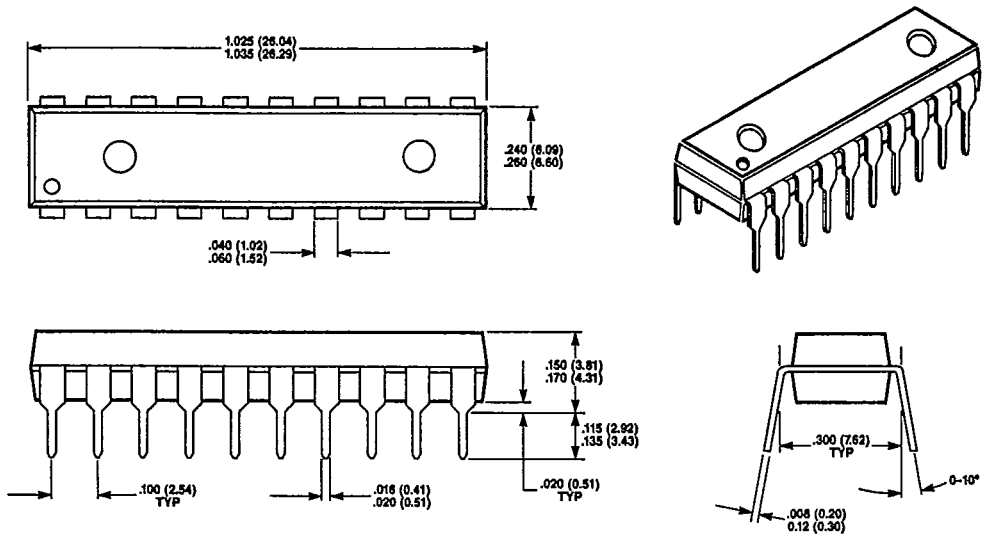
Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

Switching Waveforms



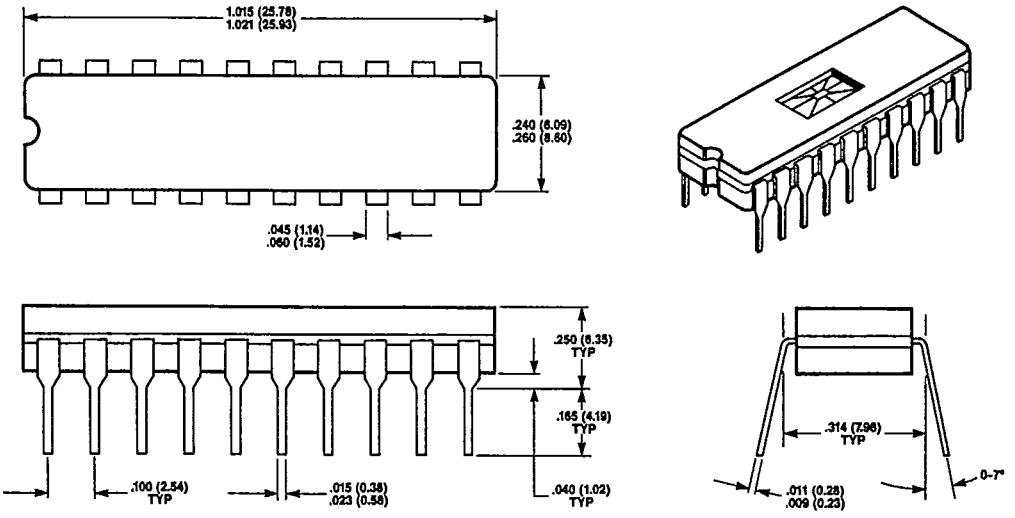
T-90-20

20 PIN PLASTIC DIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

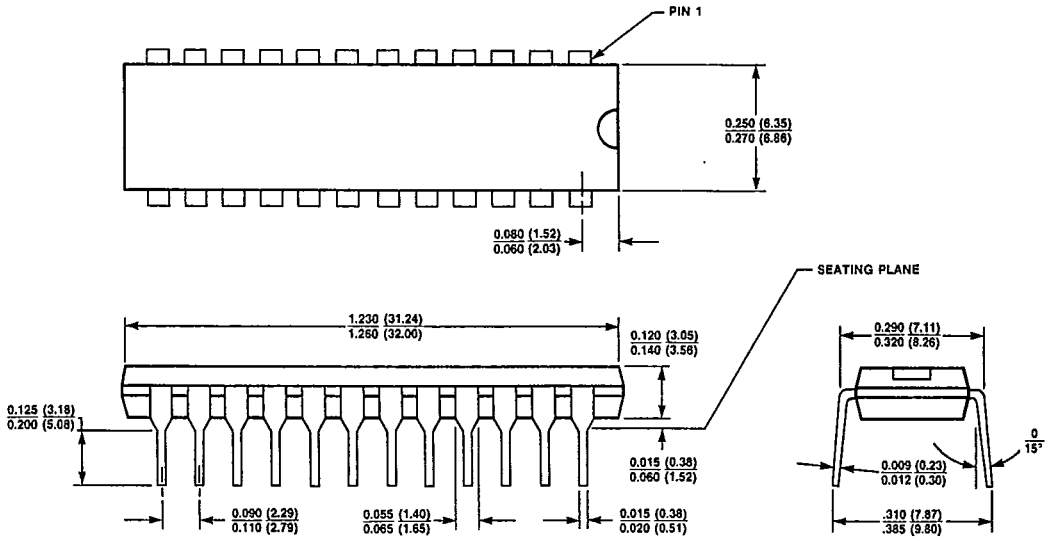
20 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

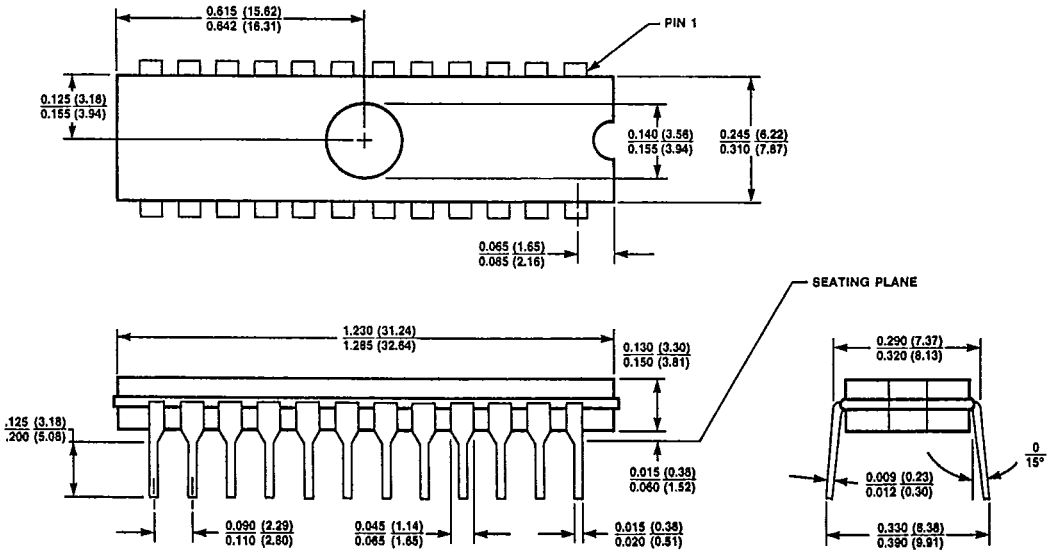
7

24 PIN PLASTIC DIP



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

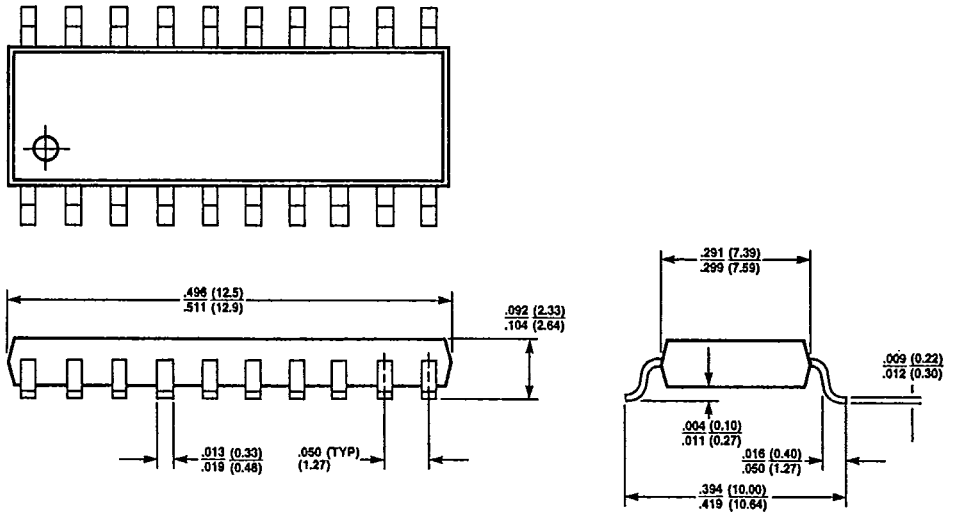
24 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

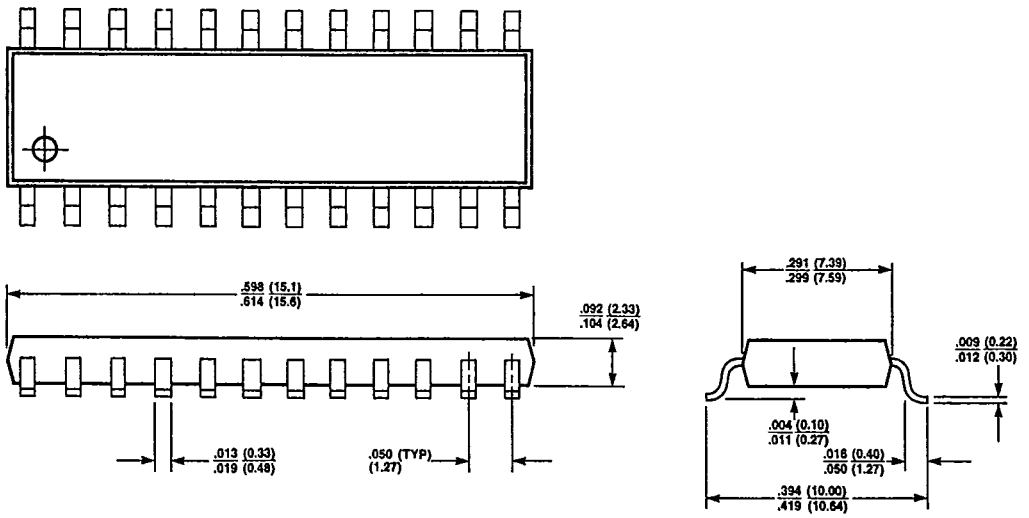
T-90-20

20 PIN SOIC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

24 PIN SOIC

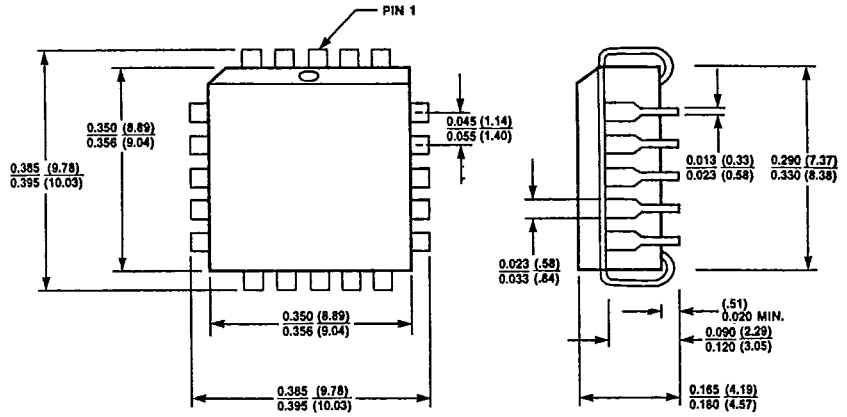


DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

7

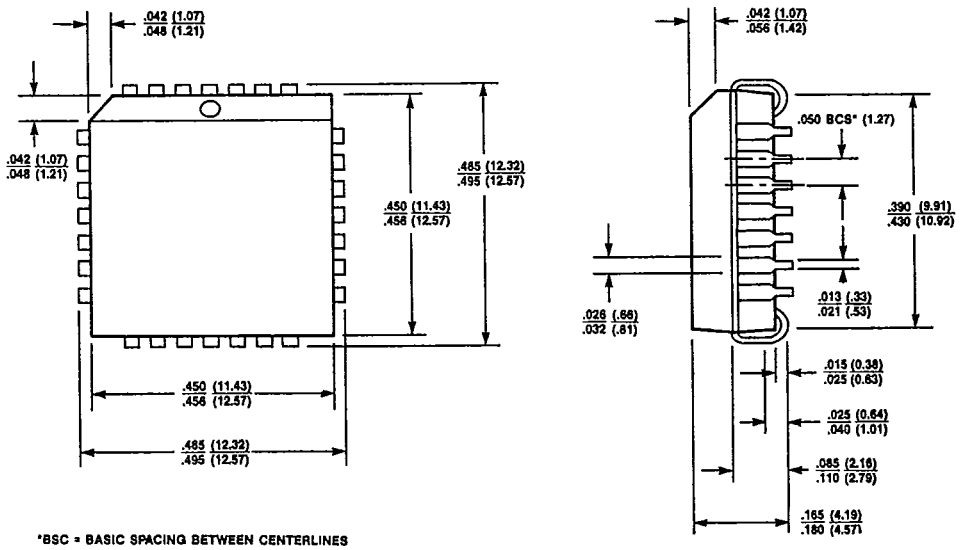
T-90-20

20 PIN PLCC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

28 PIN PLCC



*BSC = BASIC SPACING BETWEEN CENTERLINES

DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.