SONY

CXK5V8257BTM/BYM/BM -70LLX/85LLX*/10LLX**

* Only TSOP available
** Only SOP available

32768-word × 8-bit High Speed CMOS Static RAM

Description

The CXK5V8257BTM/BYM/BM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits.

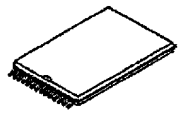
A polysilicon TFT cell technology realized extremely low standby current and higher data retention stability.

Operating on a single 3.3 V supply.

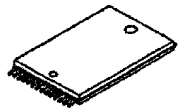
And special feature are, low power consumption and high speed.

The CXK5V8257BTM/BYM/BM is a suitable RAM for portable equipment with battery back up.

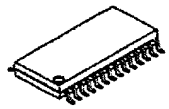
CXK5V8257BTM
28 pin TSOP (Plastic)



CXK5V8257BYM
28 pin TSOP (Plastic)



CXK5V8257BM
28 pin SOP (Plastic)



Features

- Extended operating temperature range: −25 to 85 °C
- Single +3.3 V supply: 3.3 V±0.3 V.
- Fast access time:

CXK5V8257BTM/BYM/BM	(Access time)	
−70LLX	70 ns	(Max.)
−85LLX	85 ns	(Max.)
−10LLX	100 ns	(Max.)

- Low Standby Current: 7.0 µA (Max.)
- Low Voltage Data retention: 2. 0V (Min.)
- Available in many packages

  CXK5V8257BTM/BYM

  8mm × 13.4mm 28 pin TSOP Package

  CXK5V8257BM

  450mil 28 pin SOP Package

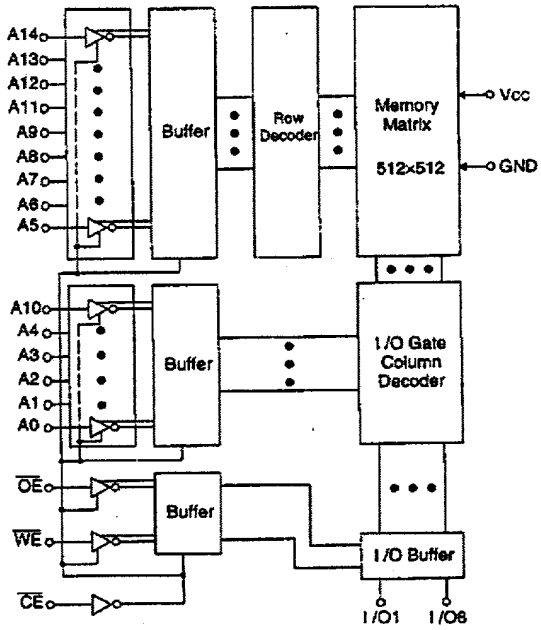
Function

32768-word × 8 bit static RAM

Structure

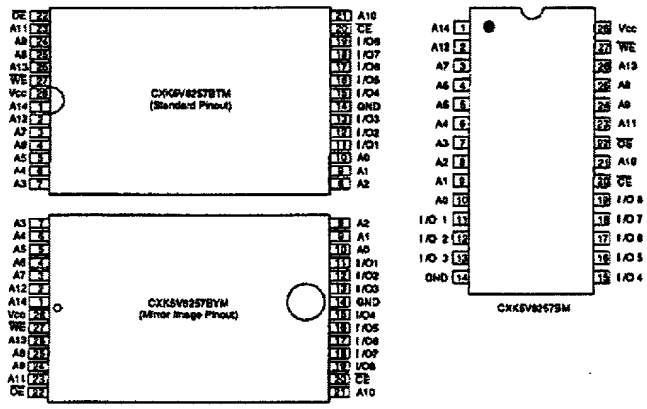
Silicon gate CMOS IC

Block Diagram



E94508-TE

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+3.3V power supply
GND	Ground

Absolute Maximum Ratings (Ta=25 °C, GND=0 V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 to +4.6	V
Input voltage	V_{IN}	−0.5* to Vcc+0.5	
Input and output voltage	$V_{I/O}$	−0.5* to Vcc+0.5	
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	−25 to +85	°C
Storage temperature	Tstg	−55 to +150	
Soldering temperature • time	Tsolder	235 • 10	°C • s

*V_{IN}, $V_{I/O}$=−3.0 V Min. for pulse width less than 50 ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	×	L	Write	Data in	I_{CC1}, I_{CC2}

×: "H" or "L"

DC Recommended Operation Conditions (Ta=−25 to +85 °C, GND=0 V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.2	—	Vcc+0.3	
Input low voltage	V_{IL}	−0.3*	—	0.6	

*V_{IL}=−3.0 V Min. for pulse width less than 50 ns.

Electrical Characteristics

• DC characteristics (Vcc=3.3 V±0.3 V, GND=0 V, Ta=–25 to 85 °C)

Item	Symbol	Test Conditions		Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		–0.5	—	0.5	µA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to Vcc		–0.5	—	0.5	µA
Operating power supply current	I_{CC1}	$\overline{CE}$=V_{IL} V_{IN}=V_{IH} or V_{IL} I_{OUT}=0 mA		—	0.9	2	mA
Average operating current	I_{CC2}	Min. cycle duty=100 % I_{OUT}=0 mA	70LLX/85LLX	—	21	40	mA
			10LLX	—	18	35	
Standby current	I_{SB1}	$\overline{CE}$≥Vcc–0.2V	–25 to +85 °C	—	—	7.0	µA
			–25 to +70 °C	—	—	3.5	
			–25 to +40 °C	—	—	0.7	
			+25 °C	—	0.12	0.35	
	I_{SB2}	$\overline{CE}$=V_{IH}		—	0.06	0.7	mA
Output high voltage	V_{OH}	I_{OH}=–2 mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.0 mA		—	—	0.4	V

* Vcc=3.3 V, Ta=25 °C

I/O Capacitance

(Ta=25 °C, f=1 MHz)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0 V	—	—	8	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0 V	—	—	10	pF

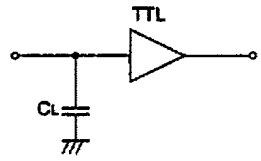
Note) This parameter is sampled and is not 100 % tested.

AC Characteristics

• AC test conditions (Vcc=3.3 V±0.3 V, Ta=–25 to +85 °C)

Item		Conditions
Input pulse high level		V_{IH}=2.2 V
Input pulse low level		V_{IL}=0.6 V
Input rise time		tr=5 ns
Input fall time		tf=5 ns
Input and output reference level		1.4 V
Output load conditions	–70LLX/85LLX	C_L*=30pF, 1TTL
	–10LLX	C_L*=100pF, 1TTL

• Test circuit



* C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE}$="H")

Item	Symbol	-70LLX		-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	100	—	ns
Address access time	t_{AA}	—	70	—	85	—	100	
Chip enable access time ($\overline{CE}$)	t_{CO}	—	70	—	85	—	100	
Output enable to output valid	t_{OE}	—	40	—	50	—	50	
Output hold from address change	t_{OH}	20	—	20	—	20	—	
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	10	—	10	—	
Chip disable to output in high Z ($\overline{CE}$)	t_{HZ}*	—	30	—	35	—	35	
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	30	—	35	—	35	

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

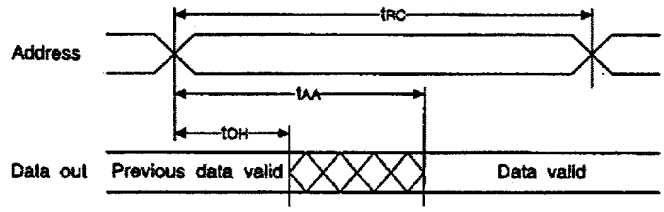
• Write cycle

Item	Symbol	-70LLX		-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	100	—	ns
Address valid to end of write	t_{AW}	60	—	80	—	80	—	
Chip enable to end of write	t_{CW}	60	—	80	—	80	—	
Data to write time overlap	t_{DW}	30	—	35	—	35	—	
Data hold from write time	t_{DH}	0	—	0	—	0	—	
Write pulse width	t_{WP}	55	—	60	—	60	—	
Address setup time	t_{AS}	0	—	0	—	0	—	
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	
Write recovery time ($\overline{CE}$)	t_{WR1}	0	—	0	—	0	—	
Output active from end of write	t_{OW}	10	—	10	—	10	—	
Write to output in high Z	t_{WHZ}*	—	30	—	35	—	35	

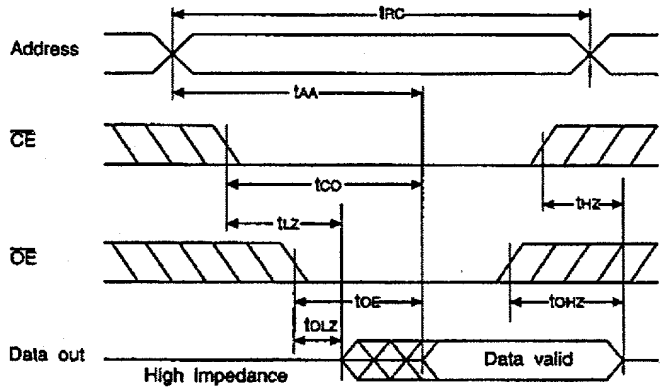
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

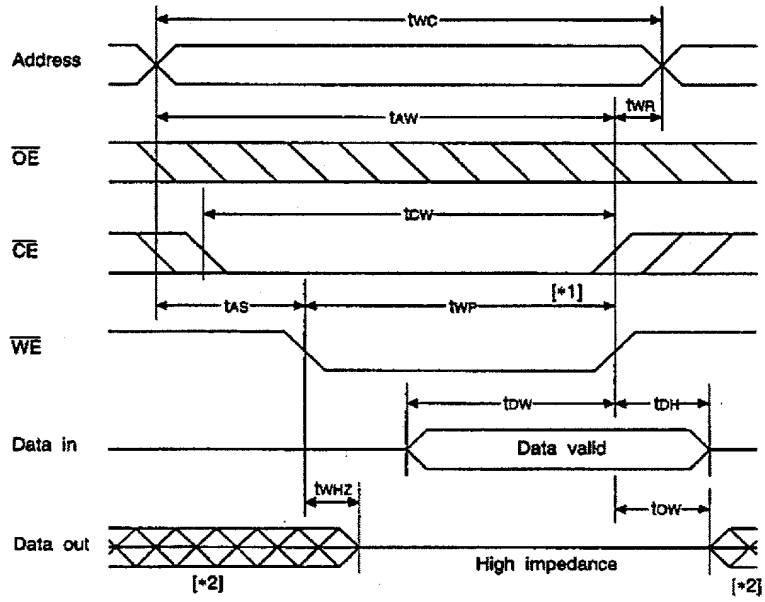
• Read cycle (1): $\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}



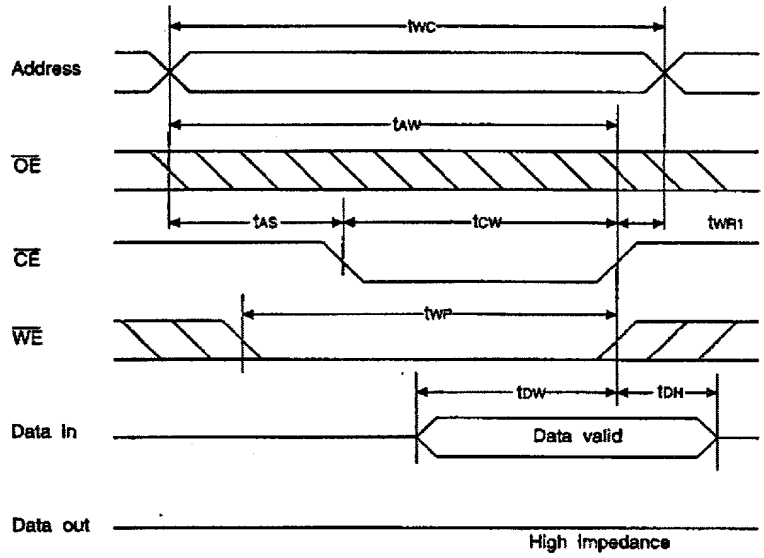
• Read cycle (2): $\overline{WE}$=V_{IH}



• Write cycle (1): $\overline{WE}$ control



• Write cycle (2): CE control



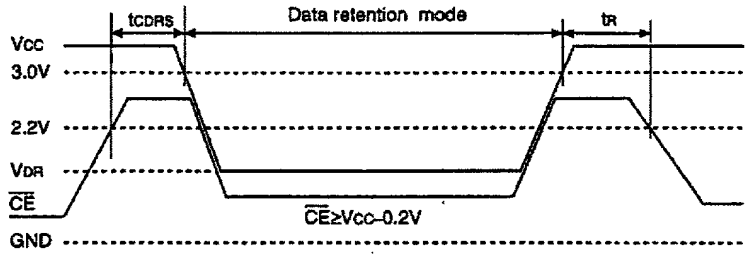
Note)

*1 Write is executed when both $\overline{CE}$ and $\overline{WE}$ are at low simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

Data Retention Waveform

• Low supply voltage data retention waveform



Data Retention Characteristics (Ta=–25 to 85 °C)

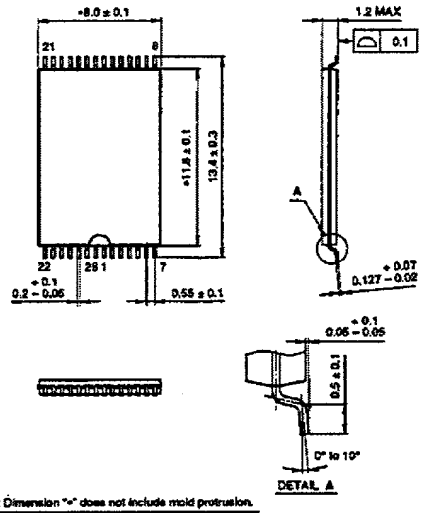
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	$\overline{CE}$≥Vcc –0.2 V		2	—	3.6	V
Data retention current	I_{CCDR1}	Vcc=3.0 V $\overline{CE}$≥2.8 V	–25 to +85 °C	—	—	6	µA
			–25 to +70 °C	—	—	3	
			–25 to +40 °C	—	—	0.6	
			+25 °C	—	0.1	0.3	
	I_{CCDR2}	Vcc=2.0 to 3.6 V $\overline{CE}$≥Vcc –0.2 V		—	0.12*	7.0	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			5	—	—	ms

*Vcc=3.3 V, Ta=25 °C

Package Outline Unit : mm

CXK5V8257BTM

28PIN TSOP (Plastic)



NOTE: Dimension "*" does not include mold protrusion.

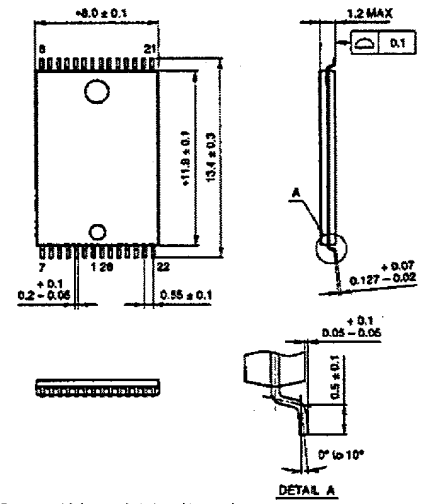
SONY CODE	TSOP-28P-L01
EIAJ CODE	TSOP028-P-0000-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

CXK5V8257BYM

28PIN TSOP (Plastic)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	TSOP-28P-L01R
EIAJ CODE	TSOP028-P-0000-B
JEDEC CODE	————

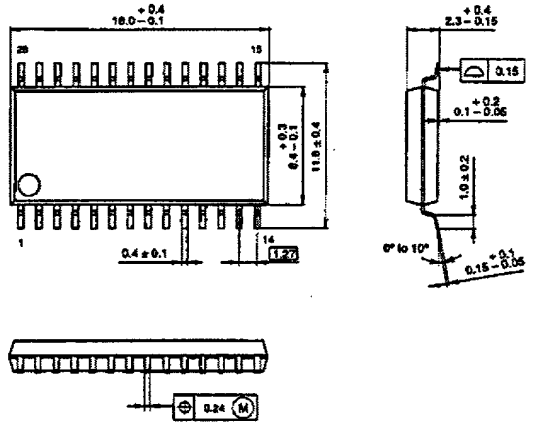
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.2g

Package Outline Unit : mm

CXK5V8257BM

28PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-28P-L35
EIAJ CODE	*SOP028-P-0450
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g