



PRELIMINARY

CYM74A590
CYM74S590
CYM74S591

VLSI 82C590 Chip Set Level II Cache Module Family

Features

- Pin-compatible secondary cache module family
- Asynchronous (CYM74A590) or synchronous (CYM74S590, CYM74S591) configurations with presence and configuration detect pins
- Ideal for Intel P54C-based systems with the VLSI 82C590 chip set
- Operates at 60 and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V inputs/outputs

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the VLSI 82C590 chip set.

CYM74A590 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution for CPU bus speeds up to 66 MHz. The CYM74A590 is organized as 32K by 64.

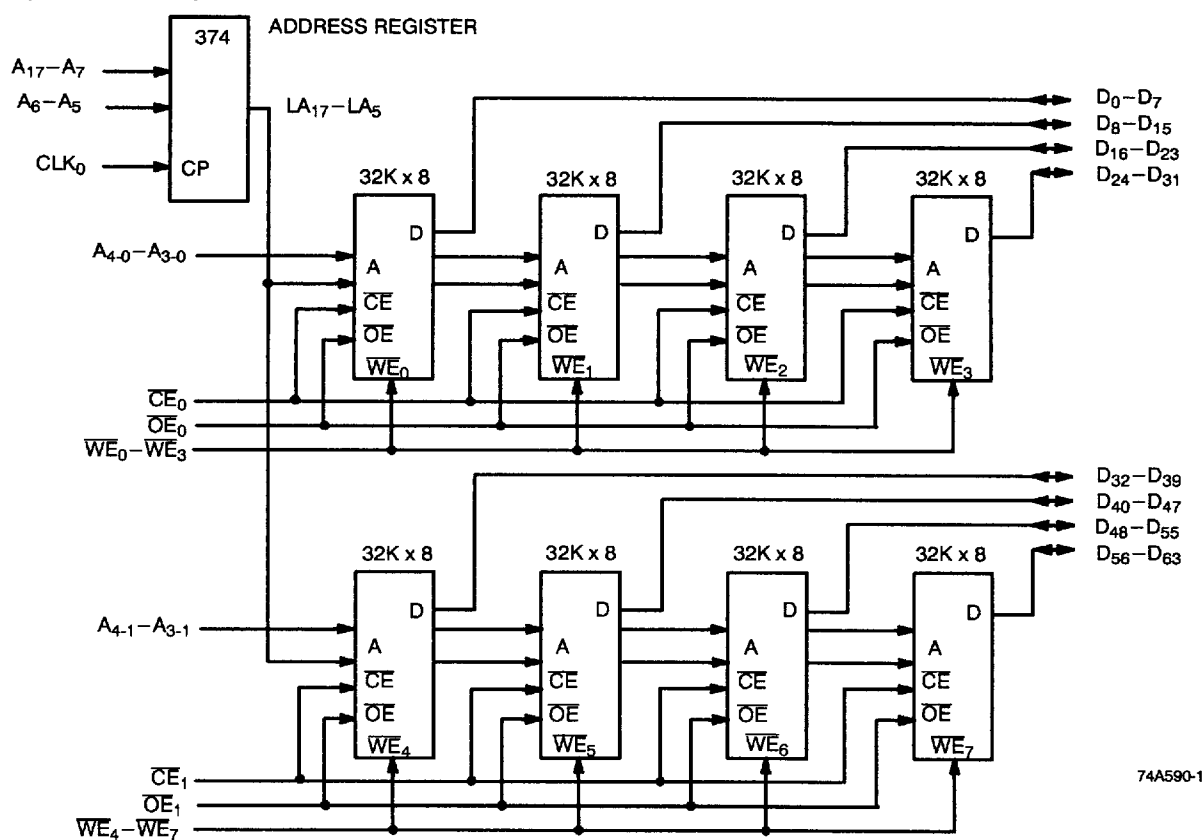
The CYM74S590 and CYM74S591 are synchronous cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74S590 is a 256-Kbyte cache module with byte parity.

The CYM74S591 is a 512-Kbyte cache module with byte parity.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

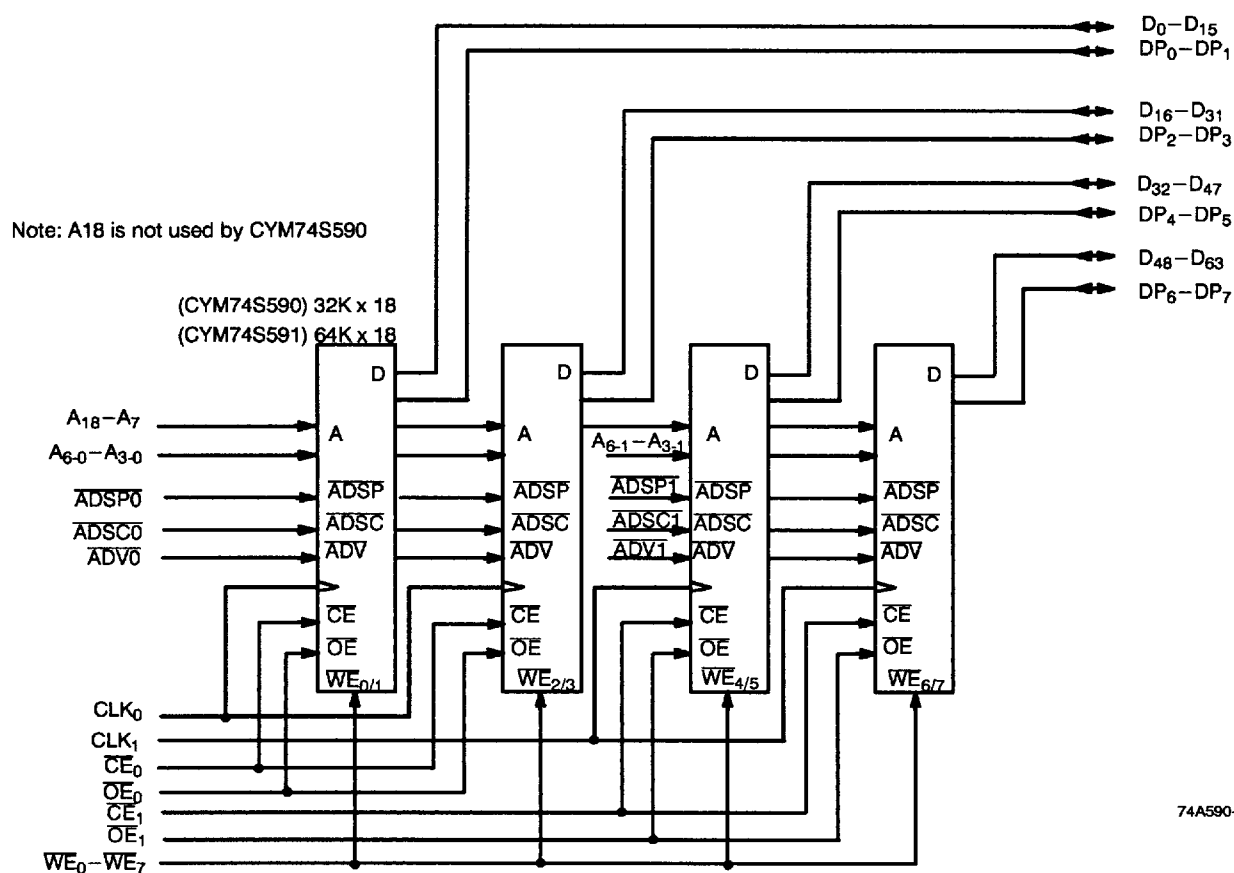
All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V-only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram – CYM74A590



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Logic Block Diagram – CYM74S590/CYM74S591



Selection Guide

	74A590-60	74A590-66	74S590-60	74S590-66	74S591-60	74S591-66
Cache Size (KB)	256	256	256	256	512	512
System Clock (MHz)	60	66	60	66	60	66
RAM Clock	Asynchronous	Asynchronous	Synchronous	Synchronous	Synchronous	Synchronous
RAM Speed	$t_{AA}=15\text{ ns}$	$t_{AA}=15\text{ ns}$	$t_{CDV}=10.5\text{ ns}$	$t_{CDV}=8.5\text{ ns}$	$t_{CDV}=10.5\text{ ns}$	$t_{CDV}=8.5\text{ ns}$

Pin Configuration
Dual Read-Out SIMM (DIMM)
Top View

GND	81	1	GND
D ₆₃	82	2	D ₆₂
V _{CC}	83	3	V _{CCQ}
D ₆₁	84	4	D ₆₀
V _{CC}	85	5	V _{CCQ}
D ₅₉	86	6	D ₅₈
D ₅₇	87	7	D ₅₆
GND	88	8	GND
DP ₇ (74S59X) / NC (74A590)	89	9	NC (74A590) / DP ₆ (74S59X)
D ₅₅	90	10	D ₅₄
D ₅₃	91	11	D ₅₂
D ₅₁	92	12	D ₅₀
GND	93	13	GND
D ₄₉	94	14	D ₄₈
D ₄₇	95	15	D ₄₆
D ₄₅	96	16	D ₄₄
D ₄₃	97	17	D ₄₂
GND	98	18	GND
D ₄₁	99	19	D ₄₀
DP ₅ (74S59X) / NC (74A590)	100	20	NC (74A590) / DP ₄ (74S59X)
D ₃₉	101	21	D ₃₈
D ₃₇	102	22	D ₃₆
D ₃₅	103	23	D ₃₄
GND	104	24	GND
D ₃₃	105	25	D ₃₂
D ₃₁	106	26	D ₃₀
D ₂₉	107	27	D ₂₈
D ₂₇	108	28	D ₂₆
D ₂₅	109	29	D ₂₄
GND	110	30	GND
DP ₃ (74S59X) / NC (74A590)	111	31	NC (74A590) / DP ₂ (74S59X)
D ₂₃	112	32	D ₂₂
D ₂₁	113	33	D ₂₀
V _{CC}	114	34	V _{CCQ}
D ₁₉	115	35	D ₁₈
GND	116	36	GND
D ₁₇	117	37	D ₁₆
V _{CC}	118	38	V _{CCQ}
D ₁₅	119	39	D ₁₄
D ₁₃	120	40	D ₁₂
GND	121	41	GND
D ₁₁	122	42	D ₁₀
V _{CC}	123	43	V _{CCQ}
D ₉	124	44	D ₈
DP ₁ (74S59X) / NC (74A590)	125	45	NC (74A590) / DP ₀ (74S59X)
V _{CC}	126	46	V _{CCQ}
D ₇	127	47	D ₆
D ₅	128	48	D ₄
D ₃	129	49	D ₂
D ₁	130	50	D ₀
GND	131	51	GND
A ₃₋₁ (74S59X) / NC (74A590)	132	52	NC (74A590) / A ₃₋₀ (74S59X)
A ₄₋₁ (74S59X) / NC (74A590)	133	53	NC (74A590) / A ₄₋₀ (74S59X)
A ₅₋₁ (74S59X) / NC (74A590)	134	54	A ₅ (74A590) / A ₅₋₀ (74S59X)
A ₆₋₁ (74S59X) / NC (74A590)	135	55	A ₆ (74A590) / A ₆₋₀ (74S59X)
A ₇	136	56	A ₈
GND	137	57	GND
A ₉	138	58	A ₁₀
A ₁₁	139	59	A ₁₂
A ₁₃	140	60	A ₁₄
A ₁₅	141	61	A ₁₆
A ₁₇	142	62	A ₁₈
GND	143	63	GND
(Reserved A ₁₉) NC	144	64	PD ₀
PD ₁	145	65	PD ₂
CLK ₀	146	66	NC (74A590) / CLK ₁ (74S59X)
(Reserved CLK ₂) NC	147	67	NC (Reserved CLK ₃)
GND	148	68	GND
WE ₇	149	69	WE ₆
WE ₅	150	70	WE ₄
WE ₃	151	71	WE ₂
WE ₁	152	72	WE ₀
GND	153	73	GND
ADSC ₁ (74S59X) / A ₃₋₁ (74A590)	154	74	A ₃₋₀ (74A590) / ADSC ₀ (74S59X)
CE ₁	155	75	CE ₀
ADV ₁ (74S59X) / A ₄₋₁ (74A590)	156	76	A ₄₋₀ (74A590) / ADV ₀ (74S59X)
OE ₁	157	77	OE ₀
V _{CC}	158	78	V _{CCQ}
ADSP ₁ (74S59X) / NC (74A590)	159	79	NC (74A590) / ADSP ₀ (74S59X)
GND	160	80	GND

74A590-3

Pin Definitions

Signal Name	Description
V _{CC}	5V Supply
V _{CCQ}	3.3V Supply
GND	Ground
A ₇ –A ₁₉	Addresses from processor
A ₃ – ₀ , A ₄ – ₀ , A ₅ – ₀ , A ₆ – ₀	Lower address from chip set for bank0, identical to the bank1 addresses
A ₃ – ₁ , A ₄ – ₁ , A ₅ – ₁ , A ₆ – ₁	Lower address from chip set for bank1, identical to the bank0 addresses
$\overline{CE}_0$, $\overline{CE}_1$	Chip Enable (same signal)
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable (same signal)
$\overline{WE}_0$, $\overline{WE}_1$, $\overline{WE}_2$, $\overline{WE}_3$ $\overline{WE}_4$, $\overline{WE}_5$, $\overline{WE}_6$, $\overline{WE}_7$	Byte Write Enables
CALE	Latch Enable – CYM74A590 only
PD ₀ –PD ₂	Presence Detect pins
D ₀ –D ₆₃	Data lines from processor
DP ₀ –DP ₇	Data Parity lines (Optional), CYM74S590 or CYM74S591 only
$\overline{ADSP}_0$, $\overline{ADSP}_1$	Processor Address Strobe, CYM74S590 or CYM74S591 only
$\overline{ADSC}_0$, $\overline{ADSC}_1$	Cache Controller Address Strobe, CYM74S590 or CYM74S591 only
$\overline{ADV}_0$, $\overline{ADV}_1$	Burst Address Advance – CYM74S590 or CYM74S591 only
CLK ₀ , CLK ₁ , CLK ₂ , CLK ₃	Clock signals
NC	Signal not connected on module.

Presence Detect Pins

	PD ₂	PD ₁	PD ₀
Asynchronous – CYM74A590	NC	GND	NC
Synchronous – CYM74S590	GND	GND	NC
Synchronous – CYM74S591	GND	GND	GND

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to $+125^{\circ}\text{C}$

Ambient Temperature

with Power Applied -0°C to $+70^{\circ}\text{C}$

3.3V Supply Voltage to Ground Potential -0.5V to $+4.6\text{V}$

5V Supply Voltage to Ground Potential -0.5V to $+5.25\text{V}$

DC Voltage Applied to Outputs

in High Z State -0.5V to $+4.6\text{V}$

DC Input Voltage -0.5V to $+4.6\text{V}$

Output Current into Outputs (LOW) 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 5\%$ $3.3\text{V} \pm 5\%$

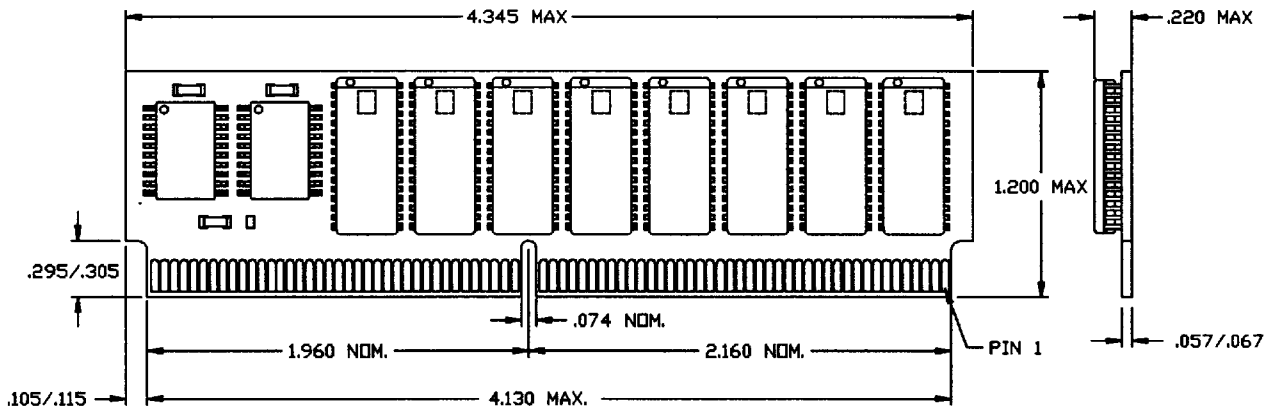
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage		2.2	V _{CCQ} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} =Min. I _{OH} = -4 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} =Min. I _{OL} = 8 mA		0.4	V
I _{CC} (74A590)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA
I _{CC} (74S590)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA
I _{CC} (74S591)	V _{CC} Operating Supply Current	V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC}		1500	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM74A590PM-60C	PM25	160-Pin Dual-Readout SIMM	Asynchronous 256 KB	Commercial
	CYM74S590PM-60C	PM26	160-Pin Dual-Readout SIMM	Synchronous 256 KB	
	CYM74S591PM-60C	PM26	160-Pin Dual-Readout SIMM	Synchronous 512 KB	
66	CYM74A590PM-66C	PM25	160-Pin Dual-Readout SIMM	Asynchronous 256 KB	Commercial
	CYM74S590PM-66C	PM26	160-Pin Dual-Readout SIMM	Synchronous 256 KB	
	CYM74S591PM-66C	PM26	160-Pin Dual-Readout SIMM	Synchronous 512 KB	

Document #: 38-M-00075

Package Diagrams
160-Pin Dual-Readout SIMM PM25

160-Pin Dual-Readout SIMM PM26
