Lattice

GAL20RA10/883

High-Speed Asynchronous E²CMOS PLD Generic Array Logic™

T-46-19-07

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - 20 ns Maximum Propagation Delay
  - Fmax = 41.7 MHz
  - 20 ns Maximum from Clock Input to Data Output
  - TTL Compatible 8 mA Outputs
  - UltraMOS® Advanced CMOS Technology
- **50% REDUCTION IN POWER FROM BIPOLAR**
  - 75mA Typ Icc
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<100 ms)
  - 20 Year Data Retention
- **TEN OUTPUT LOGIC MACROCELLS**
  - Independent Programmable Clocks
  - Independent Asynchronous Reset and Preset
  - Registered or Combinatorial with Polarity
  - Full Function and Parametric Compatibility with PAL20RA10
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
  - State Machine Control
  - Standard Logic Consolidation
  - Multiple Clock Logic Designs
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

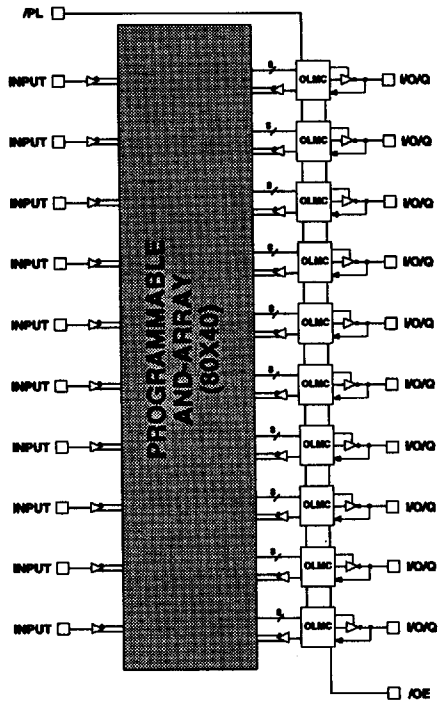
DESCRIPTION

The GAL20RA10/883 is a high performance E²CMOS programmable logic device processed in full compliance to MIL-STD-883. With a 20ns maximum propagation delay time, it is the fastest military grade 20RA10 device on the market. In addition to speed performance, Lattice's Electrically Erasable (E²) floating gate technology provides low power performance. The GAL20RA10's typical Icc of 75mA, represents a 50% savings in power when compared to bipolar counterparts. E² technology also offers high speed (<100ms) erase times providing the ability to reprogram or test the devices quickly and efficiently.

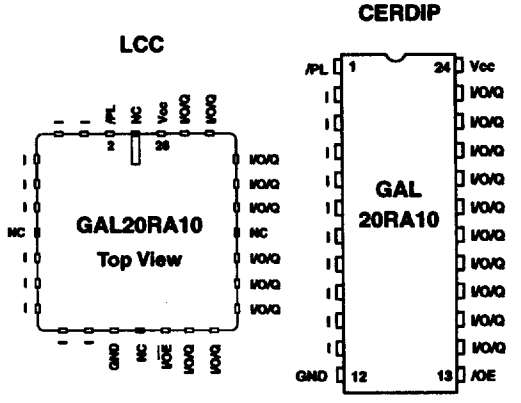
The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is a direct parametric compatible CMOS replacement for the PAL20RA10 device.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacturing. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE guarantees data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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Specifications *GAL20RA10/883*

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Case Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Military Devices:
Case Temperature (T_C) ..... -55 to +125°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.50 to +5.50V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–50	—	–135	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	—	75	120	mA

1) The leakage current is due to the internal pull-up on all pins. See the Input Buffer section in the commercial datasheet for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25 C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
C_{VO}	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

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AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-20		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinatorial Output	—	20	—	25	ns
tco	1	Clock to Output Delay	—	20	—	25	ns
tsu	—	Setup Time, Input or Feedback before Clock	10	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock	3	—	5	—	ns
fmax[2]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	33.3	—	25.0	—	MHz
	1	Maximum Clock Frequency with No Feedback	41.7	—	33.3	—	MHz
twh	—	Clock Pulse Duration, High	12	—	15	—	ns
twl	—	Clock Pulse Duration, Low	12	—	15	—	ns
ten / tdis	2,3	Input or I/O to Output Enabled / Disabled	—	20	—	25	ns
ten / tdis	2,3	$\overline{OE}$ to Output Enabled / Disabled	—	15	—	15	ns
tar / tap	1	Input or I/O to Asynchronous Reset / Preset	—	20	—	25	ns
tarw / tapw	—	Asynchronous Reset / Preset Pulse Duration	20	—	25	—	ns
tarr / tapr	—	Asynchronous Reset / Preset Recovery Time	12	—	20	—	ns
twp	—	Preload Pulse Duration	20	—	25	—	ns
tsp	—	Preload Setup Time	15	—	20	—	ns
thp	—	Preload Hold Time	15	—	20	—	ns

1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Descriptions** section.

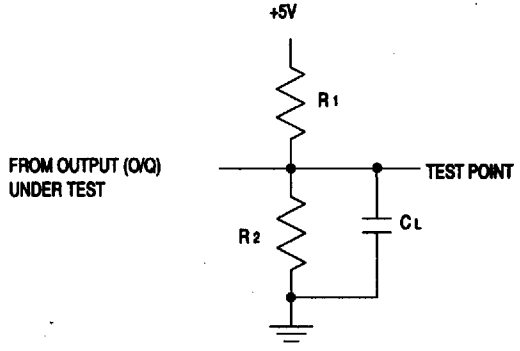
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		470Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	470Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	470Ω	390Ω	5pF



CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

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SWITCHING WAVEFORMS

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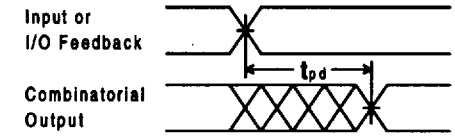
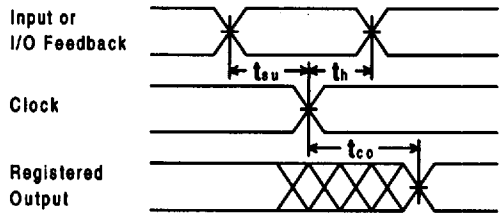
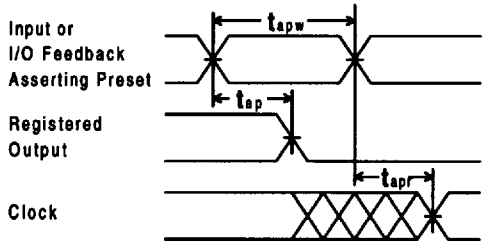


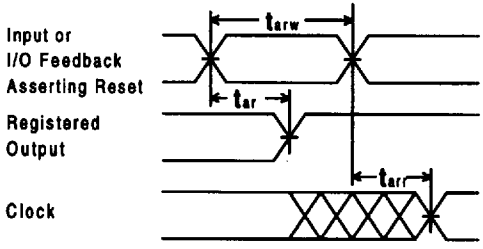
Combinatorial Output



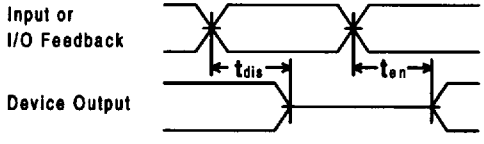
Registered Output



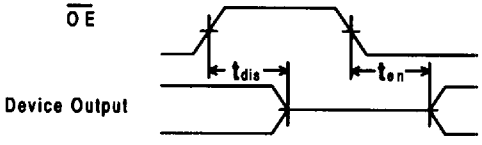
Asynchronous Preset



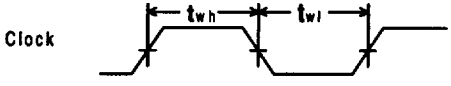
Asynchronous Reset



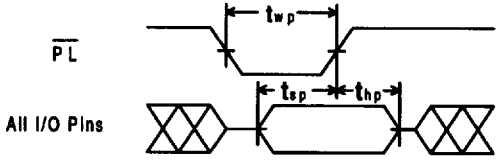
Input or I/O Feedback to Enable / Disable



OE to Enable / Disable



Clock Width



Parallel Preload

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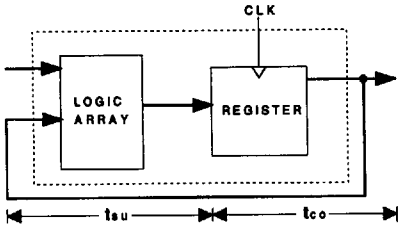
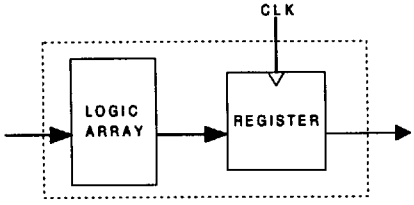
fmax DESCRIPTIONS



fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax With No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.

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GAL20RA10/883 ORDERING INFORMATION (MIL-STD-883 and SMD)

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Package	Ordering # MIL-STD-883	Ordering # SMD #
20	10	20	120	24-Pin CERDIP	GAL20RA10-20LD/883	Contact Factory
				28-Pin LCC	GAL20RA10-20LR/883	Contact Factory
25	15	25	120	24-Pin CERDIP	GAL20RA10-25LD/883	Contact Factory
				28-Pin LCC	GAL20RA10-25LR/883	Contact Factory

PART NUMBER DESCRIPTION