



Description

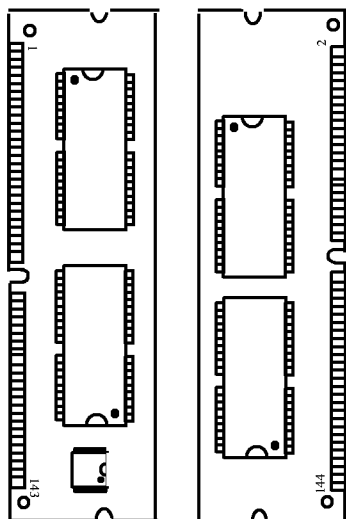
The GMM2645228CNTG is a 4M x 64 bits Synchronous Dynamic RAM SO-DIMM which is assembled 4 pieces of 4M x 16bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 144 pin printed circuit board with decoupling capacitors. The GMM2645228CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2645228CNTG provides common data inputs and outputs.

Features

- * PC100,PC66 Compatible
7K(2-2-2),7J(3-2-2),10K(PC66)
- * 3.3V +/- 0.3V Power supply
- * Maximum Clock frequency
100 / 125 MHz
- * LVTTTL Interface
- * Burst read/write operation and burst read/
single write operation capability
- * Programmable burst length ;
1, 2, 4, 8, Full page
- * Programmable burst sequence
Sequential / Interleave
- * Full Page burst length capability
Sequential burst
Burst stop capability
- * Programmable $\overline{\text{CAS}}$ Latency ; 2, 3
- * CKE power down mode
- * Input / Output data masking
- * 4096 Refresh Cycles / 64ms
- * Auto refresh / Self refresh Capability
- * Serial Presence Detect with EEPROM

GMM2645228CNTG (Both Side)



Pin Name

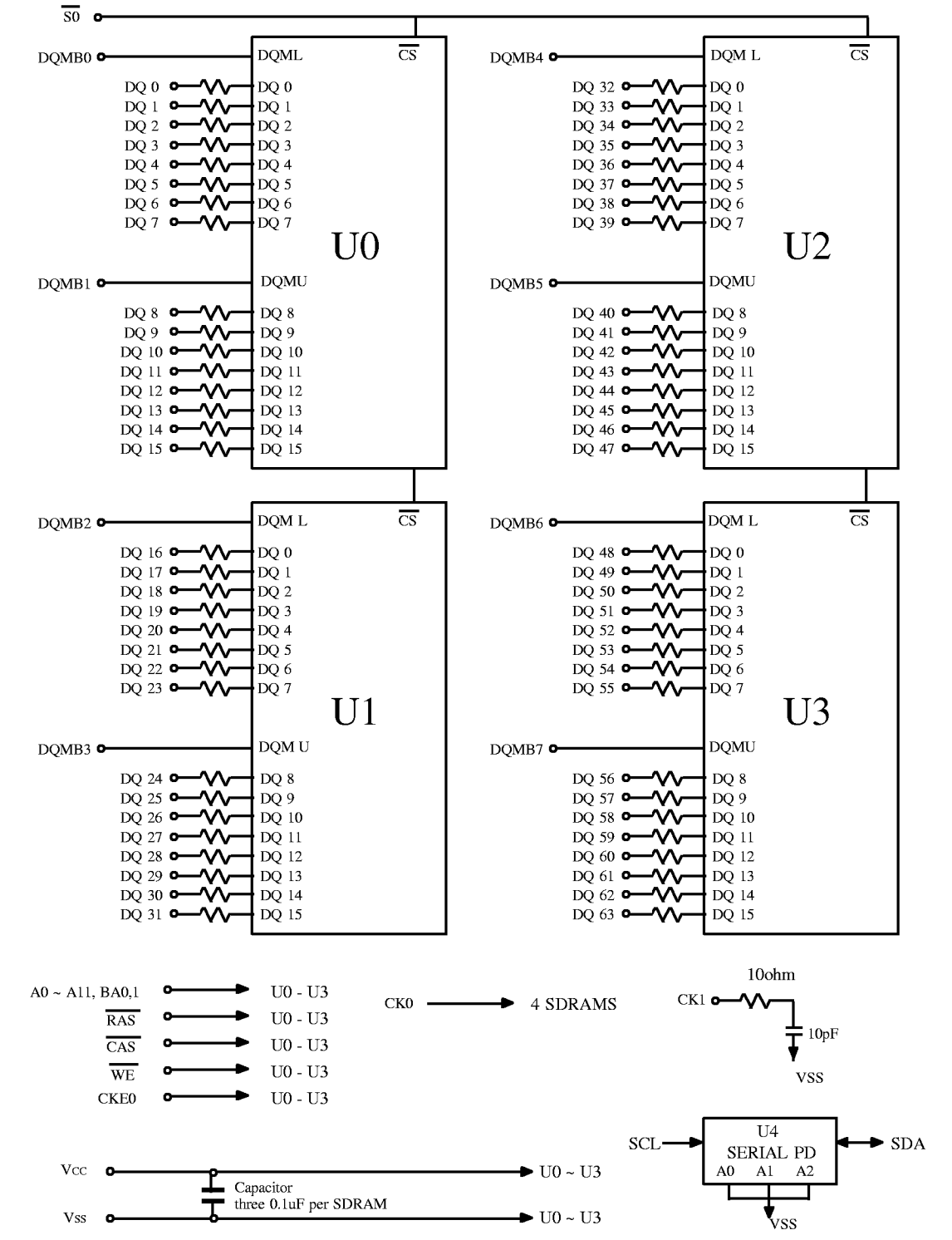
CK0,1	Clock inputs
CKE0	Clock Enable
$\overline{\text{S0}}$	Chip Select
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
A0~A11	Address input
BA0,1	Bank Address input
DQ0~63	Data input / output
DQMB0~7	Data input / output Mask
Vcc	Power for internal circuit
Vss	Ground for internal circuit
NC	No Connect
SDA	Serial Data input / output
SCL	Serial Clock
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	25	DQMB1	49	DQ13	73	DU	97	DQ22	121	DQ24
2	Vss	26	DQMB5	50	DQ45	74	CK1	98	DQ54	122	DQ56
3	DQ0	27	Vcc	51	DQ14	75	Vss	99	DQ23	123	DQ25
4	DQ32	28	Vcc	52	DQ46	76	Vss	100	DQ55	124	DQ57
5	DQ1	29	A0	53	DQ15	77	NC	101	Vcc	125	DQ26
6	DQ33	30	A3	54	DQ47	78	NC	102	Vcc	126	DQ58
7	DQ2	31	A1	55	Vss	79	NC	103	A6	127	DQ27
8	DQ34	32	A4	56	Vss	80	NC	104	A7	128	DQ59
9	DQ3	33	A2	57	NC	81	Vcc	105	A8	129	Vcc
10	DQ35	34	A5	58	NC	82	Vcc	106	BA0	130	Vcc
11	VDD	35	Vss	59	NC	83	DQ16	107	Vss	131	DQ28
12	VDD	36	Vss	60	NC	84	DQ48	108	Vss	132	DQ60
13	DQ4	37	DQ8	61	CK0	85	DQ17	109	A9	133	DQ29
14	DQ36	38	DQ40	62	CKE0	86	DQ49	110	BA1	134	DQ61
15	DQ5	39	DQ9	63	Vcc	87	DQ18	111	A10/AP	135	DQ30
16	DQ37	40	DQ41	64	Vcc	88	DQ50	112	A11	136	DQ62
17	DQ6	41	DQ10	65	$\overline{\text{RAS}}$	89	DQ19	113	Vcc	137	DQ31
18	DQ38	42	DQ42	66	$\overline{\text{CAS}}$	90	DQ51	114	Vcc	138	DQ63
19	DQ7	43	DQ11	67	$\overline{\text{WE}}$	91	Vss	115	DQMB2	139	Vss
20	DQ39	44	DQ43	68	CKE1*	92	Vss	116	DQMB6	140	Vss
21	Vss	45	Vcc	69	$\overline{\text{S0}}$	93	DQ20	117	DQMB3	141	SDA
22	Vss	46	Vcc	70	A12*	94	DQ52	118	DQMB7	142	SCL
23	DQMB0	47	DQ12	71	$\overline{\text{ST}}^*$	95	DQ21	119	Vss	143	Vcc
24	DQMB4	48	DQ44	72	A13*	96	DQ53	120	Vss	144	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0,1 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pins)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A7 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
Vcc (power supply pins)	3.3 V is applied. (Vcc is for the internal circuit)
Vss (power supply pins)	Ground is connected. (Vss is for the internal circuit)
NC	No Connection pins.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V _T	-0.5 to V _{CC} +0.5 (≤ 4.6 (max))	V	1
Supply voltage relative to Vss	V _{CC}	-0.5 to +4.6	V	1
Short circuit output current	I _{OUT}	50	mA	
Power dissipation	P _T	4.0	W	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +125	°C	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (T_a = 0 to + 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V _{CC} , V _{CCQ}	3.0	3.6	V	1
	V _{SS} , V _{SSQ}	0	0	V	
Input high voltage	V _{IH}	2.0	V _{CC} + 0.3	V	1, 2
Input low voltage	V _{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.6V for pulse width ≤ 3ns

3. V_{IL} (min) = -2.0V for pulse width ≤ 3ns

DC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	- 8	- 7K	- 7J	- 10K	Unit	Test conditions	Notes
			Max	Max	Max	Max			
Operating current		ICC1	280	280	280	250	mA	Burst length= 1 t _{RC} = min	1, 2, 3
Standby current in power down		ICC2P	6	6	6	6	mA	CKE = V _{IL} , t _{CK} = 12 ns	5
Standby current in power down (input signal stable)		ICC2PS	1.6	1.6	1.6	1.6	mA	CKE=V _{IL} , t _{CK} = infinity	6
Standby current in non power down (CAS latency=2)		ICC2N	40	40	40	40	mA	CKE,CS = V _{IL} , t _{CK} = 12ns	4
Standby current in non power down (input signal stable)		ICC2NS	16	16	16	16	mA	CKE = V _{IL} , t _{CK} = infinity	8
Active standby current in power down		ICC3P	20	20	20	20	mA	CKE = V _{IL} , t _{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		ICC3PS	16	16	16	16	mA	CKE = V _{IL} , t _{CK} = infinity	2,6
Active standby current in non power down		ICC3N	100	100	100	100	mA	CKE,CS = V _{IH} , t _{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		ICC3NS	40	40	40	40	mA	CKE = V _{IH} , t _{CK} = infinity	2,8
Burst operating current	(CL= 2)	ICC4	420	450	300	300	mA	t _{CK} = min BL = 4	1,2,3
	(CL= 3)	ICC4	550	450	450	450	mA		
Refresh current		ICC5	420	420	420	300	mA	t _{RC} = min	3
Self refresh current		ICC6	1.6	1.6	1.6	1.6	mA	V _{IH} >= V _{CC} - 0.2 V _{IL} <= 0.2V	7

DC Characteristics ($T_a = 0$ to 70°C , V_{CC} , $V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$, V_{SS} , $V_{SSQ} = 0\text{ V}$)

Parameter	Symbol	- 8, - 7K, - 7J, - 10K		Unit	Test conditions	Notes
		Min	Max			
Input leakage current	I_{LI}	-1	1	μA	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current	I_{LO}	-1.5	1.5	μA	$0 \leq V_{out} \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	V	$I_{OH} = -2\text{ mA}$	
Output low voltage	V_{OL}	-	0.4	V	$I_{OL} = 2\text{ mA}$	

Notes : 1. I_{CC} depends on output load condition when the device is selected. $I_{CC}(\text{max})$ is specified at the output open condition.

2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance ($T_a = 25^\circ\text{C}$, V_{CC} , $V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance ($A0 \sim A11, BA0,1$)	-	30	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}, \overline{CAS}, \overline{WE}$)	-	28	pF	1, 3
C_{I3}	Input capacitance ($CK0$)	-	40	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}, CKE0$)	-	32	pF	1, 3
C_{I5}	Input capacitance ($DQMB0 \sim DQMB7$)	-	12	pF	1, 3
$C_{I/O}$	Input / output capacitance ($DQ0 \sim DQ63$)	-	16	pF	1, 2, 3

- Note :
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. DQMB = V_{IH} to disable Dout.
 3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	- 8		- 7K		- 7J		- 10K		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t _{CK}	12	-	10	-	15	-	15	-	ns	1
	(CL=3)	t _{CK}	8	-	10	-	10	-	10	-		
CLK high pulse width		t _{CKH}	3	-	3	-	3	-	3	-	ns	1
CLK low pulse width		t _{CKL}	3	-	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t _{AC}	-	8	-	6	-	8	-	9	ns	1, 2
	(CL=3)	t _{AC}	-	6	-	6	-	6	-	8		
Data-out hold time		t _{OH}	3	-	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedance		t _{LZ}	2	-	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedance (CL = 2, 3)		t _{HZ}	-	6	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t _{DS}	2	-	2	-	2	-	2	-	ns	1
Data-in hold time		t _{DH}	1	-	1	-	1	-	1	-	ns	1
Address setup time		t _{AS}	2	-	2	-	2	-	2	-	ns	1
Address hold time		t _{AH}	1	-	1	-	1	-	1	-	ns	1
CKE setup time		t _{CES}	2	-	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t _{CESP}	2	-	2	-	2	-	2	-	ns	1
CKE hold time		t _{CEH}	1	-	1	-	1	-	1	-	ns	1
Command ($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM) setup time		t _{CS}	2	-	2	-	2	-	2	-	ns	1
Command ($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM) hold time		t _{CH}	1	-	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t _{RC}	72	-	70	-	70	-	90	-	ns	1
Active to Precharge command period		t _{RAS}	48	120000	50	120000	50	120000	60	120000	ns	1
Active command to column command (same bank)		t _{RCD}	24	-	20	-	20	-	30	-	ns	1
Precharge to active command period		t _{RP}	24	-	20	-	20	-	30	-	ns	1

AC Characteristics ($T_a = 0$ to 70°C , V_{CC} , $V_{CCQ} = 3.3\text{ V} \pm 0.3\text{ V}$, V_{SS} , $V_{SSQ} = 0\text{ V}$)
(Continued)

Parameter	Symbol	- 8		- 7K		- 7J		- 10K		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	8	-	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	16	-	20	-	20	-	20	-	ns	1
Refresh period	t_{REF}	-	64	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes $t_r = 1\text{ ns}$. Reference level for timing of input signals is 1.40 V .

If t_r is longer than 1 ns , transition time compensation should be considered.

2. Access time is measured at 1.40 V . Load condition is $C_L = 50\text{ pF}$ without termination.

3. $t_{LZ}(\text{min})$ defines the time at which the outputs achieves the low impedance state.

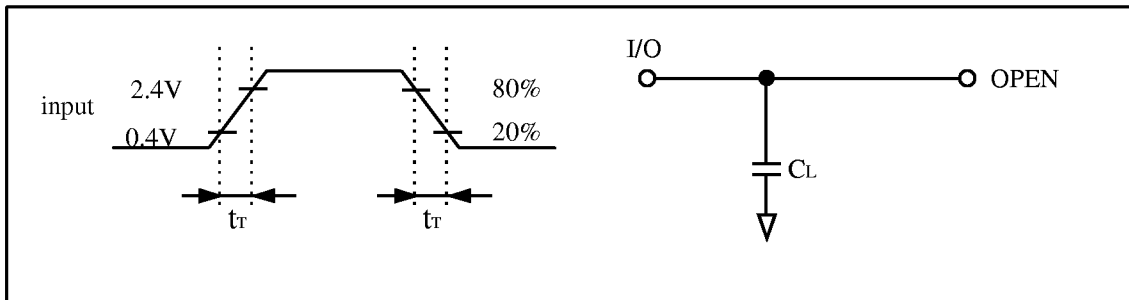
4. $t_{HZ}(\text{max})$ defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

* Input and output-timing reference levels: 1.4 V

* Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

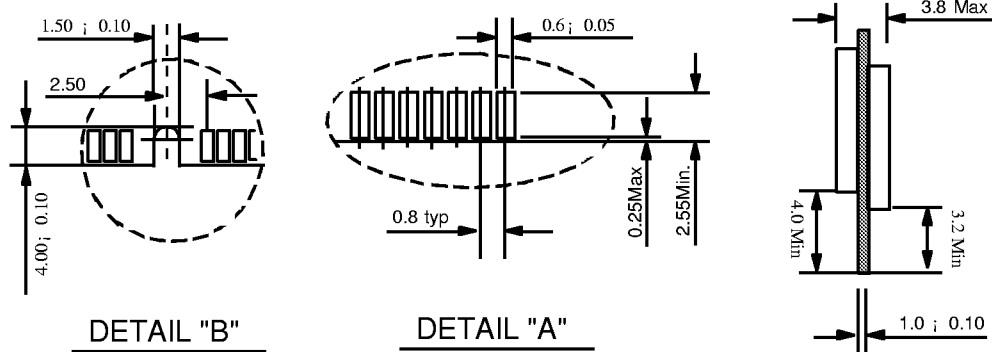
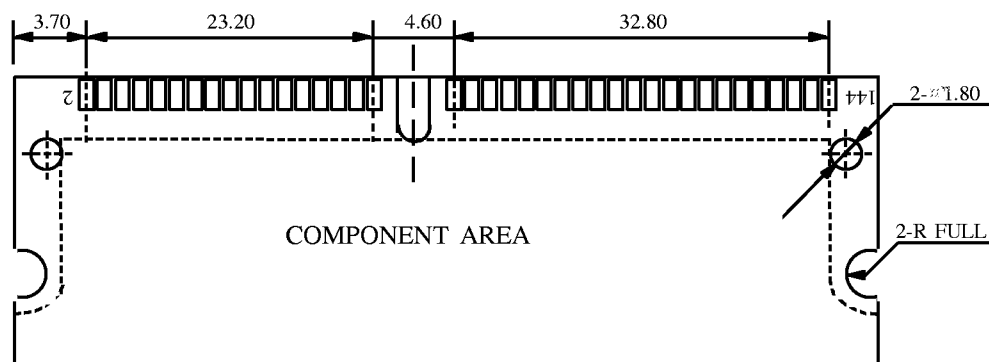
Parameter		Symbol	- 8		- 7K	- 7J		- 10K		Notes
Frequency(MHz)			125	83	100	100	66	100	66	
t _{CK} (ns)			8	12	10	10	15	10	15	
Active command to column command (same bank)		t _{RCD}	3	2	2	2	2	3	2	1
Active command to active command period (same bank)		t _{RC}	9	6	7	7	6	9	6	= [t _{RAS} + t _{RP}],
Active command to precharge command (same bank)		t _{RAS}	6	4	5	5	4	6	4	1
Precharge command to active command (same bank)		t _{RP}	3	2	2	2	2	3	2	1
Write recovery or data-in to precharge command (same bank)		t _{RWL}	1	1	1	1	1	1	1	1
Active command to active command (different bank)		t _{RRD}	2	2	2	2	2	2	2	1
Self refresh exit time		t _{SREX}	1	1	1	1	1	1	1	
Last data in to active command (Auto precharge, same bank)		t _{APW}	4	3	3	3	3	4	3	= [t _{RWL} + t _{RP}], 1
Self refresh exit to command input		t _{SEC}	9	6	7	7	6	9	6	= [t _{RC}]
Precharge command to high impedance	(CL=2)	t _{HZP}	-	2	2	-	2	-	2	
	(CL=3)	t _{HZP}	3	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)		t _{APR}	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=2)	t _{EP}	-	- 1	-1	-	- 1	-	- 1	
	(CL=3)	t _{EP}	-2	- 2	-2	-2	- 2	-2	- 2	
Column command to column command		t _{CCD}	1	1	1	1	1	1	1	
Write command to data in latency		t _{WCD}	0	0	0	0	0	0	0	
DQM to data in		t _{DID}	0	0	0	0	0	0	0	
DQM to data out		t _{DOD}	2	2	2	2	2	2	2	
CKE to CLK disable		t _{CLE}	1	1	1	1	1	1	1	
Register set to active command		t _{RSA}	1	1	1	1	1	1	1	
CS̄ to command disable		t _{CDD}	0	0	0	0	0	0	0	
Power down exit to command input		t _{PEC}	1	1	1	1	1	1	1	

Relationship Between Frequency and Minimum Latency

Parameter		Symbol	- 8		- 7K	- 7J		- 10K		Notes
Frequency(MHz)			125	83	100	100	66	100	66	
t _{CK} (ns)			8	12	10	10	15	10	15	
Burst stop to output valid data hold	(CL=2)	I _{BSR}	-	1	1	-	1	-	1	
	(CL=3)	I _{BSR}	2	2	2	2	2	2	2	
Burst stop to output high impedance	(CL=2)	I _{BSH}	-	2	2	-	2	-	2	
	(CL=3)	I _{BSH}	3	3	3	3	3	3	3	
Burst stop to write data ignore		I _{BSW}	0	0	0	0	0	0	0	

Notes : 1. I_{RCD} to I_{RRD} are recommended value.

Unit: mm



12