



HI-REL DATA SHEET

HM 65687

64 k x 1
ULTIMATE CMOS SRAM

FEATURES

- ACCESS TIME : 35*/45/55 ns
- VERY LOW POWER CONSUMPTION
 - ACTIVE : 175.0 mW (typ)
 - STANDBY : 2.0 μ W (typ)
 - DATA RETENTION : 0.8 μ W (typ)
- WIDE TEMPERATURE RANGE : - 55 TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED

* Preliminary

DESCRIPTION

The HM 65687 is a very low power CMOS static RAM organized as 65536 x 1 bit. It is manufactured using the MHS high performance CMOS technology named SCMOS.

With this process, MHS is the first to bring the solution for applications where fast computing is as mandatory as low consumption, such as the aerospace electronics, the portable instruments or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the HM 65687 combines an extremely low standby

supply current (Typical value = 0.1 μ A) with a fast access time at 35 ns over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Extra protection against heavy ions is given by the use of an epitaxial layer of a P substrate.

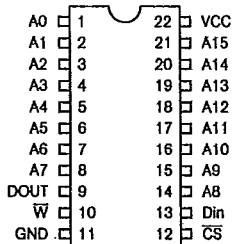
The HM 65687 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

PACKAGES

Ceramic 300 mils, 22 pins, DIL.

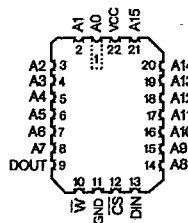
LCC, 22 pins.

Pinout DIL 22 pins (top view)



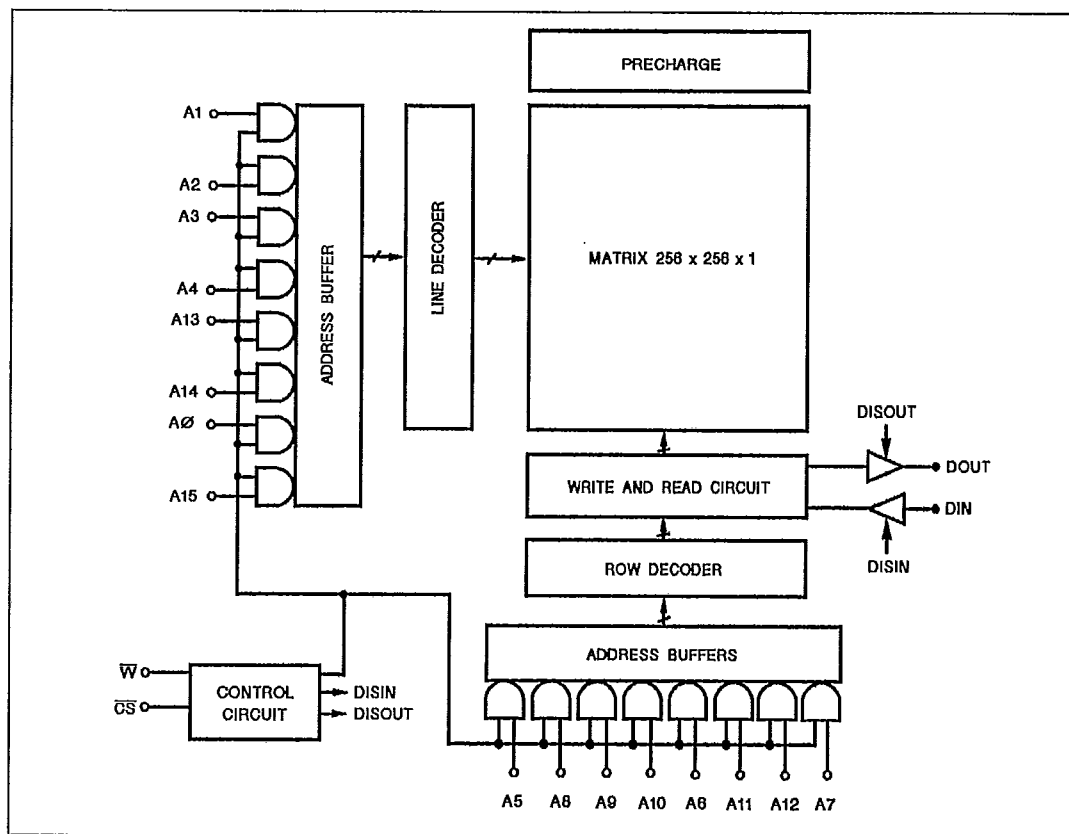
* preliminary

Pinout LCC 22 pins (top view)

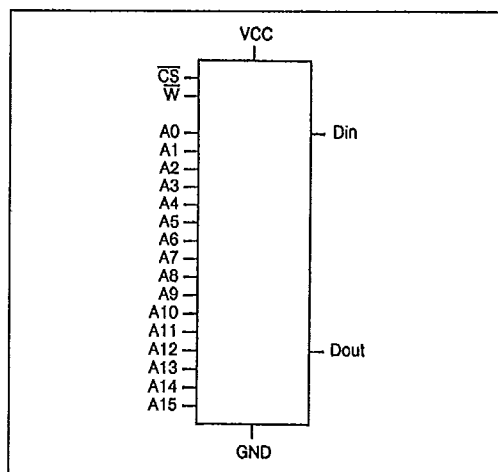


MATRA M H S

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

A0-A15	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	Vcc	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect/Power down
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

MATRA M H S

Supply voltage to GND potential : - 0.3 V to + 7.0 V

Input or Output voltage applied : (Gnd - 0.3 V) to (Vcc + 0.3 V)

Storage temperature : - 65°C to + 150°C

Electro static discharge voltage > 2000 V (MIL STD 883, METHOD 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	Vcc = 5 V $\pm$ 10 %	- 55°C to + 125°C
Industrial	Vcc = 5 V $\pm$ 10 %	- 40°C to + 85°C

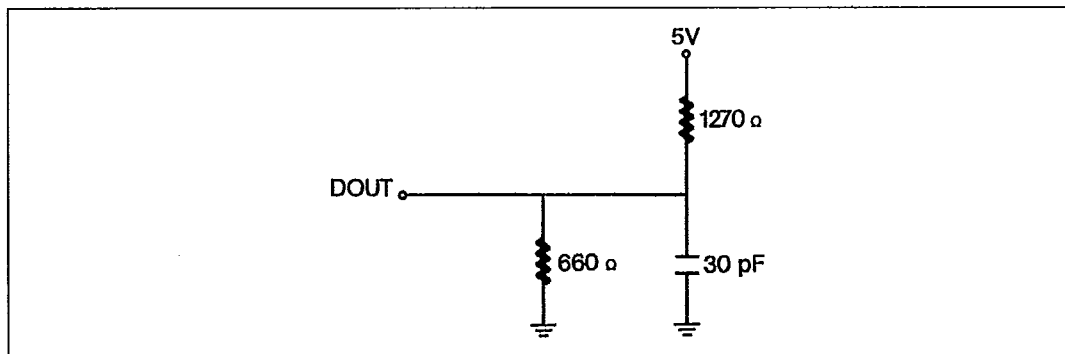
ELECTRICAL CHARACTERISTICS

DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65687 Q	65687 B	65687 S	65687	65687 C	Unit	Value	Note 8
ICCSB (1)	Standby supply current	20	15	20	15	20	mA	Max	M
ICCSB1 (2)	Standby supply current (I/M)	500	5/50	100/500	5/50	100/500	μ A	Max	M
ICCOP (3)	Operating supply current	100	75	100	75	100	mA	Max	M
ICC (4)	Operating supply current	20	15	20	15	20	mA	Max	M
II/O (5)	Input/Output leakage current	$\pm$ 1	$\pm$ 1	$\pm$ 1	$\pm$ 1	$\pm$ 1	μ A	Max	M
VIL (6)	Input low voltage	0.8	0.8	0.8	0.8	0.8	V	Max	T
VIH (6)	Input high voltage	2.2	2.2	2.2	2.2	2.2	V	Min	T
VOL (7)	Output low voltage	0.4	0.4	0.4	0.4	0.4	V	Max	M
VOH (7)	Output high voltage	2.4	2.4	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	5	5	5	5	5	pF	Max	G
C OUT	Output capacitance	7	7	7	7	7	pF	Max	G

- Notes : 1. $CS1 > VIH$, $CS2 < VIL$
 2. $CS1 > Vcc - 0.3V$, $CS2 < -0.3V$, Output current = 0 mA, I = Industrial M = Military
 3. Vcc max, Iout = 0 mA, Duty cycle 100 %, F = max, Vin = Vcc / Gnd
 4. $CS1 < -VIL$, $CS2 > VIH$, Iout = 0 mA, Vin = Gnd to Vcc
 5. Vcc = 5.5V, Vin = Gnd to Vcc
 6. VIH max = Vcc + 0.3V, VIL min = - 0.3V or - 1V pulse width 50 ns.
 7. Vcc min, IOL = 4 mA, IOH = - 1 mA
 8. Including open/short test or inputs clamp voltage.
 G - Guaranteed - Not tested : Parameter measured at design validation and at any design change.
 M - Measured : Parameter measured and data-log capability.
 T - Tested : Parameter verification during testing.

OUTPUT LOAD



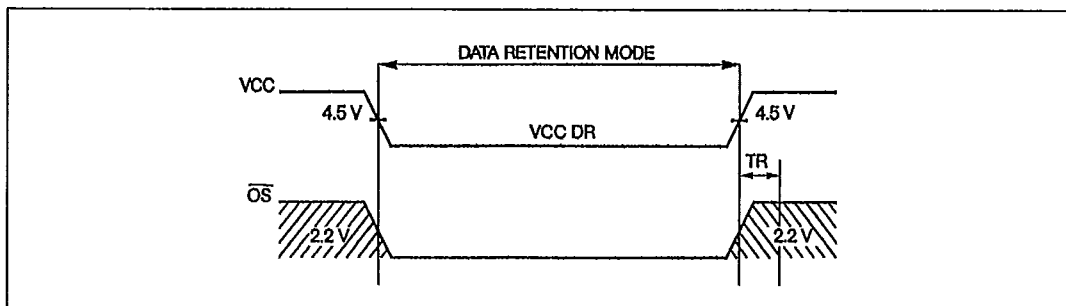
DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within V_{CC} to $V_{CC} + 0.3$ V.

2. $\overline{CS}$ must be kept between $V_{CC} + 0.3$ V and 70 % of V_{CC} during the power up and power down transitions.

3. The RAM can begin operation > 45 ns after V_{CC} reaches the minimum operating voltage (4.5V).

TIMING**DATA RETENTION CHARACTERISTICS**

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM (12)	UNIT	NOTE 8
VCCDR	Vcc for data retention	2.0	—	—	V	T
TCDR	Chip deselect to data retention time	0.0	—	—	ns	
TR	Operation recovery time	TAVAV (10)	—	—	ns	
ICCDR1 (11)	Data retention current @ 2.0 V : HM-65687 (B)- HM-65687 S/C/Q	— —	0.1 0.1	3/20.0 30/200.0	μA μA	M M
ICCDR2 (11)	Data retention current @ 3.0 V : HM-65687 (B)- HM-65687 S/C/Q	— —	0.3 0.3	3/30.0 50/300.0	μA μA	C C

Notes : 9. $T_A = 25^\circ C$.

10. TAVAV = Read cycle time.

11. $CS = V_{CC}$, $V_{in} = Gnd/V_{CC}$, this parameter is only tested to $V_{CC} = 2$ V.

12. I = Industrial / M = Military.

ELECTRICAL CHARACTERISTICS**AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)****AC CONDITIONS :**

Input pulse levels : Gnd to 3.0 V

Input rise : 5 ns

VCC : 5 V $\pm$ 10 %

Input timing reference levels : 1.5 V

Output load : 1 TTL gate + 30 pF

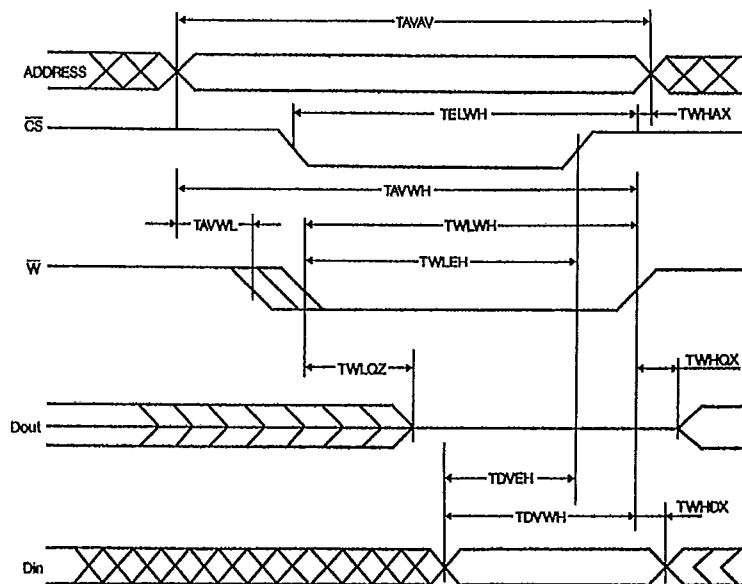
WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER *	65687 Q	65687 B	65687 S	65687	65687 C	UNIT	VALUE
TAVAV	Write cycle time	35	45	45	55	55	ns	min
TAVWL	Address set-up time	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	35	45	45	55	55	ns	min
TDVWH	Data set-up time	22	25	25	25	25	ns	min
TELWH	CS low to write end	35	45	45	55	55	ns	min
TWLQZ (12)	Write low to high Z	15	15	15	20	20	ns	max
TWLWH	Write pulse width	30	40	40	50	50	ns	min
TWHAX	Address hold to end of write	5	5	5	5	5	ns	min
TWHDX	Data hold time	3	3	3	3	3	ns	min
TWHQX (12)	Write high to low Z	0	0	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

- * : All parameters only tested and screened during full speed functional test.
For subgroups 7 and 8, functional test is performed at 1 MHz with VIL = 0V and VIH = 3V.

WRITE CYCLE

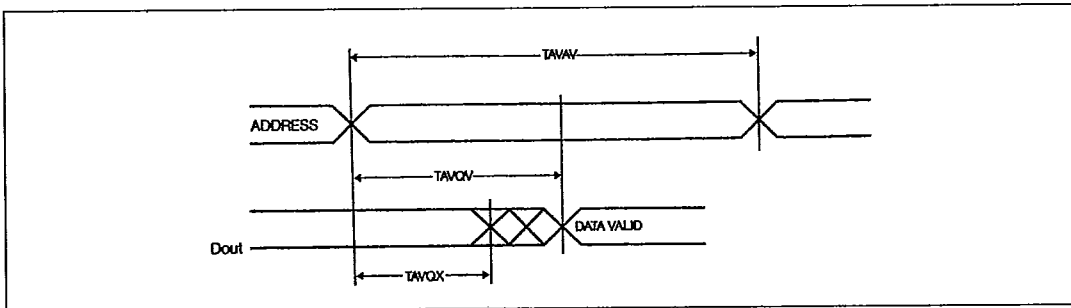


Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

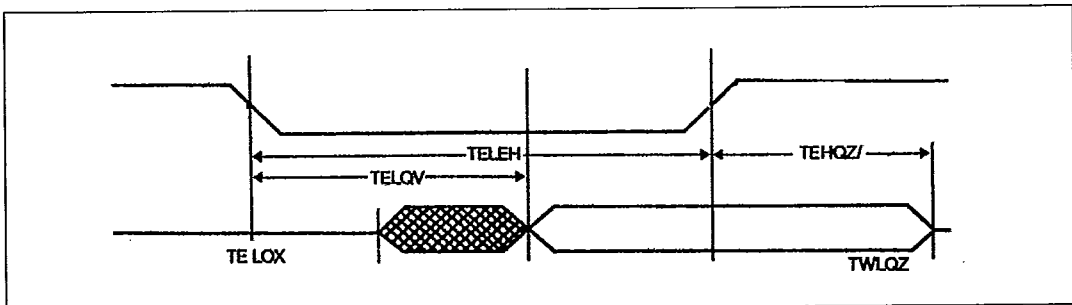
READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER *	65687 Q	65687 B	65687 S	65687	65687 C	UNIT	VALUE
TAVAV	Read cycle time	35	45	45	55	55	ns	min
TAVQV	Address access time	35	45	45	55	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	3	ns	min
TELQV	Chip-select access time	35	45	45	55	55	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	5	5	ns	min
TTEHQZ	$\overline{CS}$ high to high Z	35	45	45	55	55	ns	max

READ CYCLE nb 1 (notes 13, 14)

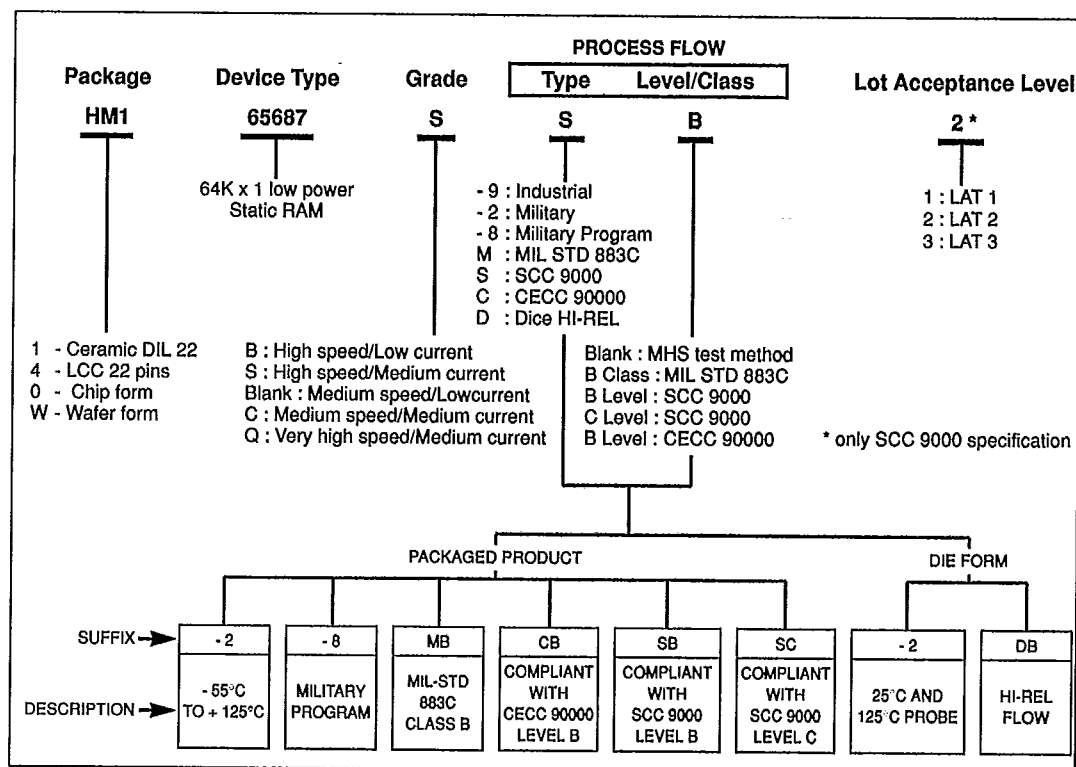


READ CYCLE nb 2 (notes 13, 15)

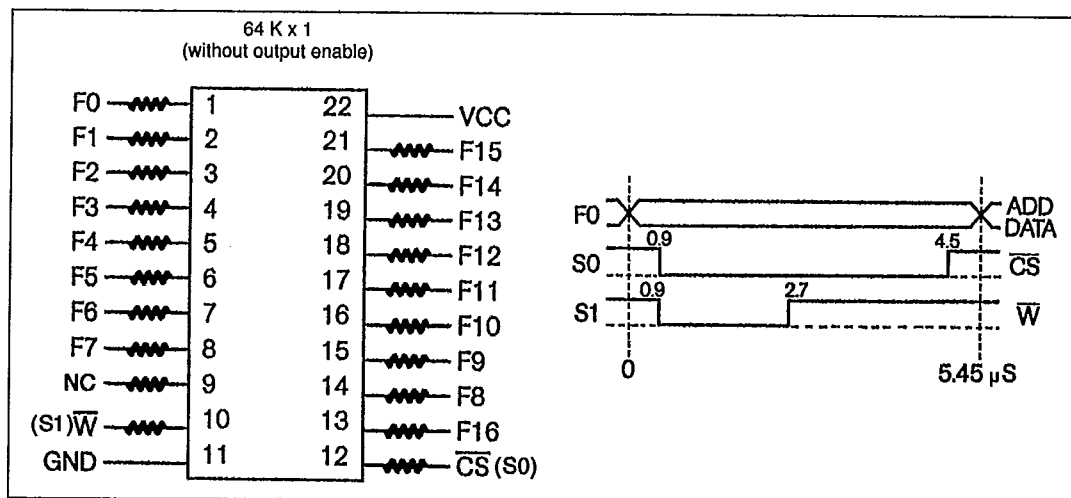
Notes : 13. $\overline{W}$ is high for read cycle.14. Device is continuously selected $\overline{CS} = \text{VIL}$.

15. Address valid prior to or coincident with CS transitive.

ORDERING INFORMATION



BURN IN SCHEMATICS



VCC = 5 V (-0, +0,5)

R = 1Ω per pin

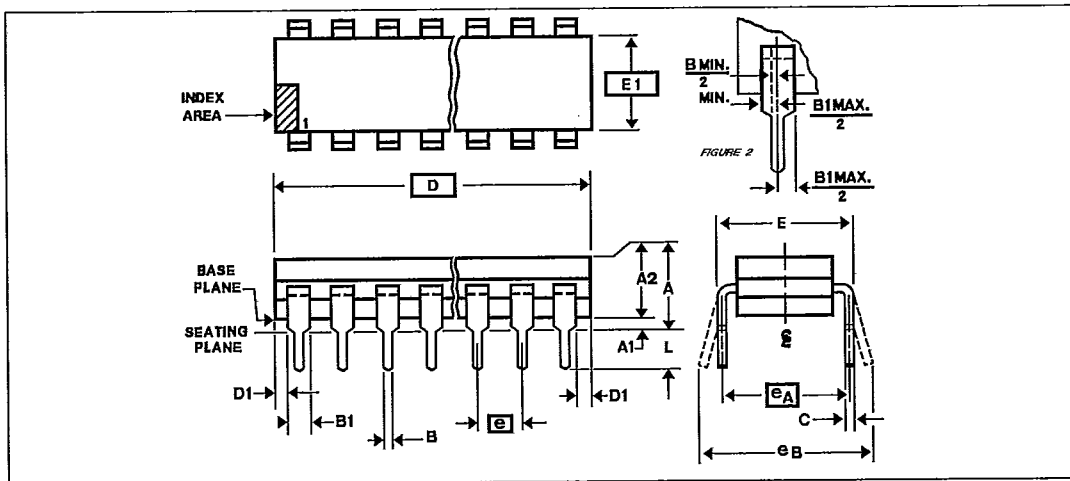
F0 = 91.6 KHz ± 20 %

Fn = 1/2 F n-1

S0 & S1 : programmable signals for write / read cycles

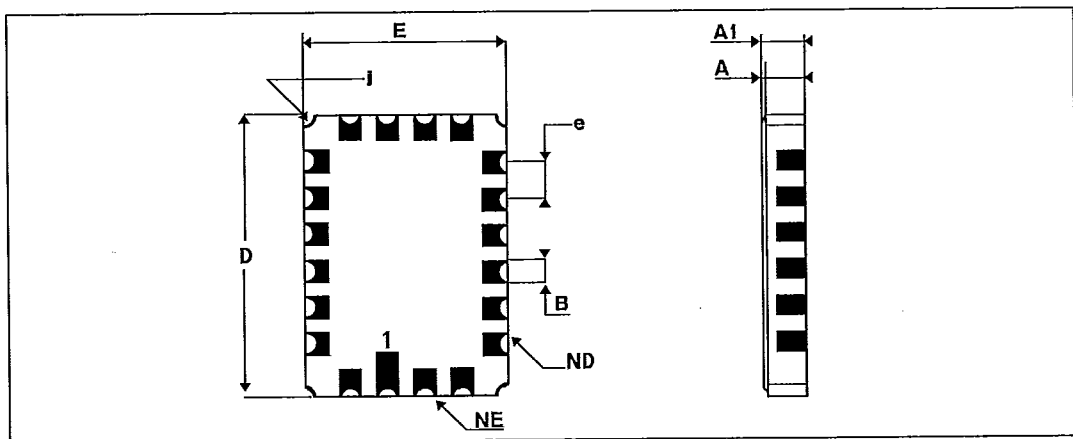
NC = Not connected

PACKAGE OUTLINES



22 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	L
MM	MIN	—	0.51	3.17	0.36	0.89	0.20	26.92	0.13	7.82	7.24	2.54	7.62	—	3.05
	MAX	5.84	—	4.95	0.58	1.78	0.38	28.19	—	8.00	7.87	BSC	BSC	10.82	5.08
INCHES	MIN	—	.020	.125	.014	.035	.008	1.060	.005	.308	.285	.100	.300	—	.125
	MAX	.230	—	.195	.023	.070	.015	1.110	—	.315	.310	BSC	BSC	.426	.200

22 LDS .050 CENTER LEADLESS
RECTANGULAR CHIP CARRIER

		A	A1	B	D	E	e	h	j	ND	NE
MM	MIN	1.37	1.62	0.15	12.31	7.24	1.27	—	0.30	7	4
	MAX	1.67	1.93	—	12.57	7.49	BSC	—	RAD	7	4
INCHES	MIN	.054	.064	.006	.485	.285	.050	—	.012	7	4
	MAX	.066	.076	—	.495	.295	BSC	—	RAD	7	4