Features

- Transport Demultiplexer
  - 160 Mbps (parallel) or 60 Mbps (serial) maximum continuous input rate
  - Table selection filtering
  - Packet Identifier Filtering (PID)

- Video Decoder
  - Up to 50 Mbps decoding
  - Compliant with ISO/IEC 13818-2 Profile @ Main Level and 4:2:2 Profile @ Main Level
  - Supports DVB standard
  - Horizontal and vertical filters
  - Supports pan and scan in 1/16 pel accuracy
  - Supports multiple input image sizes
  - On-Screen Display (OSD)
  - Programmable output interface
  - Programmable PTS filtering
  - 3:2 pull-down support
  - Supports VBI output

- Audio Decoder
  - Dual Audio Decoders with two channel outputs (six channels with Dolby[1] Digital)
  - Supports ISO/IEC 13818-3 MPEG-1 and 2, Layers I and II audio
  - Decodes elementary streams (ES) or packetized elementary streams (PES)
  - Multiple playback sampling frequencies
  - Multiple playback modes including PCM and Karaoke
  - Dolby Digital decoding and playback (IBM39MPEGCS24DPFA16C only)
  - Host controlled programming interface
  - 64 step audio attenuation with smooth transition between steps

- Audio/video synchronization
- Audio and video error detection, concealment, and notification
- 208 pin, plastic quad flat pack (PQFP) package

Description

The IBM39MPEGCS24PFA16C and IBM39MPEGCS24DPFA16C are high performance audio/video decoders, designed for high-end decompression applications, such as broadcast distribution, professional audio/video editing and content creation, digital television set-top boxes, and high-end PC multimedia applications. They comply with the ISO/IEC 13818-2 Recommendation H.262 Draft International Standard (MPEG-2 standard) Main Profile @ Main Level and 4:2:2 Profile @ Main Level. They support interlaced output video data and are capable of supporting MPEG-2 I,P,B compressed data streams up to a sustained rate of 50 Mbps.

These decoders provide an MPEG transport demultiplexer, an MPEG video decoder and two MPEG/Dolby Digital audio decoders. The transport demultiplexer can receive transport streams up to 160 Mbps. The video decoder can decode MPEG-2 Main Profile as well as

4:2:2 Profile @ Main Level video packetized elementary streams. Dual audio decoders can decode MPEG Layers I and II and Dolby Digital (IBM39MPEGCS24DPFA16C only) packetized elementary streams. Two built-in PLLs generate the audio sampling frequencies and support audio and video synchronization. Gen-lock is supported by providing separate video and STC clock inputs. The IBM39MPEGCS24PFA16C and IBM39MPEGCS24DPFA16C are 208 pin, plastic quad flat pack (PQFP) package devices.

The integrated audio decoder is capable of decoding Dolby Digital 5.1 channels, or MPEG-2 compatible Layer I and II streams in support of compliant bit rates and sample rates to produce two-channel basic stereo (with no downmixing) digital audio output.
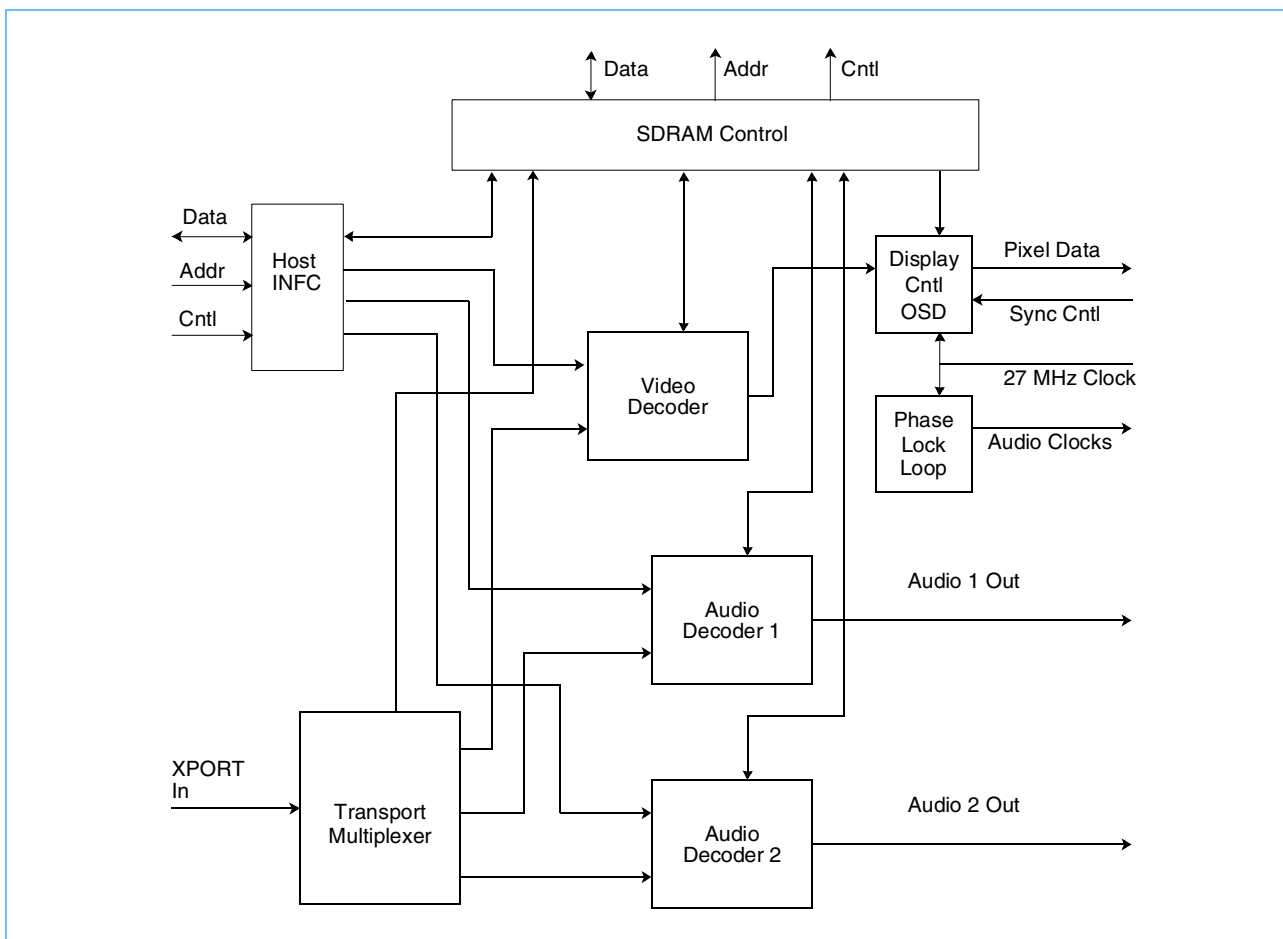
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1. "Dolby" is a trademark of Dolby Laboratories.

Ordering Information

IBM Part Number	Video 4:2:2 P@ML	Audio MPEG-2 Layer I and Layer II	Audio Dolby Digital[1]
IBM39MPEGCS24PFA16C	Yes	Yes	No
IBM39MPEGCS24DPFA16C	Yes	Yes	Yes

1. Dolby certification is pending. Dolby Digital license is required.

Block Diagram

Transport Demultiplexer

The transport demultiplexer performs the MPEG-2 transport stream parsing to extract the packetized elementary streams for the audio and video decoders. It provides a full set of demultiplexing functions, including synchronization, PID filtering, clock recovery, table section filtering, CRC checking, and data management. These basic functions are configured by the application and implemented in hardware for improved performance and to minimize the impact on the remainder of the system.

The transport demultiplexer is compliant with ISO/IEC 13818-1 system layer standard, and operates at up to 160 Mbps (parallel) or 60 Mbps (serial) maximum continuous input rate.

MPEG-2 Transport Synchronization

The transport demultiplexer accepts either parallel (8-bit) or serial data. It detects the synchronization character and establishes transport packet boundaries. In the case of serial input, where only a bit clock is provided, it also establishes byte alignment. There are input controls for error flagging and to force packet alignment if already established by a front end device.

PID Filtering

There are up to 32 programmable PID values that are used to filter the transport stream. The PID filter associates a 5-bit PID index with each of the 32 entries. Entries in the PID filter can be disabled by writing the null PID value. PID index 31 is reserved for the video PID, PID index 30 is for the audio1 PID, and PID index 29 is for the audio2 PID. The others are defined by the application.

Clock Recovery

The transport demultiplexer assists in recovering the program clock from the transport stream. It extracts Program Clock References (PCRs) from the indicated PID, calculates the offset from the current System Time Clock (STC) value, and compares it against a threshold defined by the application to determine if clock frequency correction is required.

The demultiplexer can either filter the clock difference directly, using a simple hardware algorithm, or it can provide an interrupt to allow the application to filter the difference. The output of the filter is loaded into a pulse modulating register, and the serial pulse train output is used to regulate an external Voltage-Controlled Crystal Oscillator (VCXO), or similar device.

Time Base Changes

When a system time base change occurs in the PCR PID stream, the transport will automatically load the STC with the new value. The first audio1, audio2, and video packets with payload which arrive after the system time base change are marked. The transport indicates the first byte of the data following the time base change to each decoder.

Table Section Filtering

The transport hardware can filter table sections, which reduces the processing load on the application and minimizes the size of temporary work spaces in system memory.

Up to 64 different 4-byte filter blocks consisting of a bit pattern and a bit mask can be defined by the application. Section filters can be constructed from one or more filter blocks to provide deep filtering into a table section. Multiple section filters can be attached to a single PID. Filter blocks can be assigned to the 32 PID indexes as needed by the application. The filtering mechanism supports multiple sections per packet as well as sections which span multiple packets.

Error Handling

The transport demultiplexer simplifies the system-level tasks of error handling and time base (STC) changes by using the compressed data connection to communicate directly with the decoders. Errors are detected and flagged in the data stream, allowing the decoders to mask the error and recover without system intervention.

Video Decoder

The video decoder is compliant with ISO/IEC 13818-2 Main Profile at Main Level and 4:2:2 Profile at Main Level. European DVB standard is supported.

Horizontal and vertical filters deliver high quality video. Pan and scan are supported with 1/16 pel accuracy. Error concealment is achieved with a sophisticated transport error support. PTS filtering is programmable.

The internal processor is the central point of control for the video decoder. It interacts with the host processor through the host interface for high level commands and status. Internally, the video decoder's processor interacts with a Huffman decoder (Variable Length Code Decoder (VLCD)), Inverse Quantizer, Inverse Discrete Cosine Transform (IDCT) Unit, and a Motion Compensation Unit.

Video Input

Elementary Streams (ES) and Packetized Elementary Streams (PES) are decoded at speeds up to 50 Mbps.

For source material that comes from film, frame rate conversion using 3:2 pulldown is supported. The MPEG-2 Pan Scan feature is supported which allows conversion of 16:9 aspect ratio images to conventional 4:3 aspect ratio displays.

The host data bus is used to input compressed audio and video data when a transport stream is not used.

Supported Input Image Sizes

Size	Aspect Ratio	Format
352 x 240 (288)	4:3	NTSC(PAL)
352 x 480 (576)	4:3	NTSC(PAL)
480 x 480 (576)	4:3	NTSC(PAL)
544 x 480 (576)	4:3	NTSC(PAL)
720 x 480 (576)	16:9	pan and scan in NTSC(PAL)
544 x 480 (576)	16:9	pan and scan in NTSC(PAL)
480 x480 (576)	16:9	pan and scan in NTSC(PAL)
352 x 240 (288)	16:9	pan and scan in NTSC(PAL)
352 x 480 (576)	16:9	pan and scan in NTSC(PAL)

Synchronization

The video decoder synchronizes the decoding of the video stream to the STC which is set by the host processor, by comparing PTS with the STC. If the difference exceeds the tolerance, the current decoded picture will either be repeated or the next B-frame will be skipped to recover synchronization. If a B-frame is not available, synchronization is accomplished by skipping a P-frame.

On-Screen Display (OSD) and Output Interface

A versatile OSD enhances the user's ability to control video decoding. It includes a multi-region link list with a color table for each region. Advanced features of the OSD include block copying, overlay and video blending, video shading (in OSD area), and animation support. OSD supports Professional Profile Display sizes up to 512 lines NTSC, 608 lines for PAL.

OSD supports Direct color (16 bits per pixel bitmap) resolution.

Through the OSD, the resolution of each region of the bitmap can be programmed separately, with the following options:

- 2 bits/pixel pair
- 2 bits/pixel
- 4 bits/pixel pair
- 4 bits/pixel
- 8 bits/pixel pair
- 8 bits/pixel

The output interface supports three sync modes: composite blanking with field ID, H/V Sync and CCIR 656 Master Mode. Signal polarity is programmable. The pixel data bus can be 8 or 16 bits.

Memory Interface

The Memory Interface is based on a 16-bit bus, and is designed to use either 16 Mb or 64 Mb, 125 MHz SDRAM, for a 4 MB or 8 MB configuration.

Audio Decoder

The IBM39MPEGCS24PFA16C/DPFA16C each contain two audio decoders. The decoders are configured by the host processor through its own set of host accessible registers.

Both of the audio decoders in the IBM39MPEGCS24DPFA16C device can perform Dolby Digital decoding as well as MPEG decoding. The IBM39MPEGCS24PFA16C device has no Dolby Digital capabilities.

Audio Input

The audio decoder receives and decodes either PES (Packetized Elementary Stream) or ES (Elementary Stream) audio data via a 20-bit Digital Signal Processor (DSP) engine. Compressed audio data can be received from the audio PID in the transport stream through the transport demultiplexer or through the host data bus as a PES or ES Stream. Input bit rate is supported up to 640 Kbps.

The audio DSP is a 20-bit computational engine which decodes the audio MPEG and Dolby Digital bit-streams, and formats PCM data for playback. PCM playback, and the MPEG and Dolby Digital algorithms, are executed via microcode, which is downloaded through the Host Interface.

Tone Generation

The audio decoder is capable of generating a specified tone frequency with a duration from 0.1 second to 3 seconds. The user may select from 128 possible tones, 31 durations and 8 attenuations. The tones are over 10 octaves of American Standard pitch ("A" = 440 Hz). Audio attenuation is performed in 64 steps with smooth transitions between steps.

Audio Output

The audio decoder supports the playback of either 16-, 18-, or 20-bit unformatted PCM bitstreams. Six sampling frequencies (16, 22.05, 24, 32, 44.1, and 48 kHz) are supported for unformatted PCM bitstreams. Both one channel (mono) and two channel (stereo) output is supported for MPEG decoding and PCM inputs, while up to six channels are possible for Dolby Digital decoding.

The interface can be programmed to support the I^2S mode, the Left Justified mode, or the Right Justified mode. To maximize compatibility with a wide variety of audio DACs, the Audio CLK signal can be programmed to 64 times the sampling clock to support the 20-bit output sample or 32 times to support the 16-bit output sample.

In addition to the PCM output, a S/PDIF (IEC958) interface is provided. This interface can either output encoded Dolby Digital (AC-3) data while decoding a Dolby Digital (AC-3) stream, or one of three pairs of channels of PCM data.

Synchronization

The audio decoder synchronizes the decoding of the audio stream to the STC which is set by the host processor by comparing PTS with the STC. If the difference exceeds the tolerance, the decoder skips or repeats samples. Audio synchronization can be disabled.

Audio / video synchronization is supported with PTS/STC comparison on each audio frame. There is a built-in phase-locked-loop to provide the audio clocks for audio and video synchronization.

Error Checking

Errors are checked and concealed to ensure high quality audio. MPEG error checking uses frame-size calculations for each frame. Audio bitstream error concealment is performed, either by sample repeats or muting, due to loss of Audio Frame synchronization or detection of CRC errors.

Dolby Digital (IBM39MPEGCS24DPFA16C only)

Only the IBM39MPEGCS24DPFA16C device is compatible with Dolby Digital. This device can decode Dolby Digital input. The audio output has three data out signals to support the six channels in Dolby Digital. An S/PDIF output is also available for either two channels of decoded data or output of the Dolby Digital stream.

Additionally, Dolby Digital Karaoke mode and Dolby Digital Surround mode (DSMOD) are supported. DSMOD pins interface to external surround mode circuitry.

Support is also provided for several downmix combinations, dialog normalization, and dynamic range control.

Environmental and Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Supply Voltage (3.3 V)	3.80	V	1
V_{DDA1}	Supply Voltage (2.5 V)	2.70	V	1
V_{DDA2}	Supply Voltage (2.5 V)	2.70	V	1
T_A	Ambient operating temperature range	70	°C	1, 2
T_S	Storage temperature range	150	°C	1, 3
P_D	Power Dissipation	1	W	

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Operating temperature range is based on ambient air temperature with natural convection.
3. Storage temperature range is guaranteed for up to 100 worst case cycles.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{DD}	Supply Voltage (3.3 V)		3.14	3.3	3.47	V
V_{DDA1}	Supply Voltage (2.5 V)		2.38	2.5	2.63	V
V_{DDA2}	Supply Voltage (2.5 V)		2.38	2.5	2.63	V
I_{CC}	Supply Current	3.3 V		250		mA
		2.5 V		80		mA
T_A	Ambient operating temperature range		0		70	°C
T_S	Storage temperature range		-65		150	°C

Current Specifications

Symbol	Parameter	RAS/CAS/ Host Data	All other drivers	Units	Notes
I_{SINK}(DC)	Sink Current	8.0	6.0	mA	1
I_{SOURCE}(DC)	Source Current	12.0	9.0	mA	2

1. I_{SINK} is measured at 0.4 V
2. I_{SOURCE} is measured at 2.4 V

DC Electrical Characteristics

Usage	MAUL	MPUL	LPUL	MPDL	LPDL	MADL	Units
3.3 V LVTTL Receiver	3.80	3.30	2.00	0.80	0.00	-0.60	V
3.3 V LVTTL Driver	3.80	3.30	2.40	0.40	0.00	-0.60	V
Definitions MAUL: Maximum Allowable Up Level MPUL: Maximum Positive Up Level LPUL: Least Positive Up Level MPDL: Maximum Positive Down Level LPDL: Least Positive Down Level MADL: Minimum Allowable Down Level							

Pin and Signal Information

In the following tables the use of overbars, for example $\overline{\text{RESET}}$, designates signals that are active low. All signals with no overbar are assumed to be active high.

Pin Descriptions

Signal Name	Description	Pin Type
27 MHz CLK	27 MHz Clock	Input
64MBIT_A11	64MBIT_A11	Output
64MBIT_BA1	64MBIT_BA1	Output
AUD 1 CLK	Audio 1 Clock	Output
AUD1 DAC CLK	Audio 1 DAC Clock	Output
AUD1 DATA(n)	Audio 1 Data Out(n)	Output
AUD1 DEEMPHASIS(n)	Audio 1 Deemphasis(n)	Output
AUD1 DSURMOD(n)	Audio 1 Dolby Sur Mode(n)	Output
AUD1 L/R	Audio 1 Left / Right	Output
AUD1 REQ	Audio 1 Data Request	Output
AUD1 SPDIF	Audio1 S/PDIF	Output
$\overline{\text{AUD1 STROBE}}$	Audio 1 Compressed Data Strobe	Input
AUD2 CLK	Audio 2 Clock	Output
AUD2 DAC CLK	Audio 2 DAC Clock	Output
AUD2 DATA(n)	Audio 2 Data Out(n)	Output
AUD2 DEEMPHASIS(n)	Audio 2 Deemphasis(n)	Output
AUD2 DSURMOD(n)	Audio 2 Dolby Sur Mode(n)	Output
AUD2 L/R	Audio 2 Left/Right	Output
AUD2 REQ	Audio 2 Data Request	Output
AUD2 SPDIF	Audio 2 S/PDIF	Output
$\overline{\text{AUD2 STROBE}}$	Audio 2 Compressed Data Strobe	Input
BA0	BA0	Output
$\overline{\text{CAS}}$	Column Address Select	Output
CD21 MODE	CD21 Mode	Input
CKE	SDRAM Clock Enable	Output
CLK	SDRAM Clock	Output
CREF	Video Clock Reference	Output
$\overline{\text{CS}}$	Chip Select	Input
$\overline{\text{CS0}}$	SDRAM Chip Select 0	Output

Pin Descriptions

Signal Name	Description	Pin Type
$\overline{CS1}$	SDRAM Chip Select 1	Output
DTACK MODE	Dtack Mode	Input
GND	Ground	Ground
HOST ADDR(n)	Host Address Bus(n)	Input
HOST DATA(n)	Host Data Bus(n)	Bi-directional
HSC	Horizontal Sync Control	Input
IRQ	Interrupt Request	Output
LDQM	SDRAM LDQM	Output
LOW WORD	Low Word	Input
MA(n)	Memory Address(n)	Output
MD(n)	Memory Data(n)	Bi-directional
N/C	No Connect	No Connect
$\overline{OE}$	Output Enable	Input
OSC SEL	OSC Select	Input
PIXEL DATA(n)	Pixel Data(n)	Output
$\overline{RAS}$	Row Address Select	Output
RD/$\overline{WR}$	Read / Write	Input
READY	Ready	Output
$\overline{RESET}$	Reset	Input
STC 27 MHz CLK	STC 27 MHz CLK	Input
TTX DATA	Teletext Data	Output
TTX DATA REQ	Teletext Data Request	Input
UDQM	SDRAM UDQM	Output
V_{DD}	Voltage (3.3 V)	Power
V_{DDA1}	Voltage (2.5 V)	Power
V_{DDA2}	Voltage (2.5 V)	Power
VID REQ	Video Data Request	Output
$\overline{VID\ STROBE}$	Video Compressed Data Strobe	Input
VSC	Vertical Sync Control	Input
$\overline{WE}$	Write Enable	Output
$\overline{WP}$	Write Pulse	Input
XPORT CLK	Transport Stream Data Clock	Input

Pin Descriptions

Signal Name	Description	Pin Type
XPORT DATA(n)	Transport Data In(n)	Input
XPORT ERROR	Transport Error	Input
$\overline{\text{XPORT PWM}}$	Transport PWM	Output
XPORT START	Transport Start	Input
XPORT VALID	Transport Data Valid	Input

IBM

Pin Assignments, Sorted by Pin Number

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	V_{DD}	31	GND	61	GND
2	GND	32	V_{DDA1}	62	HOST ADDR 6
3	MD1	33	V_{DD}	63	HOST ADDR 5
4	MD0	34	MA3	64	HOST ADDR 4
5	UDQM	35	$\overline{RESET}$	65	HOST ADDR 3
6	LDQM	36	MA2	66	HOST ADDR 2
7	V_{DD}	37	MA1	67	V_{DD}
8	CLK	38	MA0	68	N/C
9	CKE	39	V_{DD}	69	V_{DD}
10	$\overline{WE}$	40	XPORT CLK	70	OSC SEL
11	GND	41	GND	71	HOST ADDR 1
12	$\overline{CAS}$	42	27 MHz CLK	72	HOST ADDR 0
13	$\overline{RAS}$	43	XPORT ERROR	73	IRQ
14	V_{DD}	44	N/C	74	VID REQ
15	$\overline{CS0}$	45	XPORT VALID	75	AUD1 REQ
16	$\overline{CS1}$	46	XPORT START	76	GND
17	V_{DD}	47	$\overline{XPORT\ PWM}$	77	AUD2 REQ
18	V_{DD}	48	XPORT DATA 7	78	$\overline{CS}$
19	BA0	49	XPORT DATA 6	79	RD/$\overline{WR}$
20	64MBIT_BA1	50	XPORT DATA 5	80	$\overline{WP}$
21	64MBIT_A11	51	V_{DD}	81	READY
22	MA10	52	GND	82	V_{DD}
23	MA9	53	V_{DD}	83	$\overline{VID\ STROBE}$
24	GND	54	GND	84	V_{DD}
25	MA8	55	XPORT DATA 4	85	$\overline{AUD1\ STROBE}$
26	MA7	56	XPORT DATA 3	86	$\overline{AUD2\ STROBE}$
27	MA6	57	XPORT DATA 2	87	LOW WORD
28	MA5	58	XPORT DATA 1	88	$\overline{OE}$
29	MA4	59	XPORT DATA 0	89	HOST DATA 15
30	V_{DD}	60	HOST ADDR 7	90	GND

Pin Assignments, Sorted by Pin Number

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
91	V_{DD}	121	AUD2 SPDIF	151	PIXEL DATA 11
92	HOST DATA 14	122	AUD2 DSURMOD 1	152	PIXEL DATA 10
93	HOST DATA 13	123	V_{DD}	153	V_{DD}
94	V_{DD}	124	AUD2 DSURMOD 0	154	PIXEL DATA 9
95	HOST DATA 12	125	AUD2 DEEMPHASIS 1	155	V_{DD}
96	HOST DATA 11	126	AUD2 DEEMPHASIS 0	156	GND
97	V_{DD}	127	AUD2 DATA 2	157	V_{DD}
98	HOST DATA 10	128	GND	158	GND
99	HOST DATA 9	129	AUD2 DATA 1	159	PIXEL DATA 8
100	HOST DATA 8	130	AUD2 DATA 0	160	PIXEL DATA 7
101	V_{DD}	131	AUD 1 CLK	161	PIXEL DATA 6
102	HOST DATA 7	132	AUD1 DAC CLK	162	PIXEL DATA 5
103	V_{DD}	133	AUD1 L/R	163	V_{DD}
104	GND	134	V_{DD}	164	PIXEL DATA 4
105	V_{DD}	135	AUD1 SPDIF	165	PIXEL DATA 3
106	GND	136	AUD1 DSURMOD 1	166	V_{DD}
107	HOST DATA 6	137	AUD1 DSURMOD 0	167	PIXEL DATA 2
108	HOST DATA 5	138	GND	168	PIXEL DATA 1
109	HOST DATA 4	139	STC 27 MHz CLK	169	GND
110	HOST DATA 3	140	AUD1 DEEMPHASIS 1	170	PIXEL DATA 0
111	V_{DD}	141	AUD1 DEEMPHASIS 0	171	VSC
112	HOST DATA 2	142	AUD1 DATA 2	172	V_{DD}
113	HOST DATA 1	143	AUD1 DATA 1	173	V_{DDA2}
114	GND	144	V_{DD}	174	V_{DD}
115	HOST DATA 0	145	AUD1 DATA 0	175	V_{DD}
116	AUD2 CLK	146	PIXEL DATA 15	176	MD 15
117	GND	147	PIXEL DATA 14	177	MD 14
118	N/C	148	PIXEL DATA 13	178	CREF
119	AUD2 DAC CLK	149	GND	179	TTX DATA REQ
120	AUD2 L/R	150	PIXEL DATA 12	180	GND

Pin Assignments, Sorted by Pin Number

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
181	HSC	191	MD 10	200	MD 5
182	TTX DATA	192	MD 9	201	GND
183	CD21 MODE	193	GND	202	GND
184	V_{DDA2}	194	MD 8	203	MD 4
185	DTACK MODE	195	N/C	204	MD 3
186	V_{DD}	196	V_{DD}	205	GND
187	MD 13	197	MD 7	206	MD 2
188	MD 12	198	GND	207	V_{DD}
189	MD11	199	MD 6	208	GND
190	GND				

Pin Assignments, Sorted by Signal Name

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
27 MHz CLK	42	$\overline{\text{CAS}}$	12	GND	190
64MBIT_A11	21	CD21 MODE	183	GND	193
64MBIT_BA1	20	CKE	9	GND	198
AUD 1 CLK	131	CLK	8	GND	201
$\overline{\text{AUD1 STROBE}}$	85	CREF	178	GND	202
AUD1 DAC CLK	132	$\overline{\text{CS}}$	78	GND	205
AUD1 DATA 0	145	$\overline{\text{CS0}}$	15	GND	208
AUD1 DATA 1	143	$\overline{\text{CS1}}$	16	HSC	181
AUD1 DATA 2	142	DTACK MODE	185	HOST ADDR 0	72
AUD1 REQ	75	GND	2	HOST ADDR 1	71
AUD1 DEEMPHASIS 0	141	GND	11	HOST ADDR 2	66
AUD1 DEEMPHASIS 1	140	GND	24	HOST ADDR 3	65
AUD1 DSURMOD 0	137	GND	31	HOST ADDR 4	64
AUD1 DSURMOD 1	136	GND	41	HOST ADDR 5	63
AUD1 L/R	133	GND	52	HOST ADDR 6	62
AUD1 SPDIF	135	GND	54	HOST ADDR 7	60
AUD2 CLK	116	GND	61	HOST DATA 0	115
$\overline{\text{AUD2 STROBE}}$	86	GND	76	HOST DATA 1	113
AUD2 DAC CLK	119	GND	90	HOST DATA 10	98
AUD2 DATA 0	130	GND	104	HOST DATA 11	96
AUD2 DATA 1	129	GND	106	HOST DATA 12	95
AUD2 DATA 2	127	GND	114	HOST DATA 13	93
AUD2 REQ	77	GND	117	HOST DATA 14	92
AUD2 DEEMPHASIS 0	126	GND	128	HOST DATA 15	89
AUD2 DEEMPHASIS 1	125	GND	138	HOST DATA 2	112
AUD2 DSURMOD 0	124	GND	149	HOST DATA 3	110
AUD2 DSURMOD 1	122	GND	156	HOST DATA 4	109
AUD2 L/R	120	GND	158	HOST DATA 5	108
AUD2 SPDIF	121	GND	169	HOST DATA 6	107
BA0	19	GND	180	HOST DATA 7	102
				HOST DATA 8	100

Pin Assignments, Sorted by Signal Name

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
HOST DATA 9	99	MD 9	192	UDQM	5
IRQ	73	N/C	44	VID REQ	74
LDQM	6	N/C	68	$\overline{\text{VID STROBE}}$	83
LOW WORD	87	N/C	118	V_{DD}	1
MA0	38	N/C	195	V_{DD}	7
MA1	37	$\overline{\text{OE}}$	88	V_{DD}	14
MA10	22	OSC SEL	70	V_{DD}	17
MA2	36	PIXEL DATA 0	170	V_{DD}	18
MA3	34	PIXEL DATA 1	168	V_{DD}	30
MA4	29	PIXEL DATA 10	152	V_{DD}	33
MA5	28	PIXEL DATA 11	151	V_{DD}	39
MA6	27	PIXEL DATA 12	150	V_{DD}	51
MA7	26	PIXEL DATA 13	148	V_{DD}	53
MA8	25	PIXEL DATA 14	147	V_{DD}	67
MA9	23	PIXEL DATA 15	146	V_{DD}	69
MD0	4	PIXEL DATA 2	167	V_{DD}	82
MD1	3	PIXEL DATA 3	165	V_{DD}	84
MD10	191	PIXEL DATA 4	164	V_{DD}	91
MD11	189	PIXEL DATA 5	162	V_{DD}	94
MD12	188	PIXEL DATA 6	161	V_{DD}	97
MD13	187	PIXEL DATA 7	160	V_{DD}	101
MD14	177	PIXEL DATA 8	159	V_{DD}	103
MD15	176	PIXEL DATA 9	154	V_{DD}	105
MD2	206	RD/$\overline{\text{WR}}$	79	V_{DD}	111
MD3	204	$\overline{\text{RAS}}$	13	V_{DD}	123
MD4	203	READY	81	V_{DD}	134
MD5	200	$\overline{\text{RESET}}$	35	V_{DD}	144
MD6	199	STC 27 MHz CLK	139	V_{DD}	153
MD7	197	TTX DATA	182	V_{DD}	155
MD8	194	TTX DATA REQ	179	V_{DD}	157

Pin Assignments, Sorted by Signal Name

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
V_{DD}	163	V_{DDA2}	173	XPORT DATA 3	56
V_{DD}	166	V_{DDA2}	184	XPORT DATA 4	55
V_{DD}	172	VSC	171	XPORT DATA 5	50
V_{DD}	174	$\overline{WE}$	10	XPORT DATA 6	49
V_{DD}	175	$\overline{WP}$	80	XPORT DATA 7	48
V_{DD}	186	XPORT CLK	40	XPORT ERROR	43
V_{DD}	196	XPORT DATA 0	59	$\overline{XPORT PWM}$	47
V_{DD}	207	XPORT DATA 1	58	XPORT START	46
V_{DDA1}	32	XPORT DATA 2	57	XPORT VALID	45

Mechanical Dimensions

28.0 ±0.1 (sq) 30.6 ±0.2 (sq)

0.22 ±0.05   0.50

A

Seating Plane

0.08

Detail A

1.3

Gage Plane

4.1 max

0.25 min

3.4

0.145

0 - 8 Degrees

0.45 - 0.75

Not to scale.
All measurements in millimeters.
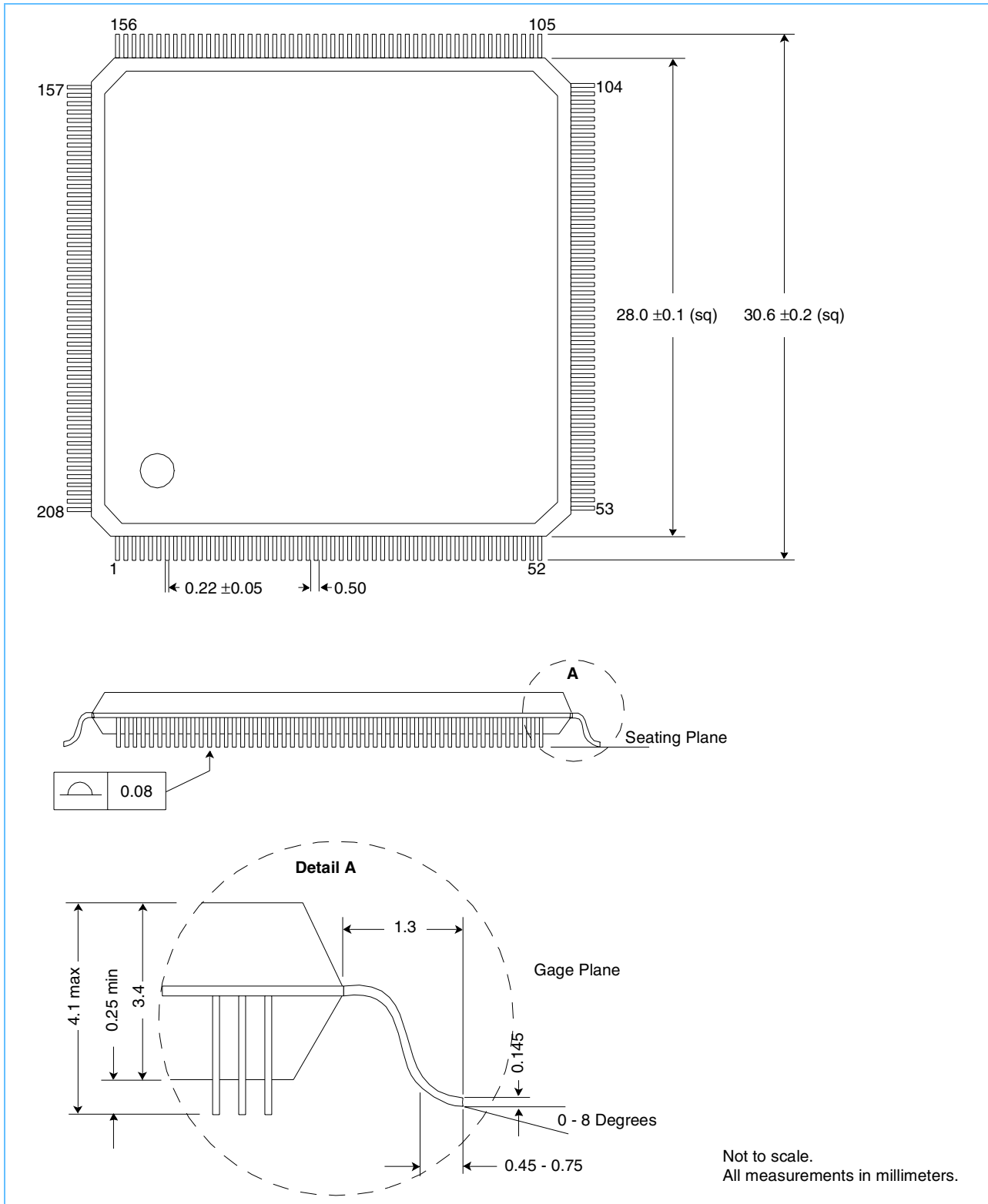
Revision Log

Revision	Contents of Modification
12/10/99	First release date. Revision 00.

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