FEATURES

- Fast Access Times: 25/35/45 ns
- Standard 24-Pin, 300-mil DIP
- Space Saving 24-Pin, 300-mil SOJ
- JEDEC Standard Pinout
- Separate Data Input and Output
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention

FUNCTIONAL DESCRIPTION

The LH52251A is a high-speed 262,144 bit static RAM organized as 256K × 1. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power drops to its lowest level (I_{SB1}) if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the D pin to the memory location specified by the 18 address lines. The Q pin goes into a High-Impedance state during Write cycles, allowing the user to connect D and Q together if desired.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read of the memory location specified by the address lines will occur. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

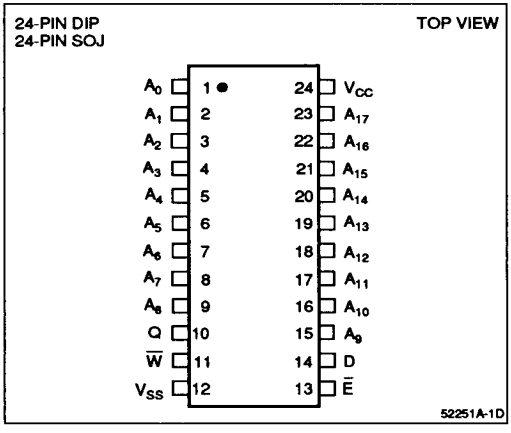

Figure 1. Pin Connections for DIP and SOJ Packages

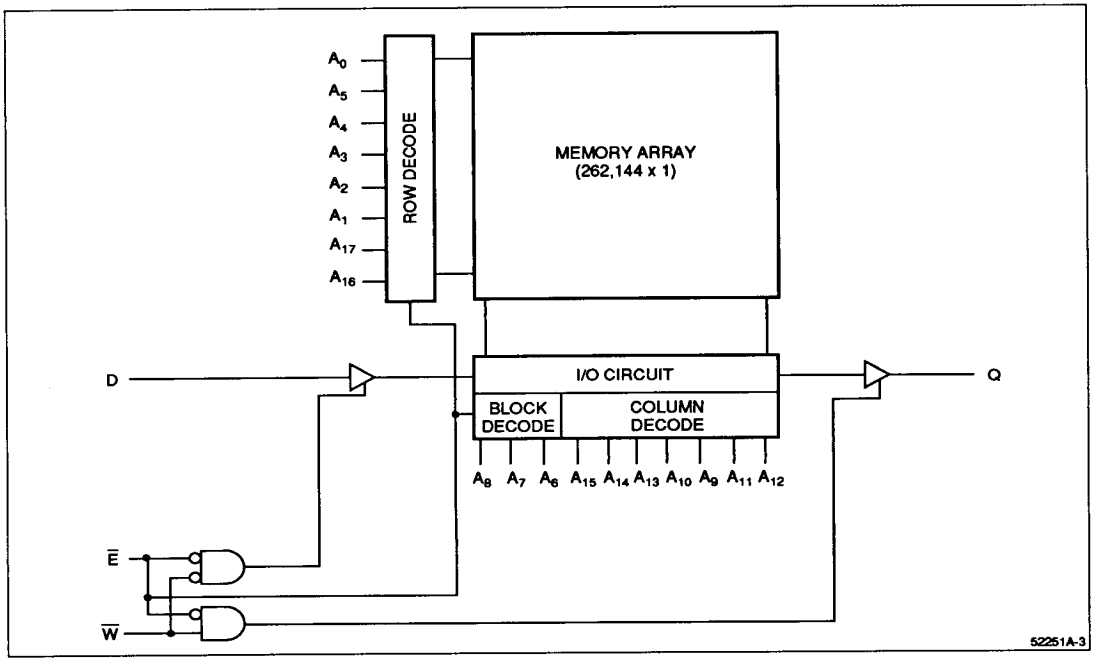

Figure 2. LH52251A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	D	Q	Icc
H	X	Not Selected	X	High-Z	Standby
L	H	Read	X	Data Out	Active
L	L	Write	Data In	High-Z	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{17}$	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
Operating Temperature	0 to 70°C

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Output should not be shorted for more than 30 seconds.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	Output open, t_{CYCLE} = 25 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IH}$ or V_{IL}			150	mA
I_{CC1}	Operating Current [1]	Output open, t_{CYCLE} = 35 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IH}$ or V_{IL}			120	mA
I_{CC1}	Operating Current [1]	Output open, t_{CYCLE} = 45 ns $\overline{E} = V_{IL}$, $\overline{W} = V_{IH}$ or V_{IL}			100	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ min			5	mA
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{IN} = 0 V to V_{CC}, V_{CC} = 5.5 V	−2		2	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{IN} = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{E} = V_{IH}$	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			250	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with output open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	0 to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

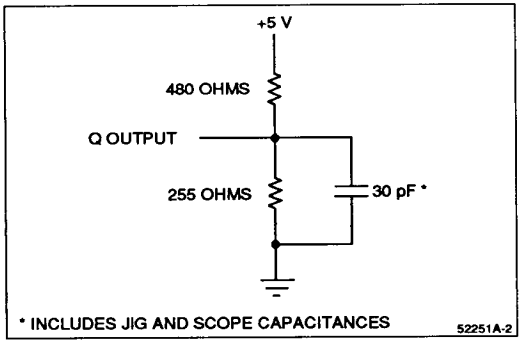

Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_D (Input Capacitance)	5 pF
C_Q (Output Capacitance)	7 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

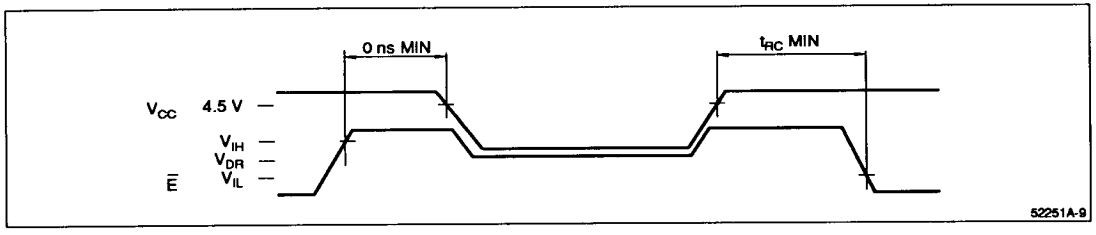

Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-25		-35		-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	25		35		45		ns
t_{AA}	Address Access Time		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		25		35		45	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		12		15		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{EW}	$\overline{E}$ Low to End of Write	20		30		40		ns
t_{AW}	Address Valid to End of Write	20		30		40		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		30		40		ns
t_{DW}	Input Data Setup Time	13		15		20		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		10		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		0		ns

NOTES:

1. AC Electrical Characteristics measurements specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to active output tests specified for a ±200 mV transition from steady state levels into the test load.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Q implies that Data Out is in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}.

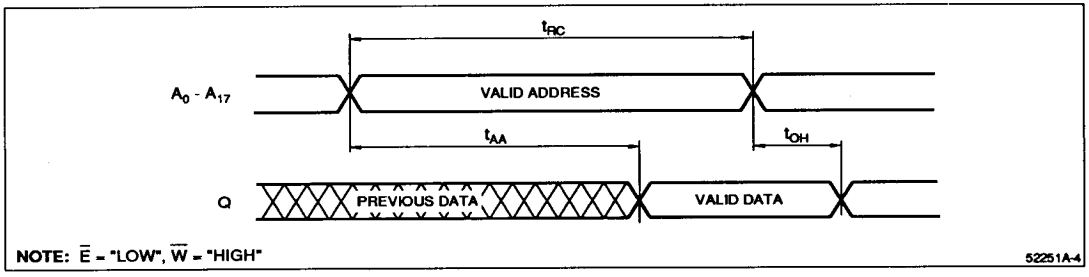

Figure 5. Read Cycle No. 1

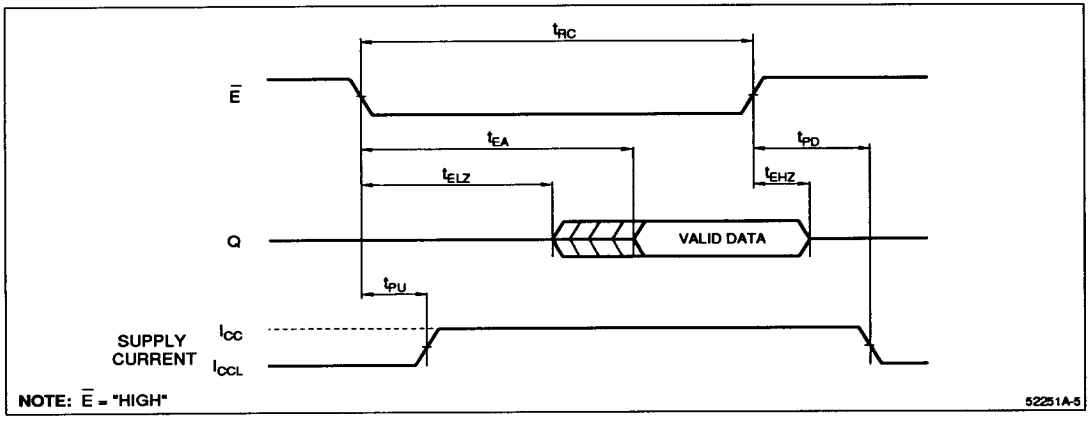

Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write Cycles. The output will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW.

Write Cycle No. 2 ($\overline{E}$ Controlled)

Data-out may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

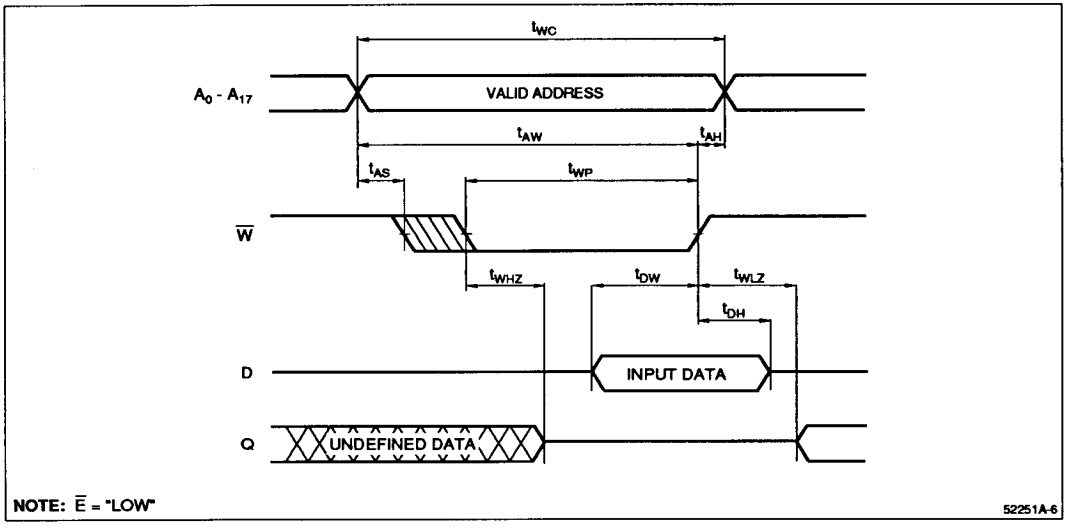

Figure 7. Write Cycle No. 1

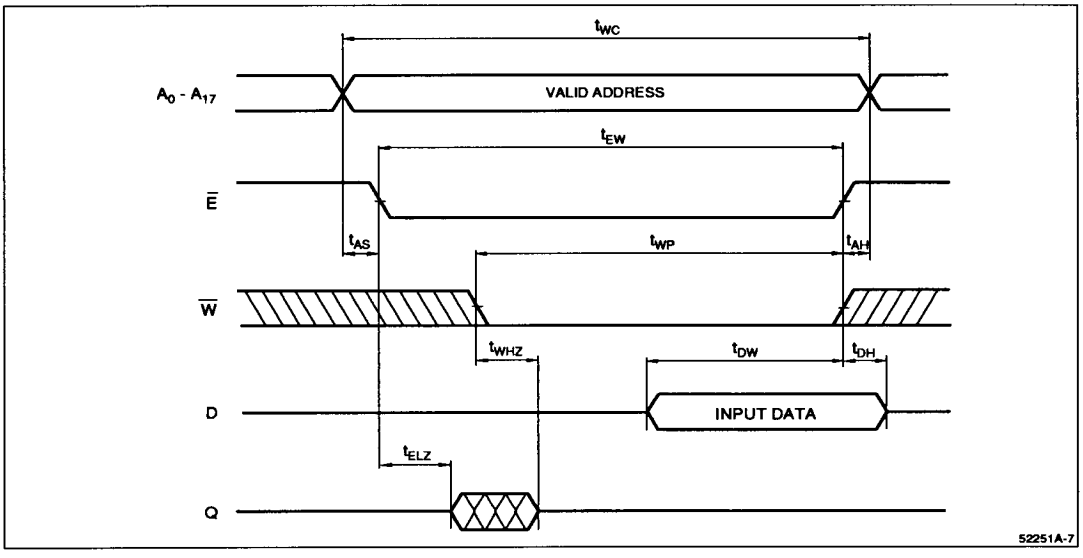

Figure 8. Write Cycle No. 2

ORDERING INFORMATION